

PRELIMINARY - October 5, 1999

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

## DESCRIPTION

The SC1538 is a dual power supply controller designed to simplify power management on motherboards. It is part of Semtech's Smart LDO™ family of products. The SC1538CS15/18 can provide a 1.818V power supply for the I/O plane and a 1.515V power supply for the GTL+ and AGP planes. The SC1538CS25/25 can provide two 2.525V supplies for clock and memory.

SC1538 features include Enable controls for each linear FET controller and over current protection. Over current protection is provided by feedback to the sense pins. If any output drops below 1V (typical) for greater than 4ms (typical), that output will shut down.

The SC1538 is available in a SO-8 surface mount package.

## FEATURES

- Dual power supplies
- 1.515V Supply for GTL+ and AGP planes/1.818V Supply for chipset I/O and memory termination
- Dual 2.525V supplies for clock and memory
- Individual Enable control of each supply
- Over current protection

## APPLICATIONS

- Motherboards
- Simple dual power supplies

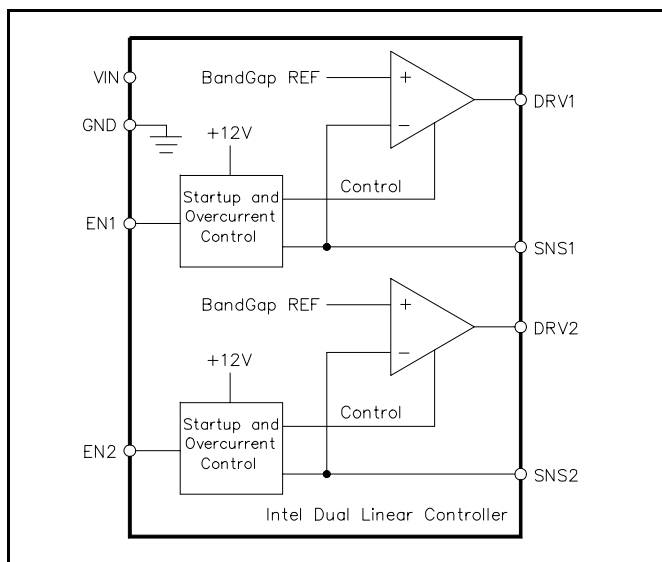
## ORDERING INFORMATION

Part Number <sup>(1)</sup>	Output Voltages	Package
SC1538CS15/18	1.515V and 1.818V	SO-8
SC1538CS25/25	2.525V and 2.525V	SO-8

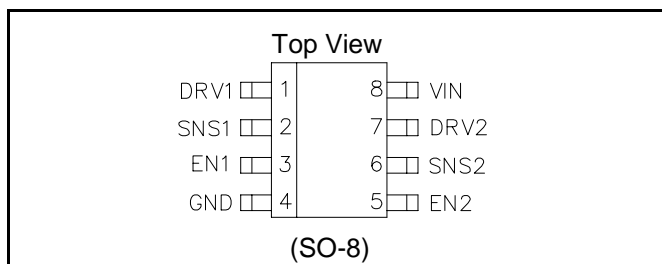
Note:

(1) Add suffix 'TR' for tape and reel packaging.

## BLOCK DIAGRAM



## PIN CONFIGURATION



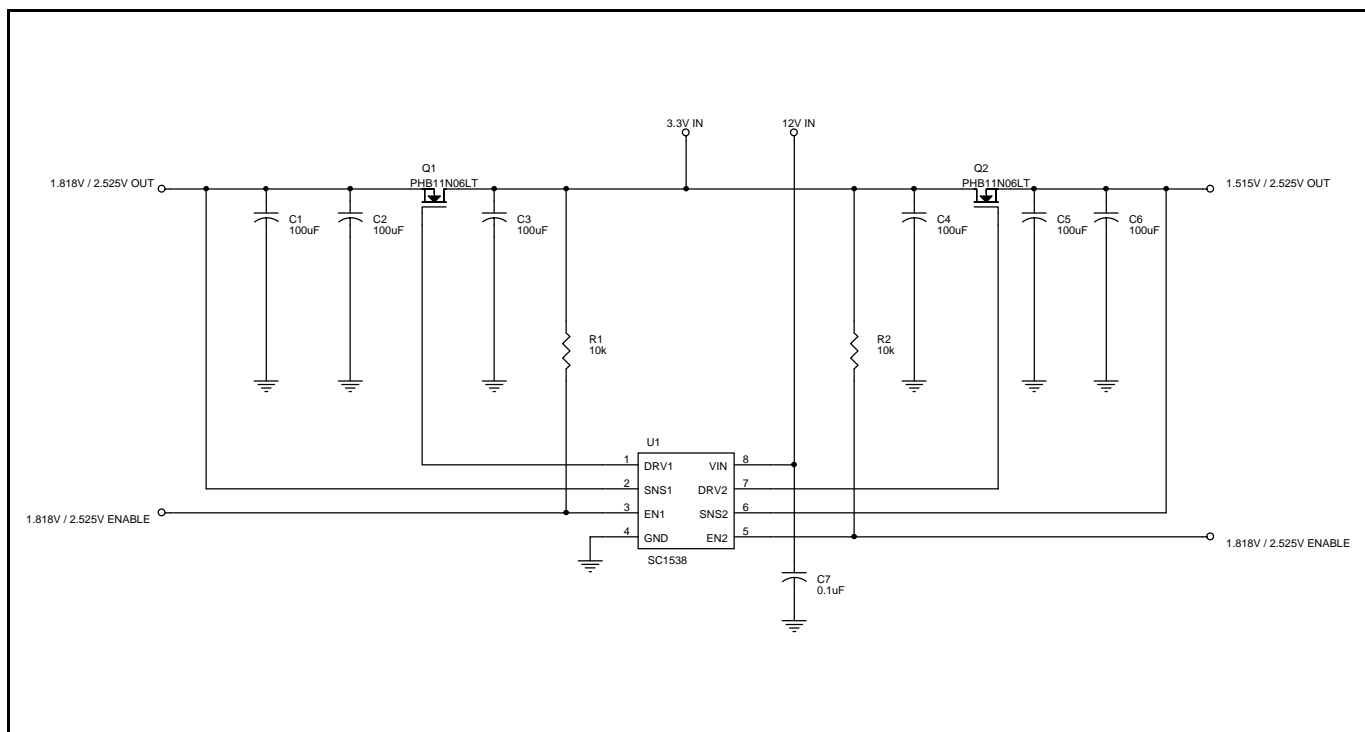
## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V <sub>IN</sub>	-0.5 to +15	V
Input Pins		-0.5 to +7	V
Operating Temperature Range	T <sub>A</sub>	0 to +70	°C
Operating Junction Temperature	T <sub>J</sub>	0 to +125	°C
Storage Temperature Range	T <sub>STG</sub>	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec	T <sub>LEAD</sub>	300	°C
Thermal Temperature Junction to Ambient	θ <sub>JA</sub>	130	°C/W
Thermal Impedance Junction to Case	θ <sub>JC</sub>	47	°C/W
ESD Rating	ESD	2	kV

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**PIN DESCRIPTION**

Pin	Pin Name	Pin Function
1	DRV1	Output of regulator #1. Drives the gate of an N-channel MOSFET to maintain 1.818V/ 2.525V.
2	SNS1	Regulator #1 Sense input. Use as a remote sense to the source of the N-channel MOSFET (Output 1).
3	EN1	Active high enable control with internal pullup. Output of regulator #1 turns off when EN1 is taken low.
4	GND	Ground
5	EN2	Active high enable control with internal pullup. Output of regulator #2 turns off when EN2 is taken low.
6	SNS2	Regulator #2 Sense input. Use as a remote sense to the source of the N-channel MOSFET (Output 2).
7	DRV2	Output of regulator #2. Drives the gate of an N-channel MOSFET to maintain 1.515V/ 2.525V.
8	VIN	+12V Supply.

**APPLICATION CIRCUIT**


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**ELECTRICAL CHARACTERISTICS**

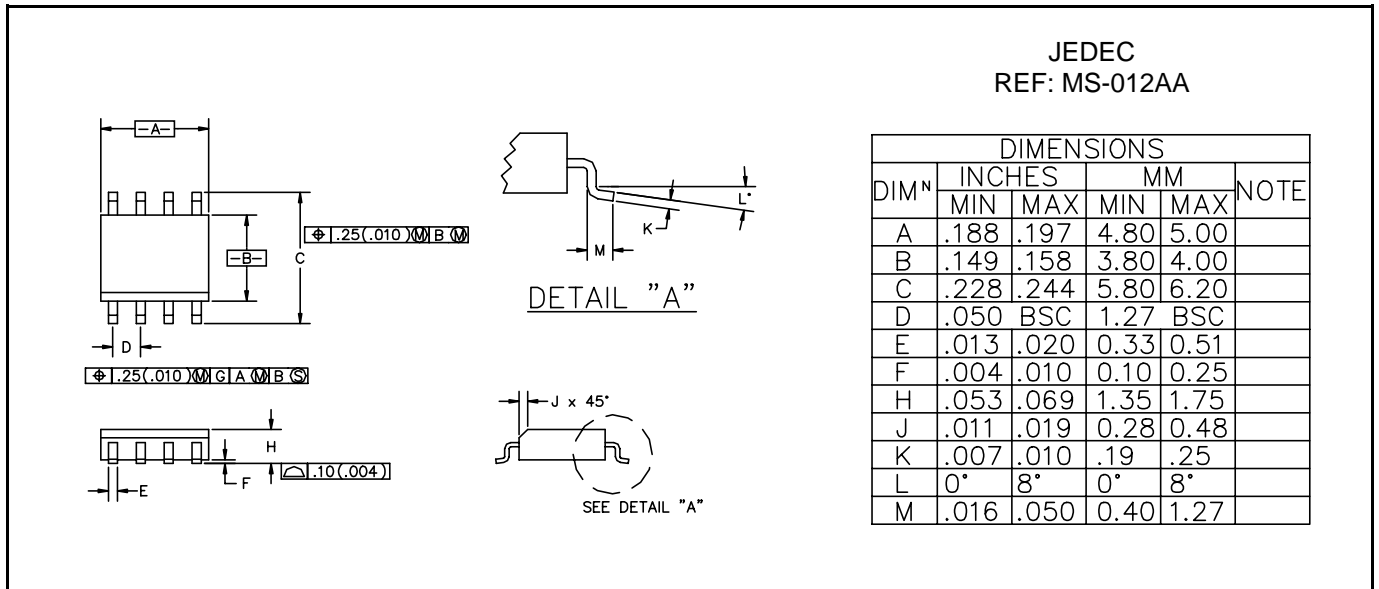
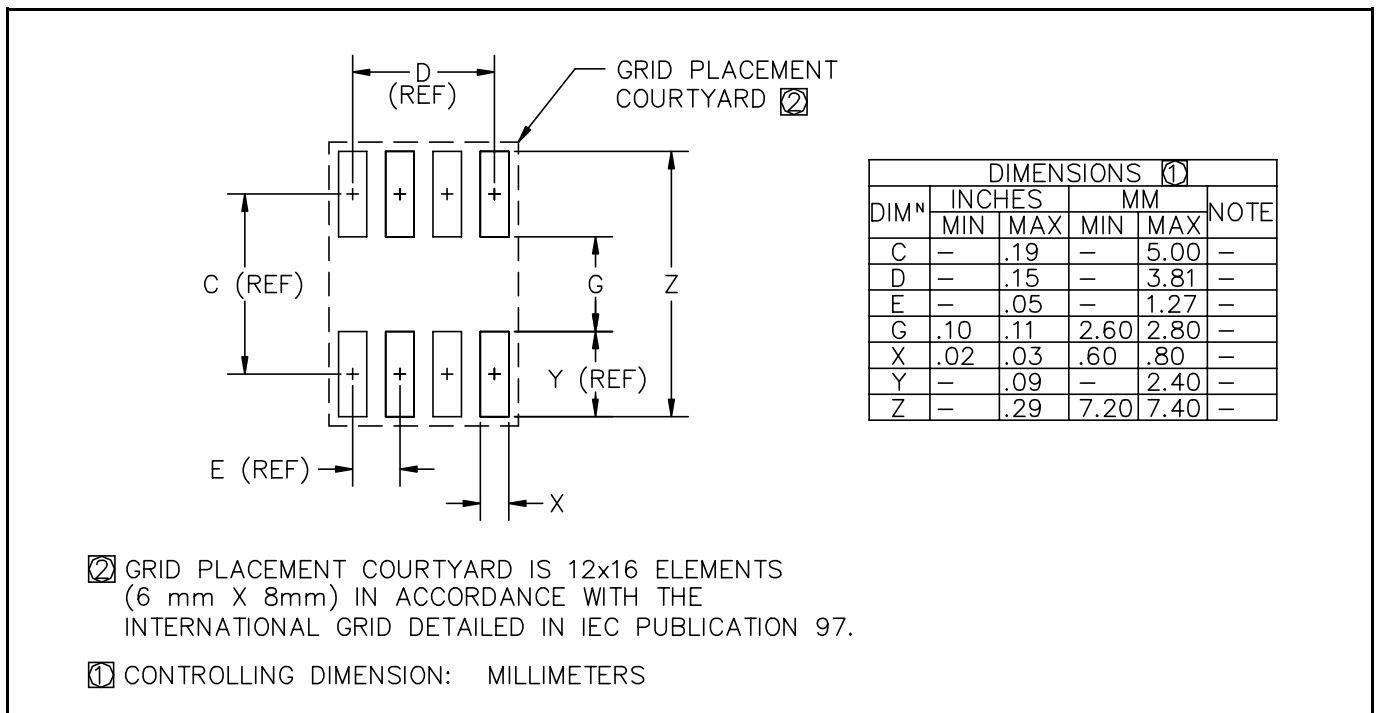
 Unless specified,  $T_A = 25^\circ\text{C}$ . Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
<b>VIN</b>						
Supply Voltage	VIN		<b>11.28</b>	12.00	<b>12.72</b>	V
Quiescent Current	I <sub>Q</sub>	Both EN High		2	3	mA
					<b>4</b>	
		One or both EN Low		1.5	2.0	mA
					<b>2.5</b>	
<b>Undervoltage Lockout</b>						
Start Threshold	UVLO		<b>7</b>	8	<b>9</b>	V
<b>Enable</b>						
Enable Pin Current	I <sub>EN</sub>	Input = Low		50	100	μA
					<b>150</b>	
Threshold Voltage	V <sub>TH</sub>	V <sub>EN</sub> rising	<b>1.6</b>		<b>2.3</b>	V
Hysteresis	V <sub>HYST</sub>		<b>100</b>	180	<b>300</b>	mV
Enable Delay Time <sup>(1)</sup>	t <sub>D(ON)</sub>	EN = Low to High, measured from EN = V <sub>TH</sub> to 10% DRV		500		ns
Disable Delay Time <sup>(1)</sup>	t <sub>D(OFF)</sub>	EN = High to Low, measured from EN = V <sub>TH</sub> to 90% DRV		150		ns
<b>DRV</b>						
Output Current	I <sub>DRV</sub>		<b>5</b>	10		mA
Output Voltage	V <sub>DRV</sub>	Full On	<b>9.0</b>	10.5		V
Rise Time <sup>(1)</sup>	t <sub>r</sub>	EN = Low to High, measured from EN = V <sub>TH</sub> to 90% DRV		1.6		ms
Fall Time <sup>(1)</sup>	t <sub>f</sub>			550		ns
<b>Output Voltage Regulation</b>						
Output Voltage <sup>(1)</sup>	VO	3.0V ≤ V <sub>FET</sub> <sup>(2)</sup> ≤ 3.6V, 1mA ≤ I <sub>O</sub> ≤ 1A	-1.5%	VO	+1.5%	V
			<b>-2.5%</b>		<b>+2.5%</b>	
<b>Overcurrent Protection</b>						
Trip Threshold	V <sub>OC</sub>		<b>-20%</b>	1.00	<b>+15%</b>	V
Power-up Output Short Circuit Immunity			1	5	60	ms
Output Short Circuit Glitch Immunity			0.5	4	6	ms
<b>Control Section</b>						
Bandwidth		DRV = 9V, THD = 5%, C <sub>L</sub> = 600pF		5		MHz

**NOTES:**

- (1) See Application Circuit  
 (2) Connected to FET drains.

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**OUTLINE DRAWING - SO-8**

**LAND PATTERN - SO-8**


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