SC192
Synchronous Buck Converter with Integrated Power Devices

Description

The SC192 is a synchronous step-down converter with integrated power devices designed for battery operated systems. The internal power switches reduce system size and cost. In addition, an efficiency of 95% can be achieved for significant line and load ranges. The SC192 is designed for single-cell Li-Ion battery applications, but also performs well in fixed 3.3V or 5V input circuits.

The SC192 has a flexible clocking scheme. It can be synchronized to an external oscillator, fixed to the internal oscillator, or allowed to modulate the frequency during light loads (PSAVE) for maximum battery life, by the method called pulse frequency modulation (PFM). Shutdown places the switches in a high impedance state and turns off all control circuitry to achieve a typical quiescent current of 0.1µA.

Line and load regulation is to +/-0.5% of the output voltage. The internal MOSFET switches provide >1A peak current to provide a DC output of at least 700mA. Grounding the ILIM pin reduces the current limit by half.

The SC192 can achieve 100% duty cycle for excellent low dropout performance and comes in a tiny MLPD-10, 3 x 3 package having a maximum height of 1mm.

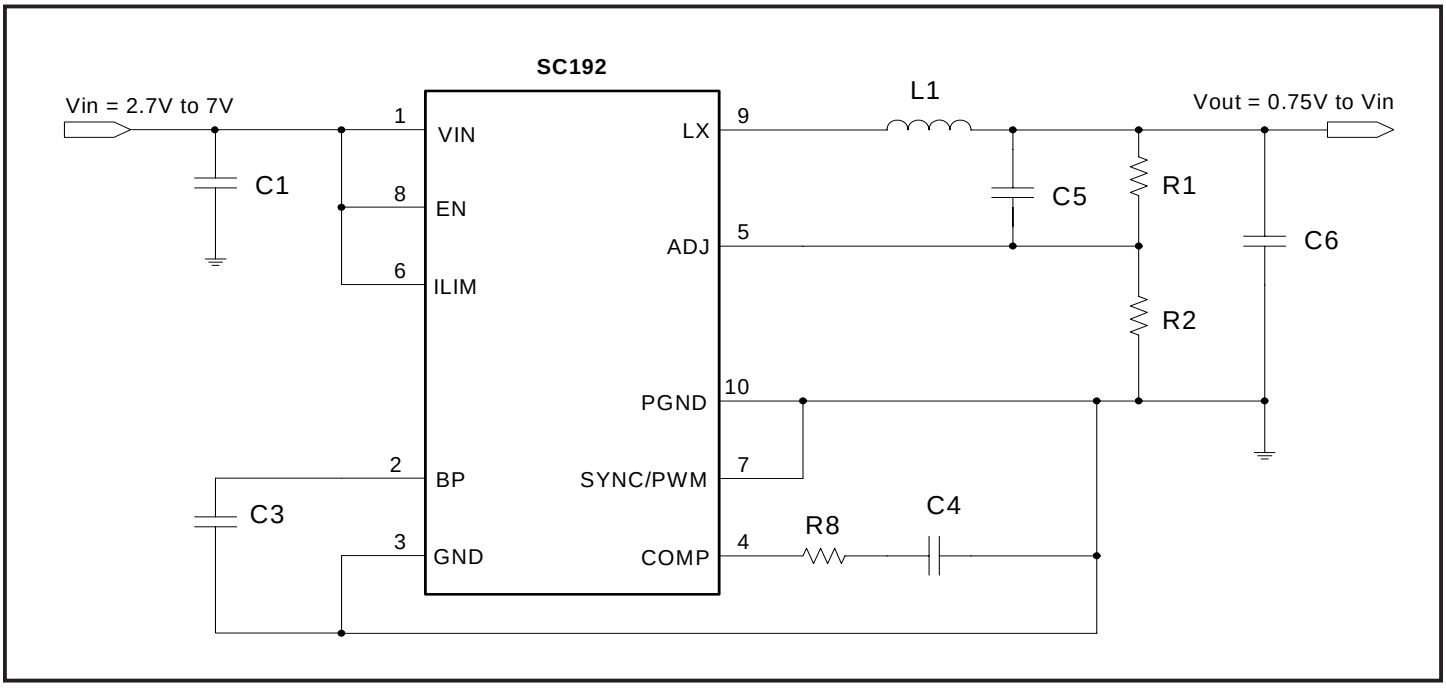
Features

- 2.7V to 7V Input Range
- Output Adjustable from 0.75V to Vin
- Fixed Frequency or PSAVE for Maximum Efficiency Over Wide Load Current Range
- 700mA Guaranteed Output Current
- No Schottky Diode Required
- 35µA Quiescent Current
- 100% Duty Cycle in Dropout
- 95% Efficiency
- Fast Transient Response
- Over Temperature Protection
- Space-saving Micro Lead-Frame Package MLPD-10 3x3

Applications

- Cell Phones
- Cordless Phones
- Notebook and Subnotebook Computers
- PDAs and Mobile Communicators
- 1 Li-Ion or 3 NiMH/NiCd Powered Devices

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
VIN input	V_{IN}	-0.3 to 7.5	V
SYNC/PWM Input	V_{SYNC}	-0.3 to 7.5	V
EN Input	V_{EN}	-0.3 to 7.5	V
PGND to GND	V_{PGDN}	-0.3 to 0.3	V
LX Voltage	V_{LX}	-1 to VIN +1	V
ILIM Voltage	V_{ILIM}	-0.3 to VIN + 0.3	V
ADJ Voltage	V_{ADJ}	-0.3 to VIN + 0.3	V
COMP Voltage	V_{COMP}	-0.3 to VIN + 0.3	V
BP Voltage	V_{BP}	VIN - 0.3 to VIN + 0.3	V
Thermal Impedance Junction to Ambient	θ_{JA}	*57	˚C/W
Output Short Circuit to GND	t_{SC}	Continuous	s
LX Current	I_{LX}	+1.6	A
Peak IR Reflow Temperature SC192IMLTR (Soldering) 10s - 30s SC192IMLTRT (Soldering) 20s - 40s	T_{LEAD}	 240 260	˚C
Storage Temperature	T_S	-65 to +160	˚C

* Tied to PCB with 1 square inch, 2 ounce copper.
Note: This device is ESD sensitive. Use of ESD handling precautions is required.

Electrical Characteristics

Unless otherwise noted: VIN = 3.6V, SYNC/PWM = VIN, ILIM = VIN, EN = VIN, T_A =-40 to 85°C. Typical values are at T_A = +25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.7		7	V
ADJ Regulation Voltage	V_{ADJ}		0.731	0.75	0.769	V
ADJ Input Current	I_{ADJ}	ADJ = 0.75V	-50	0	50	nA
Output Voltage Adjust Range	V_{OUT}		V_{ADJ}		V_{IN}	V
Line Regulation	REG_{LINE}		-0.5		+0.5	%
Load Regulation(1)	REG_{LOAD}	Peak Inductor Current = 0 to 700mA	0		0.6	%
P-Channel On Resistance	R_{DSP}	I_{LX} = 200mA		0.3		Ω
N-Channel On Resistance	R_{DSN}	I_{LX} = 200mA		0.4		Ω

Electrical Characteristics Cont.

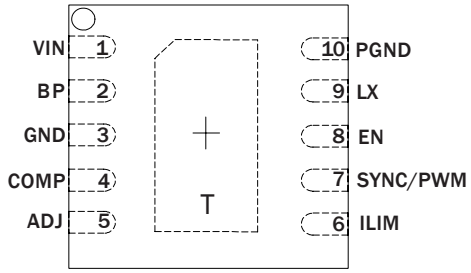
Unless otherwise noted: VIN = 3.6V, SYNC/PWM = VIN, ILIM = VIN, EN = VIN, T_A =-40 to 85°C. Typical values are at T_A = +25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
P-Channel Current Limit	$I_{LIM(P)}$	ILIM = GND	420	600	780	mA
		ILIM = V_{IN}	840	1200	1560	mA
N-Channel Current Limit	$I_{LIM(N)}$	SYNC/PWM = GND, PSAVE Mode	45	105	165	mA
			-320	-420	-520	mA
Quiescent current	I_Q	SYNC/PWM = GND, PSAVE Mode		35	50	µA
Shutdown Current	I_{SD}	EN = 0, LX = Open, T_A = 25˚C			1	µA
LX leakage Current PMOS	I_{LXP}	VIN = 5.5V, LX = 0V, EN = 0V			1	µA
LX leakage Current NMOS	I_{LXN}	VIN = 5.5V, LX = 5.5V, EN = 0V	-20			µA
Oscillator Frequency	f_{OSC}		650	750	830	kHz
SYNC Frequency Range	f_{SYNC}		500		1000	kHz
Duty Cycle Range	D	SYNC/PWM = GND, PSAVE Mode	20		100	%
UVLO Threshold	V_{UVL}		2.35	2.5	2.65	V
UVLO Hysteresis	V_{UVLHYS}			50		mV
Thermal Shutdown				160		˚C
Logic Input High	V_{IH}	EN, SYNC/PWM, ILIM	2			V
Logic Input Low	V_{IL}	EN, SYNC/PWM, ILIM			0.8	V
Logic Input Current High	I_{IH}	EN, SYNC/PWM, ILIM	-2		2	µA
Logic Input Current Low	I_{IL}	EN, SYNC/PWM, ILIM	-2		2	µA

Notes:
(1) Load regulation limits are specified from 0 to 700mA. This specification is calculated based on parameters measured individually and is not a tested parameter. See the load regulation limit graph on page 13 for more detailed view of performance.

Pin Configuration

TOP VIEW



MLPD-10: 3X3 10 LEAD

Ordering Information

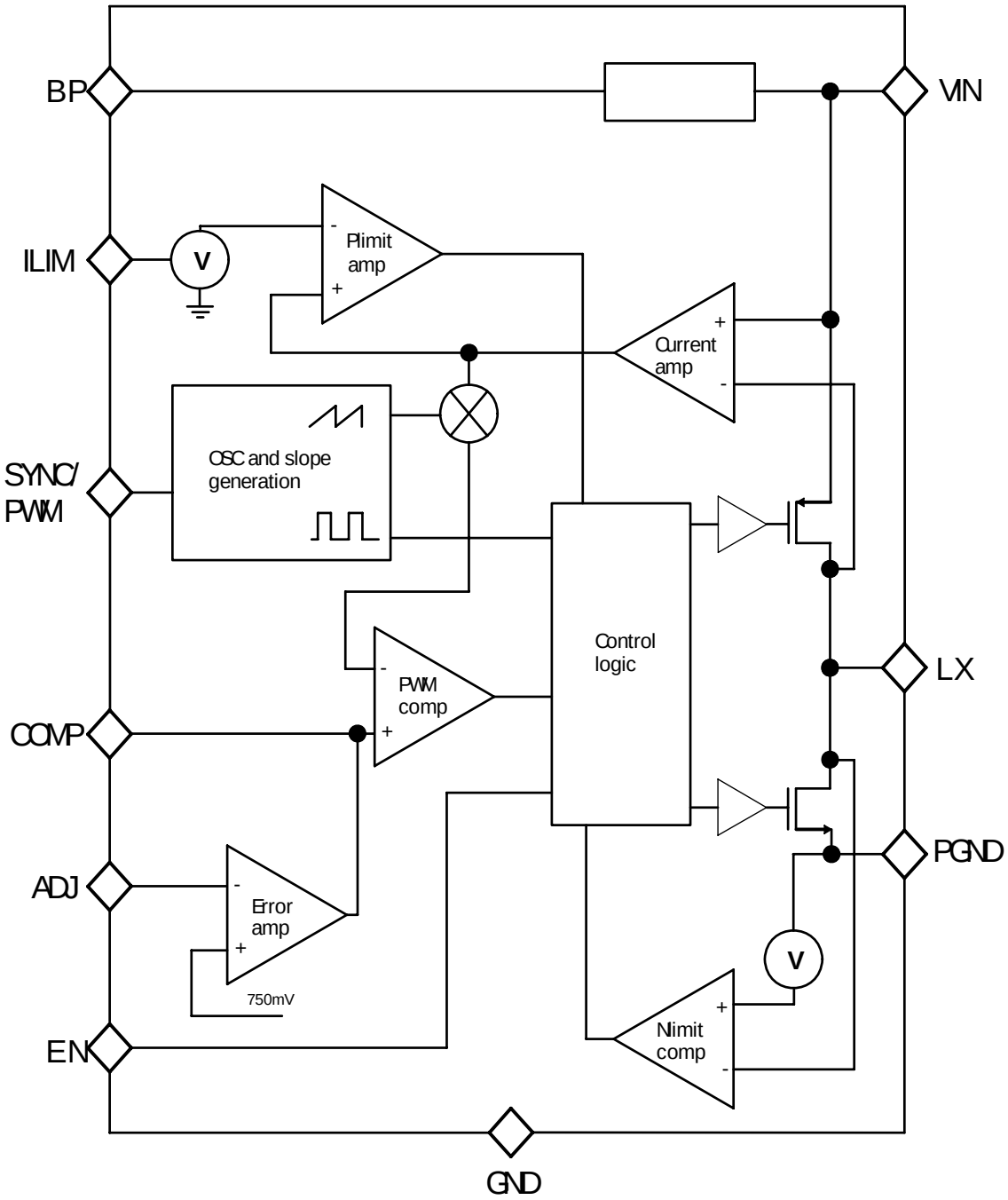
DEVICE[1]	PACKAGE
SC192IMLTR	MLPD-10 3x3
SC192IMLTRT[2]	
SC192EVB	Evaluation Board

Note:
(1) Only available in tape and reel packaging. A reel contains 3000 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	VIN	Input power supply voltage; this input goes directly to the internal MOSFET switches.
2	BP	Bypass capacitor pin; an external capacitor combined with an internal resistor provides a filtered supply voltage for the internal control circuitry. Connect a 0.1uF capacitor from BP to ground.
3	GND	Analog ground.
4	COMP	Compensation pin for the error amplifier.
5	ADJ	Output adjust pin; connect to a resistor divider to set the output voltage.
6	ILIM	Digital current limit select input. Connect ILIM to GND for 0.6A current; connect ILIM to VIN for 1.2A current limit.
7	SYNC/PWM	Oscillator synchronization input. Tie to VIN for forced PWM mode, GND to enable power save mode, or an external clock signal for frequency synchronization.
8	EN	Enable digital input; a high input enables the SC192 a low disables the device and reduces quiescent current to 0.1uA. In shutdown, LX becomes high impedance.
9	LX	Inductor connection to the switching FETs.
10	PGND	Power Ground.
T	Thermal Pad	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

Block Diagram



Description

Description

The SC192 step-down, pulse-width-modulated (PWM), DC-DC converter has an adjustable output range from 0.75V to the input voltage. The device has an internal synchronous rectifier and does not require a schottky diode on the LX pin.

At moderate to heavy loads, the converter operates in the PWM mode with a fixed frequency of 750kHz. At light loads the converter enters the power save mode by modulating the frequency, pulse-frequency-modulation (PFM) which achieves high efficiency under light load conditions.

Normal Mode

This is a standard fixed frequency current mode topology. The current feedback is through the PMOS current path and is amplified and summed with the internal slope compensation network and DC offset. The voltage feedback loop is through the resistor divider attached to the ADJ pin. The transconductance error amplifier output is the compensation (COMP) pin with the usual external compensation network attached. The PWM COMP pin closes the loop by comparing the summed current feedback and the COMP signal to determine the length of the ON time. The period is set by the on-board oscillator or external clock attached to the SYNC pin.

Power Save Mode

If SYNC/PWM is DC low, power save mode is used at light loads to improve efficiency. When the output current reaches a low enough level, the part goes into a voltage hysteresis mode of operation. The current level for this is set to be the current reversal protection on the NMOS device. The output voltage is then allowed to decay to a lower threshold with the part in a reduced quiescent current (PSAVE) state. After this lower threshold is reached the part is reawoken to normal operation, but with a current offset on the COMP pin to drive the output voltage regulation point to be above an upper threshold point. However the offset is removed once the upper threshold is reached. If the load current is now sufficiently large the part will return to normal regulation, if not another PSAVE cycle will start.

Frequency Foldback

When the ADJ pin is low the output switching frequency is folded back in several discrete steps to protect against a short to GND on the output and improve inrush current control during start-up.

Forced PWM

If SYNC/PWM is DC high, the forced PWM mode is enabled. This ensures that the switching frequency of the converter is maintained over the full range of output loads. This means that the current reversal threshold of the NMOS is changed to a negative value and the 100% duty cycle and power save modes are also disabled.

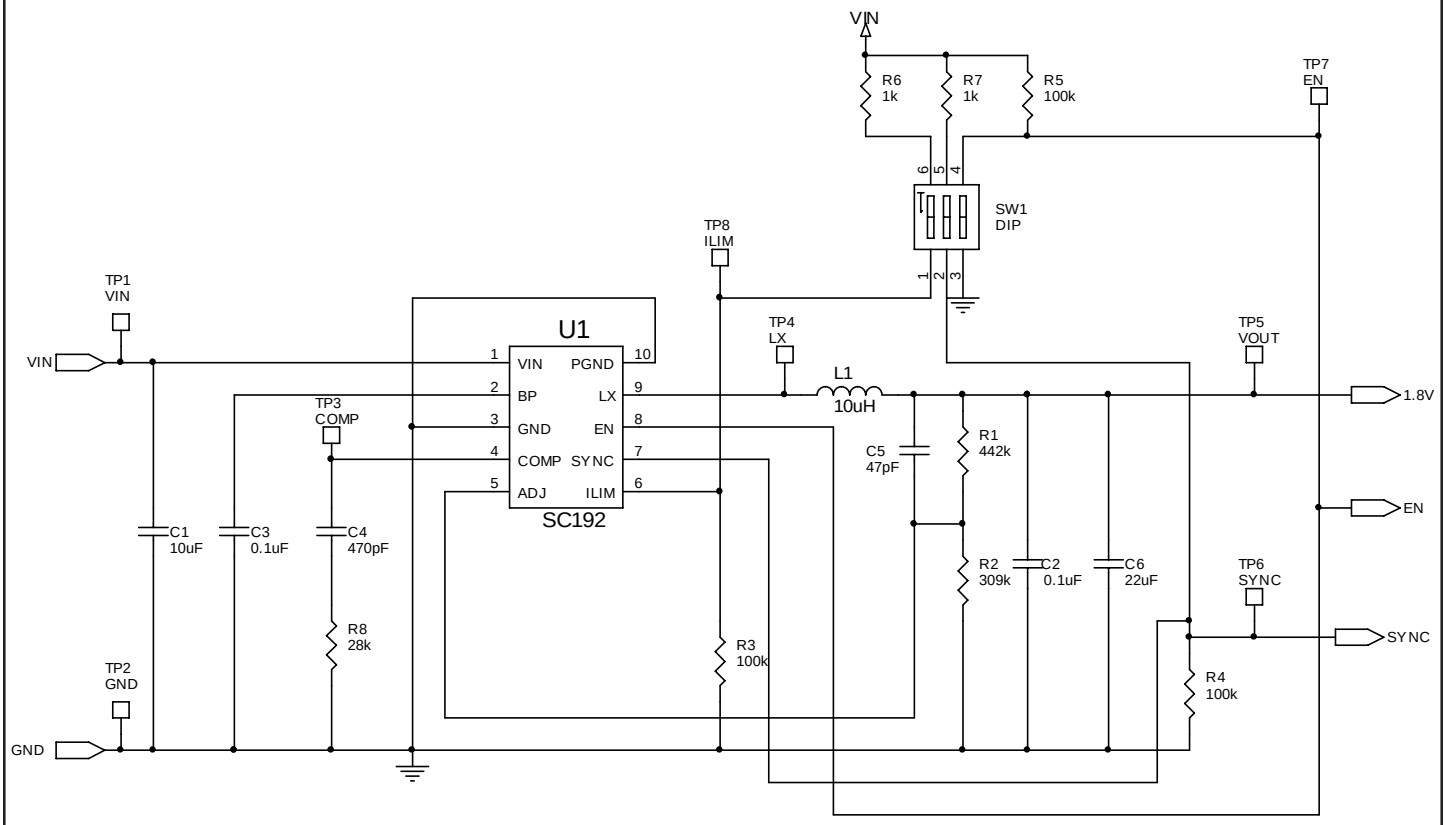
100% Duty-Cycle Operation

Normally the control loop constrains the duty cycle of the converter with minimum on and off times, but if the output voltage droops to the lower power-save threshold and the ON time is not terminated by the PWM comparator or PMOS current limit, then the next PMOS on time is allowed to extend until either the PWM comparator or PMOS current limit trips. This is then followed by a minimum off time. This maximum on time/minimum off time is allowed to continue until the upper power-save threshold is reached. This allows the part to go into a dropout mode of operation if the input supply collapses down to the output voltage. If this happens, the output voltage is equal to the input voltage minus the voltage drop across the P-channel MOSFET.

Soft Start

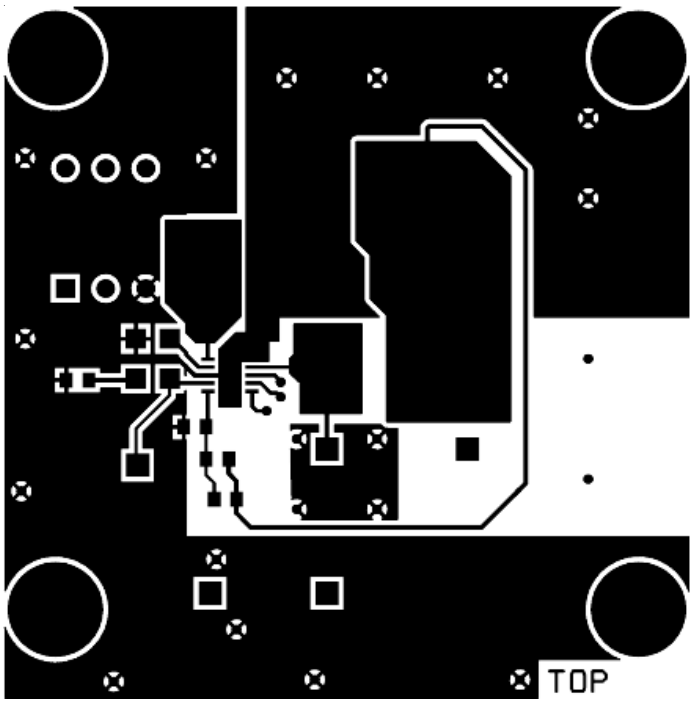
The soft start mode is enabled after every shutdown cycle to limit inrush current from the battery. In conjunction with the frequency foldback this controls the maximum current during start-up. The PMOS current limit is stepped from 25%, to 50%, to 75%, and then 100% by an internal 2ms timer. As soon as the part reaches regulation, soft start mode is disabled.

Evaluation Board Schematic

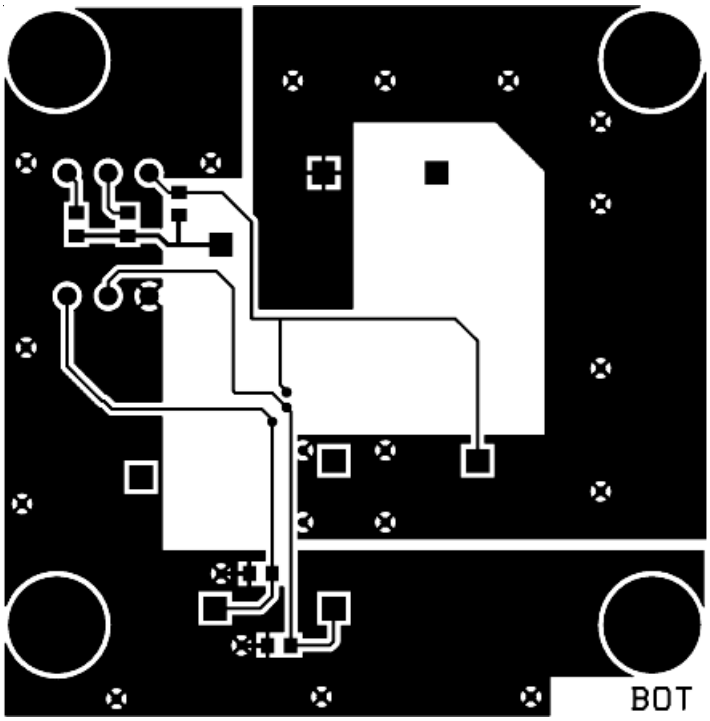


Evaluation Board Gerber Plots

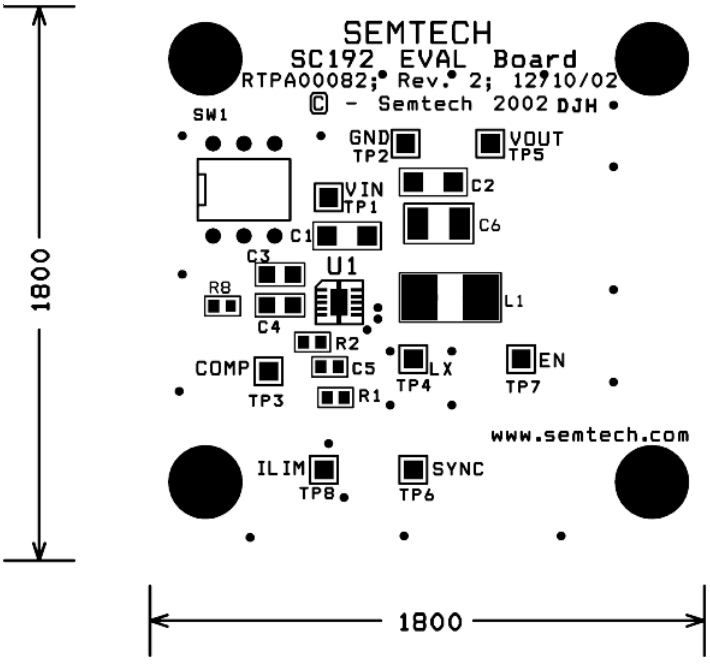
TOP COPPER



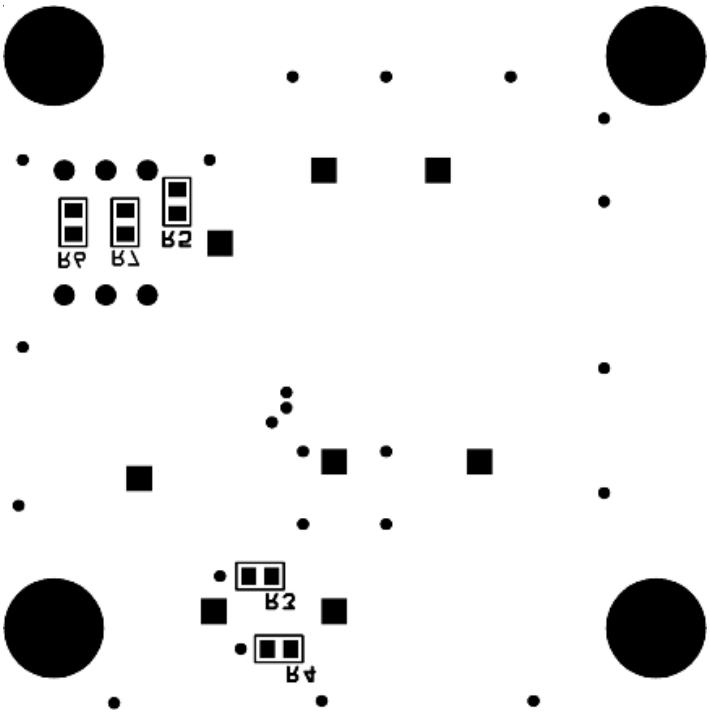
BOTTOM COPPER



TOP SILKSCREEN



BOTTOM SILKSCREEN



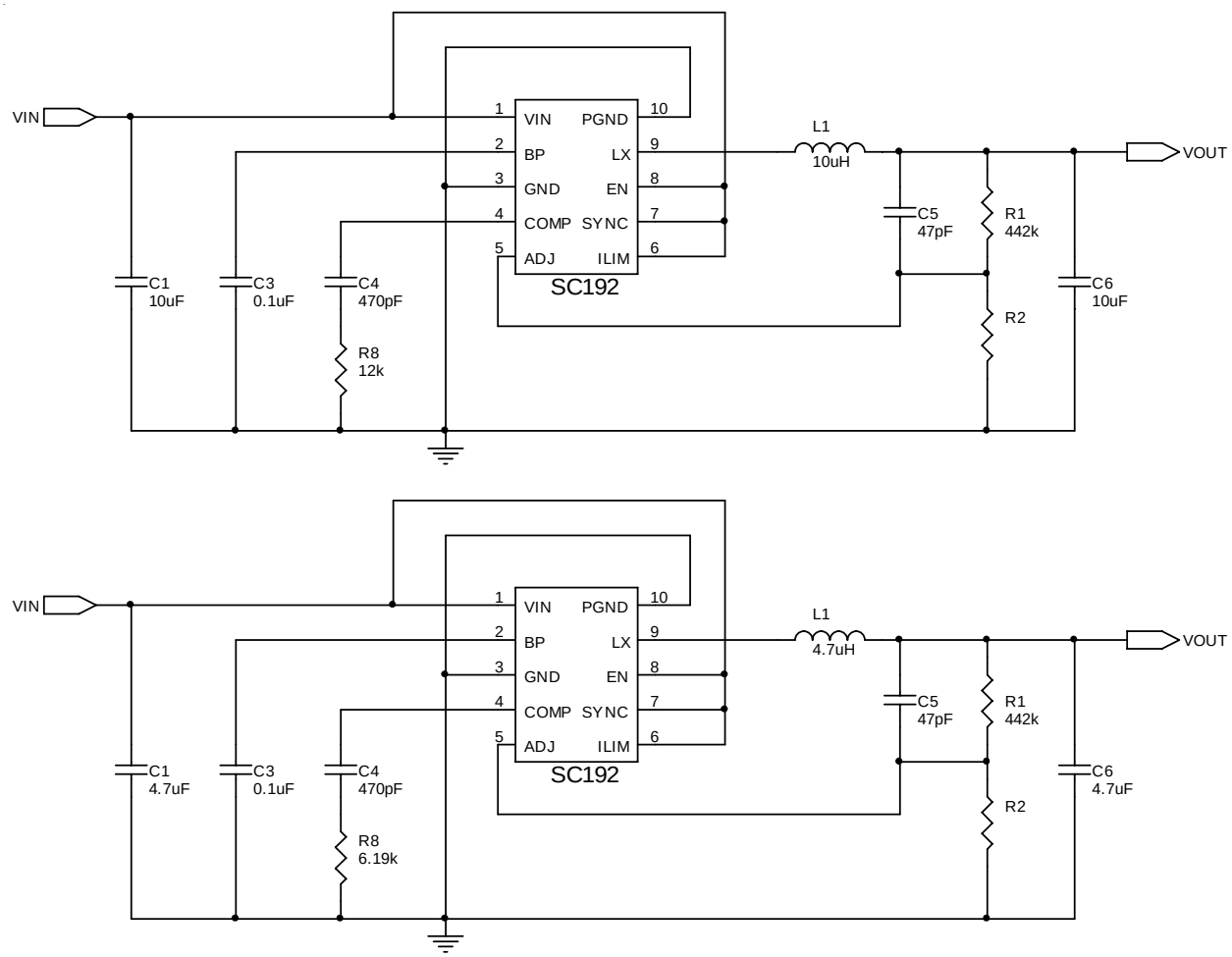
Applications Information

Selecting Components

When selecting components for the an SC192 application the main factors are typically performance, size and cost. For higher performance the designer will select higher values of input and output capacitors to reduce ripple current and voltage. However, for an application that can tolerate higher ripple, less expensive and smaller components can be utilized. The schematics below show two possibilities. The first shows the use of 10µF capacitors on the input and output with L1 = 10µH, while the second shows the use of smaller less expensive 4.7µF capacitors and L1 = 4.7µH. The only circuit consideration for choosing one over the other is the compensation components C4 & R8. When these components are in place the values of R2 can be chosen for a given output voltage. The values that should be used are indicated in Table 1 below. Using a different value for R1 is not advised since this will change the loop characteristics and may cause the supply to become unstable. Any output voltage is achievable using R1 of 442k and then selecting R2 to achieve the desired output voltage. The equation for VOUT is:

$$Vout = \left(\frac{R1}{R2} + 1\right) \bullet 0.75$$

Because the SC192 has external compensation the use of small inexpensive ceramic capacitors can be used for the output capacitor allowing the designer greater flexibility.



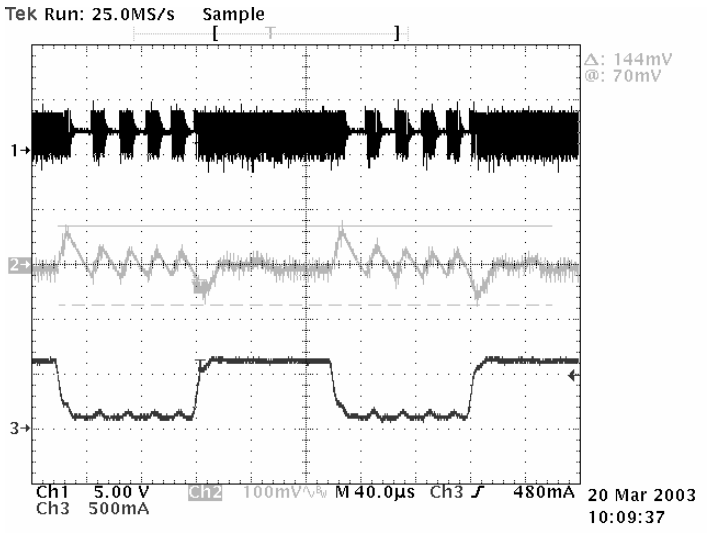
Applications Information Cont.

TABLE 1

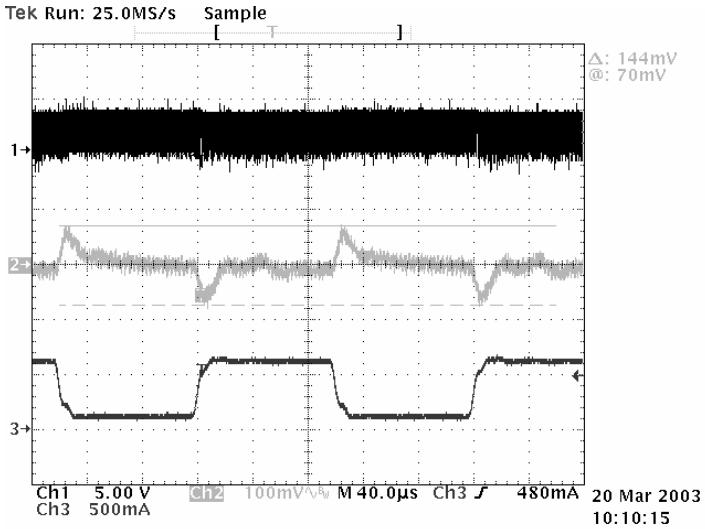
VOUT	R2	C6 = Cout = 10uF L1 = 10uH	C6 = Cout = 22uF L1 = 10uH	C6 = Cout = 4.7uF L1 = 4.7uH
3.3V	130k	C4 = 470pF R8 = 12k	C4 = 470pF R8 = 28k	C4 = 470pF R8 = 6.19k
2.5V	187k			
1.8V	309k			
1.5V	442k			
1.0V	1.30M			

The plots below were taken at Vin = 3.6V, Vout = 1.8V, with the compensation components listed in Table 1. The upper plot is LX, the middle plot is output voltage, the lower plot is the current transient of 0.1A to 0.6A

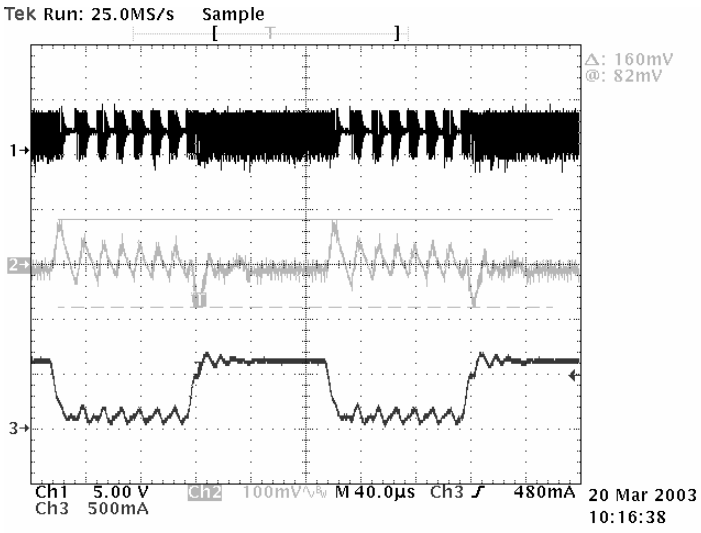
PSAVE, Cout = 20uF, Lout = 10uH



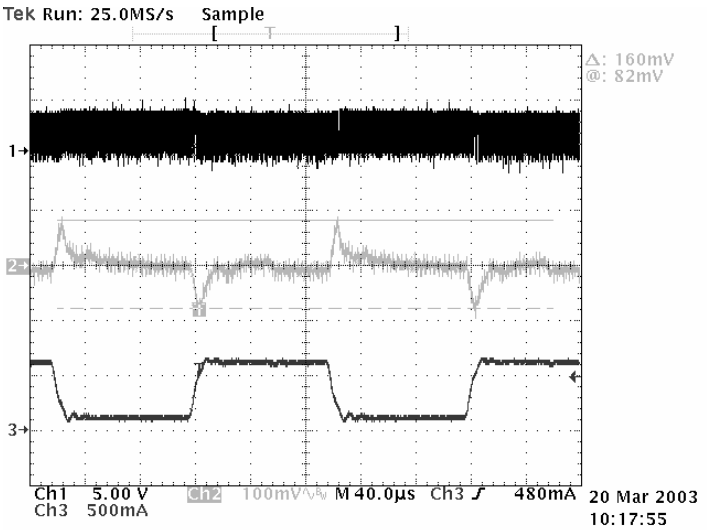
PWM, Cout = 20uF, Lout = 10uH



PSAVE, Cout = 10uF, Lout = 10uH

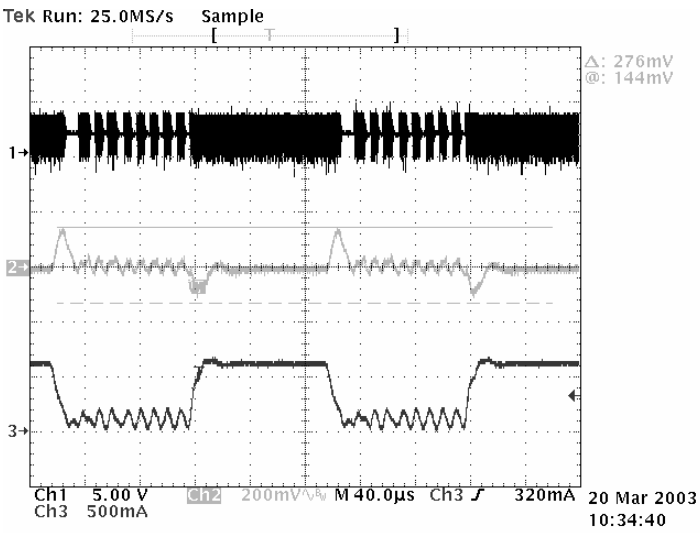


PWM, Cout = 10uF, Lout = 10uH

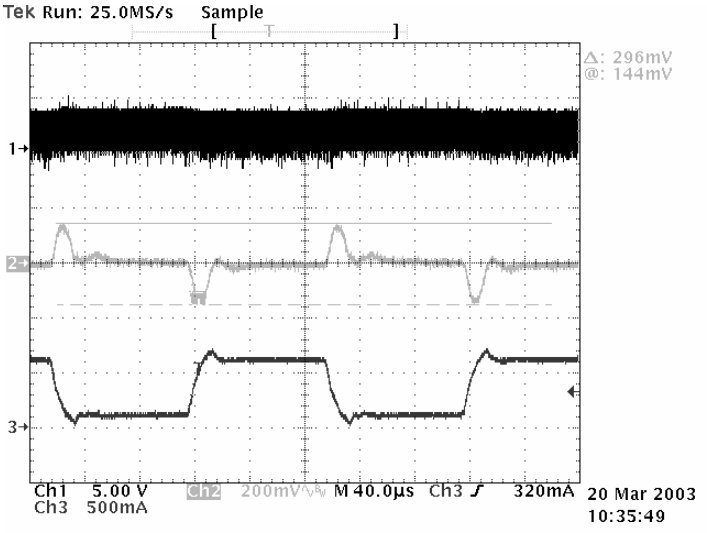


Applications Information Cont.

PSAVE, Cout = 4.7uF, Lout = 4.7uH



PWM, Cout = 4.7uF, Lout = 4.7uH



Inductor Selection

The inductor values listed in Table 1 will work for nearly all combinations of output current and output voltages. After selecting 4.7uH or 10uH for the inductor value two additional inductor parameters should be considered. The current rating of the inductor and the DC resistance.

The DC resistance has a great impact on efficiency due to copper losses. However, small inductors tend to have higher DC resistance. Therefore a compromise between size and efficiency will need to be made.

The inductor current must be chosen to prevent the inductor from saturation. The most conservative approach would be to select an inductor with a saturation current slightly above the maximum current capability of the SC192 which is 1.56A peak current for ILIM = Vin or 780mA for ILIM = GND.

A more accurate design of the inductor would be to rate the inductor for the maximum output current plus the inductor ripple current that can be calculated as follows:

$$I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \bullet f} \right) \bullet V_{OUT}$$

f = Switching frequency
L = Inductor Value
ΔI_L = Peak-to-peak inductor ripple current
I_L = Maximum inductor current
V_{OUT} = Output voltage
V_{IN} = Input voltage
C_{OUT} = Output Capacitance
I_{OUT} = Output Current
$I_{OUT(MAX)}$ = Maximum DC Output Current

Output Capacitor Selection

Because the SC192 has external compensation available, low ESR ceramic capacitors can be used. This eliminates the need for bulky tantalum capacitors. Values for the output capacitors in Table 1 will work for nearly all combinations of output current and output voltages. The equation for determining the size of the output capacitor in terms of minimizing the ripple voltage is given as follows:

$$\Delta V_O = \Delta I_L \bullet \left(\frac{1}{8 \bullet C_{OUT} \bullet f} + ESR \right)$$

Input Capacitor Selection

The input ripple current can be reduced with properly selecting the input capacitor. Again, values for the input capacitors in Table 1 will work for nearly all combinations of input current and output voltages. The input capacitor should be rated for the maximum input ripple current calculated as:

Applications Information Cont.

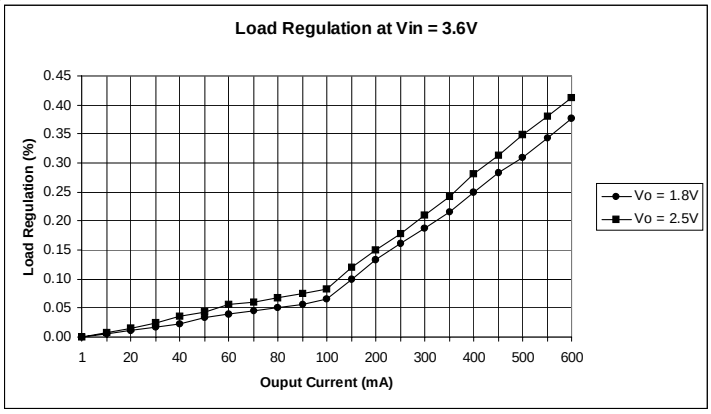
$$I_{RMS} = \sqrt{V_{OUT} \bullet V_{IN} - V_{OUT}} \bullet \frac{I_{OUT}}{V_{IN}}$$

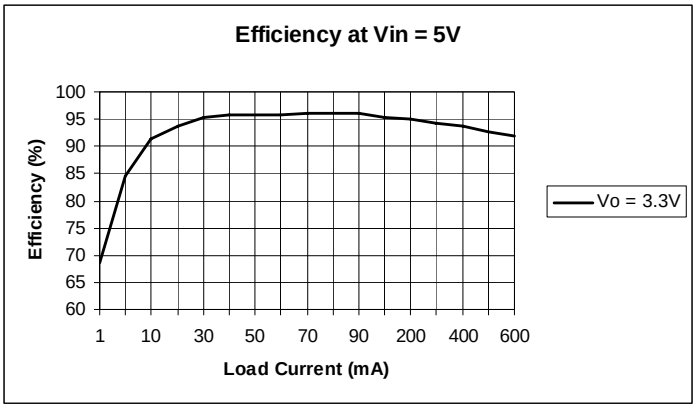
The worst case RMS ripple current occurs at a duty cycle of 0.5 and its value at that point is $\frac{I_{OUT}}{2}$.

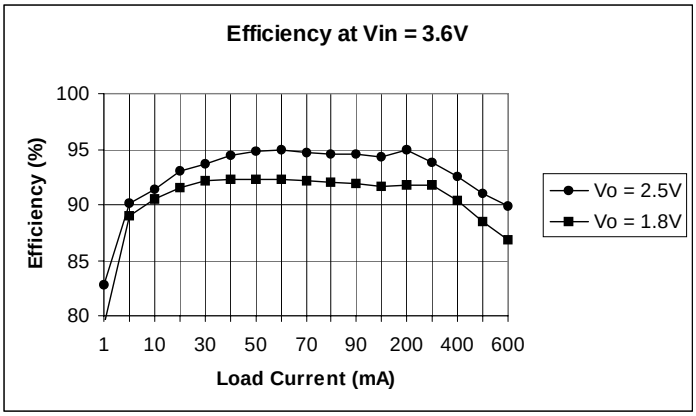
Ceramic capacitors are recommended for input capacitors because of their low ESR and high ripple current capabilities. In addition, it is advised that the input capacitor be placed as close to the input pin of the IC as possible.

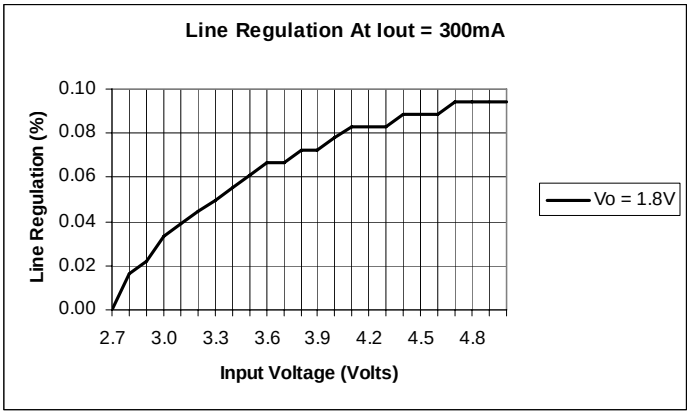
Layout Considerations

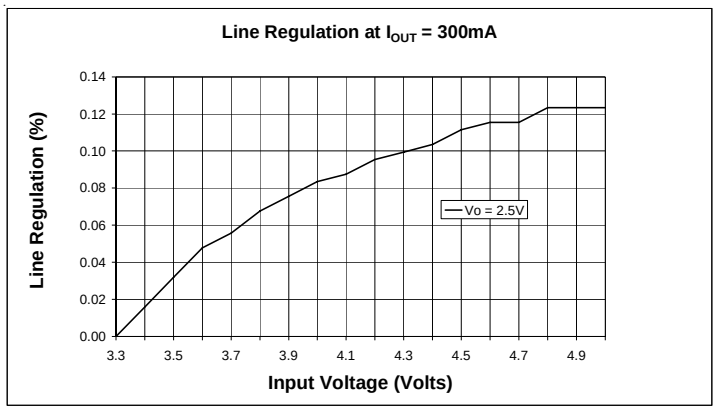
PCB layout is of utmost importance because the switching frequency is 750kHz with peak currents over 1A. A careful layout will avoid potential stability and EMI problems. Traces should be as wide and as short as possible. Keep the input capacitor as close to the package as possible. This will help minimize large loop areas. Keep the power ground and analog ground separated and tie the two together at one common point. Notice the top copper Gerber plot (see Page 8), pin 3 and pin 10 are tied together under the package. Be aware of the high current paths and avoid tying signal grounds to the high power grounds where the signal paths might experience large fluctuations in voltages as high currents pass though copper traces.

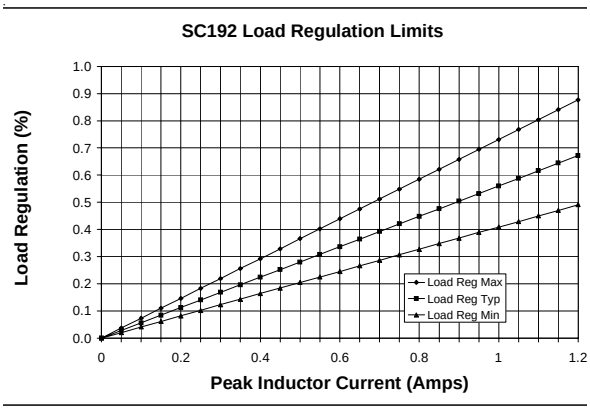


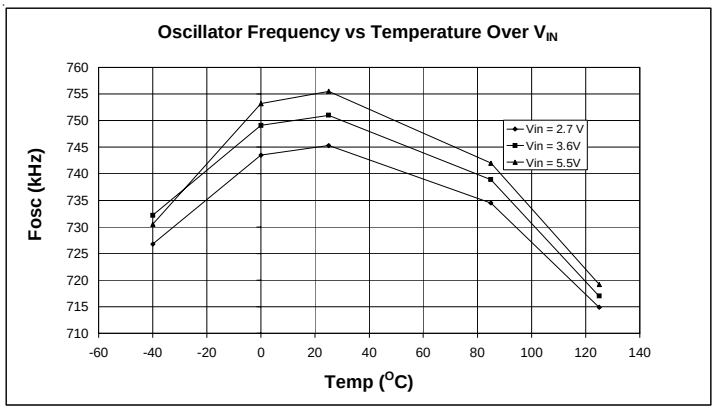


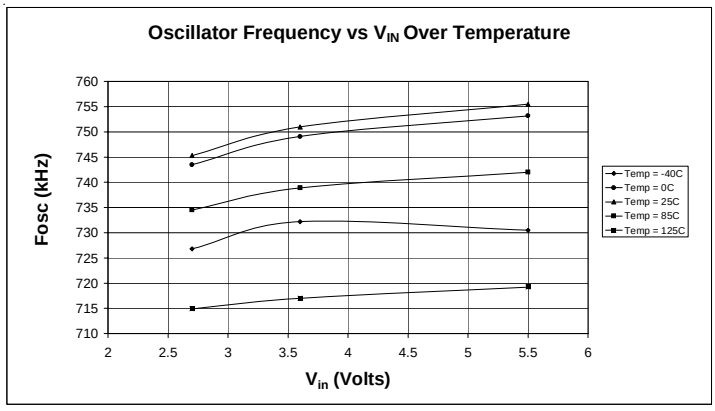


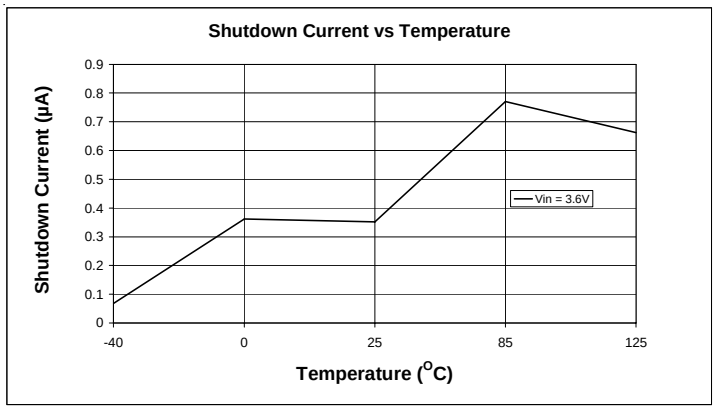




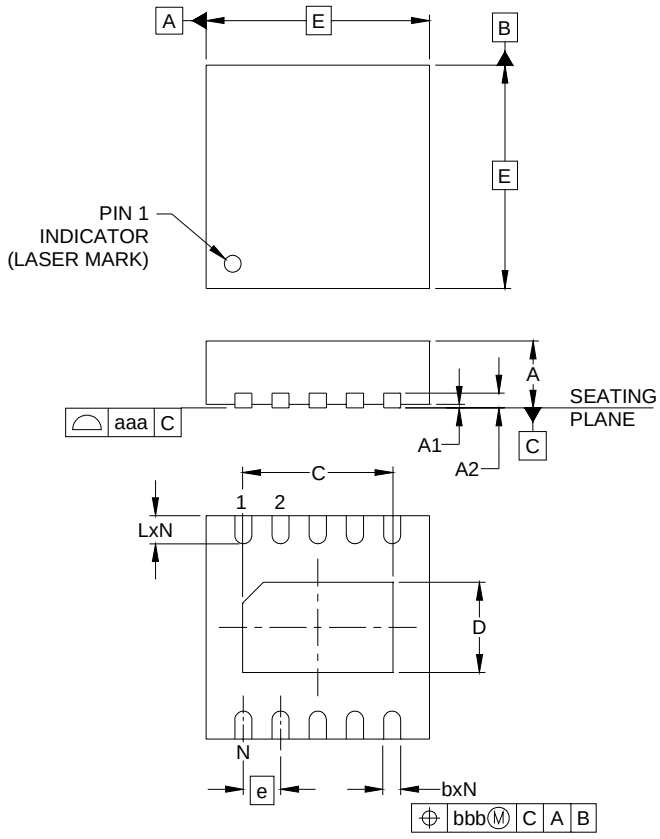








Outline Drawing - MLPD-10, 3 x 3



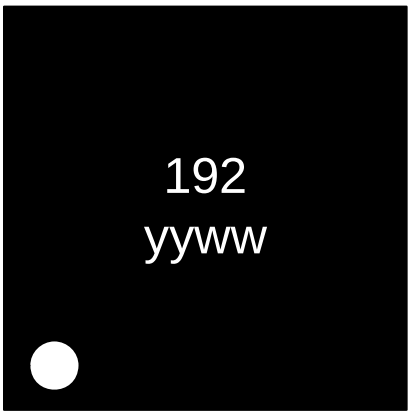
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.009	.011	0.18	0.23	0.30
C	.074	.079	.083	1.87	2.02	2.12
D	.042	.048	.052	1.06	1.21	1.31
E	.114	.118	.122	2.90	3.00	3.10
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	10			10		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Marking Information

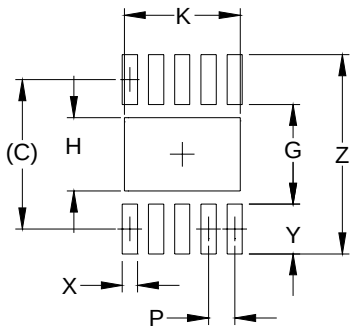
Top Marking



yy = two-digit year of manufacture
ww = two-digit week of manufacture

POWER MANAGEMENT

Land Pattern - MLPD-10, 3 x 3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.112)	(2.85)
G	.075	1.90
H	.055	1.40
K	.087	2.20
P	.020	0.50
X	.012	0.30
Y	.037	0.95
Z	.150	3.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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