SC195F

3.5MHz, 500mA Synchronous Step Down DC-DC Regulator

POWER MANAGEMENT

Features

- Input Voltage — 2.9V to 5.5V
- Output Voltage — 0.8V to 3.3V
- Output current capability — 500mA
- Efficiency up to 94%
- 15 Programmable output voltages
- Fast transient response
- Oscillator frequency — 3.5MHz
- 100% duty cycle capability
- Quiescent current — 4.8 mA typ
- Shutdown Current — 0.1µA typ
- Internal soft-start
- Over-voltage protection
- Current limit and short circuit protection
- Over-temperature protection
- Input under-voltage lockout
- Floating control pin protection
- MLPQ-UT8 1.5 x 1.5 x 0.6 (mm) package
- Pb free, halogen free, and RoHS/WEEE compliant

Applications

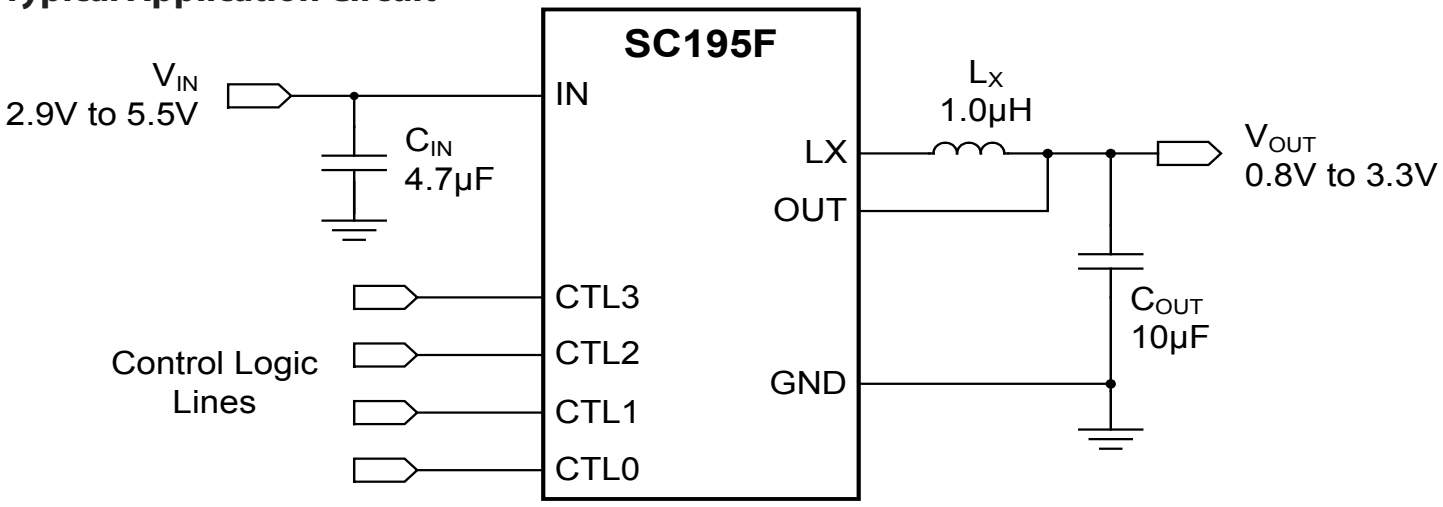
- Smart phones and cellular phones
- MP3/Personal media players
- Personal navigation devices
- Digital cameras
- Single Li-ion cell or 3 NiMH/NiCd cell devices
- Devices with 3.3V or 5V internal power rails

Description

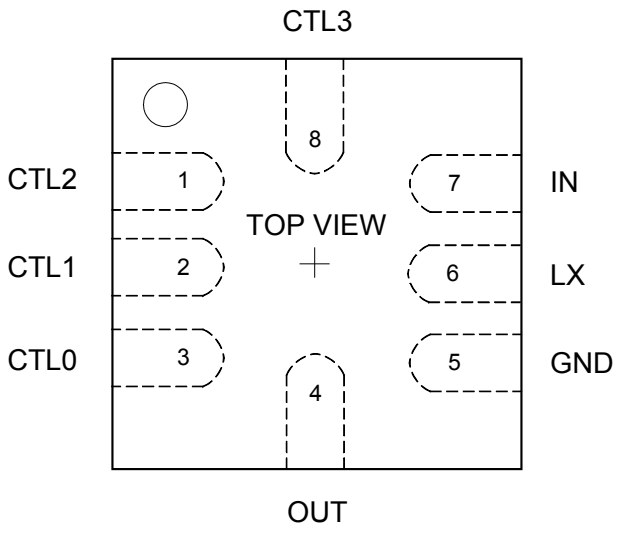
The SC195F is a high efficiency, 500mA step down regulator designed to operate with an input voltage range of 2.9V to 5.5 V. The input voltage range makes it ideal for battery operated applications with space limitations. The SC195F operates at a fixed 3.5MHz switching frequency in normal PWM (Pulse-Width Modulation) mode. The SC195F also includes fifteen programmable output voltage settings that can be selected using the four control pins, eliminating the need for external feedback resistors. The output voltage can be fixed to a single setting or dynamically switched between different levels. Pulling all four control pins low disables the output.

The SC195F provides several protection features to safeguard the device under stressed conditions. These include short circuit protection, over-temperature protection, input under-voltage lockout, and soft-start to control in-rush current. These features, coupled with the small 1.5 x 1.5 x 0.6 (mm) package make the SC195F a versatile device ideal for step-down regulation in products needing high efficiency and a small PCB footprint.

Typical Application Circuit



Pin Configuration



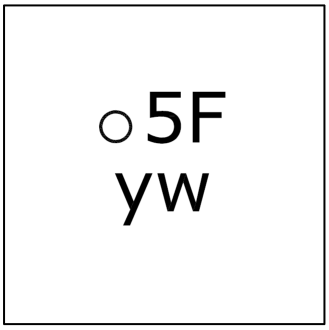
MLPQ-UT8; 1.5 x 1.5, 8 LEAD
θ_{JA} = 116°C/W

Ordering Information

Device	Package
SC195FULTRT[1][2]	MLPQ-UT8 1.5 x 1.5
SC195FEVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free packaging only. Device is WEEE and RoHS compliant and halogen-free.

Marking Information



5F=SC195F
yw=Date Code

Table 1 – Output Voltage Settings

CTL3	CTL2	CTL1	CTL0	Vout
0	0	0	0	Off
0	0	0	1	0.80
0	0	1	0	1.00
0	0	1	1	1.20
0	1	0	0	1.40
0	1	0	1	1.50
0	1	1	0	1.60
0	1	1	1	1.80
1	0	0	0	2.30
1	0	0	1	2.35
1	0	1	0	2.00
1	0	1	1	2.40
1	1	0	0	2.45
1	1	0	1	2.80
1	1	1	0	3.00
1	1	1	1	3.30

Absolute Maximum Ratings

IN (V) ..... -0.3 to +6.0
LX Voltage (V) ..... -1.0 to V_{IN} +0.5
Other Pins (V) ..... -0.3 to V_{IN} + 0.3
Output Short Circuit to GND ..... Continuous
ESD Protection Level[1] (kV) 2.5

Recommended Operating Conditions

Input Voltage Range (V) ..... +2.9 to +5.5

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) 116
Junction Temperature Range (°C) ..... -40 to +150
Storage Temperature Range (°C) ..... -65 to +150

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB per JESD51 standards.

Electrical Characteristics

Unless otherwise specified: V_{IN}= 3.6V, C_{IN}=4.7µF, C_{OUT}=10µF, L_X=1µH, V_{OUT}=2.0V, $T_{J(MAX)}$=125°C, T_A= -40 to +85 °C. Typical values are T_A=+25 °C

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Voltage Range	V_{OUT}		0.8		3.3 [1]	V
Output Voltage Tolerance	V_{OUT_TOL}	I_{OUT} = 200mA	-2.0		2.0	%
Line Regulation	$\Delta V_{LINEREG}$	2.9 ≤ V_{IN} ≤ 5.5V, I_{OUT} = 200mA		0.3		%/V
Load Regulation	$\Delta V_{LOADREG}$	200mA ≤ I_{OUT} ≤ 500mA		-1		%/A
Output Current Capability	I_{OUT}		500			mA
Current Limit Threshold	I_{LIMIT}		800		1300	mA
Foldback Current Limit	I_{FB_LIM}	I_{LOAD} > I_{LIMIT}		150		mA
Under-Voltage Lockout	V_{UVLO}	Rising V_{IN}			2.9	V
		Hysteresis		200		mV
Quiescent Current	I_Q	I_{OUT} = 0mA		4.8		mA
Shutdown Current	I_{SD}	$V_{CTL\ 0-3}$ = 0V		0.1	1.0	µA
LX Leakage Current	I_{LX}	Into LX pin		0.1	1.0	µA
High Side Switch Resistance[2]	R_{DSON_P}	I_{OUT}= 100mA		250		mΩ
Low Side Switch Resistance[3]	R_{DSON_N}	I_{OUT}= 100mA		350		
Switching Frequency	f_{SW}		2.8	3.5	4.2	MHz

Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft-Start	t_{SS}	V_{OUT} = 90% of final value (4)		350	500	µs
Thermal Shutdown	T_{OT}	Rising temperature		160		°C
Thermal Shutdown Hysteresis	T_{HYST}			20		°C
Logic Inputs - CTL0, CTL1, CTL2, and CTL3						
Input High Voltage	V_{IH}		1.6			V
Input Low Voltage	V_{IL}				0.4	V
Input High Current	I_{IH}	$V_{CTL\ 0\text{-}3}$= V_{IN}	-2.0		5.0	µA
Input Low Current	I_{IL}	$V_{CTL\ 0\text{-}3}$= GND	-2.0		2.0	µA

Notes

(1) Maximum output voltage is limited to VIN if the input is less than 3.3V.

(2) Measured from IN to LX.

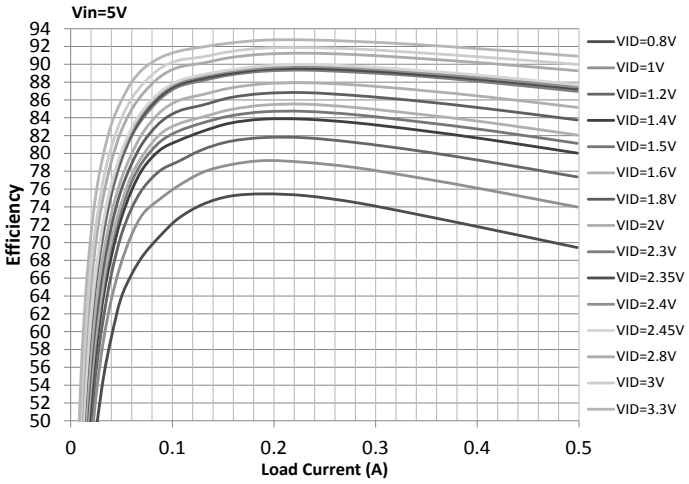
(3) Measured from LX to GND.

(4) Soft start time depends on the load and output capacitance, see Soft Start section.

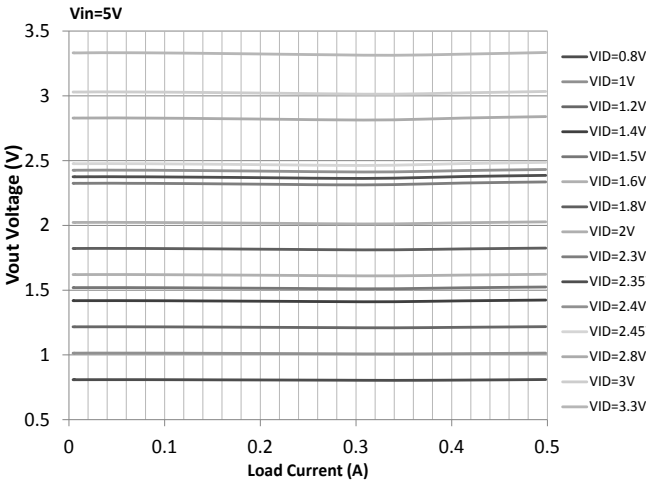
Typical Characteristics

C_{IN} = 4.7µF, C_{OUT} = 10µF, L_X = 1µH, T_A = 25°C unless otherwise noted.

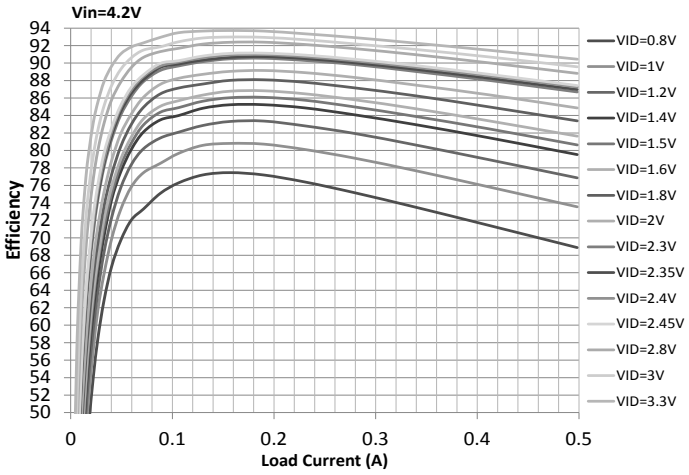
Efficiency vs. I_{OUT} Vin=5V



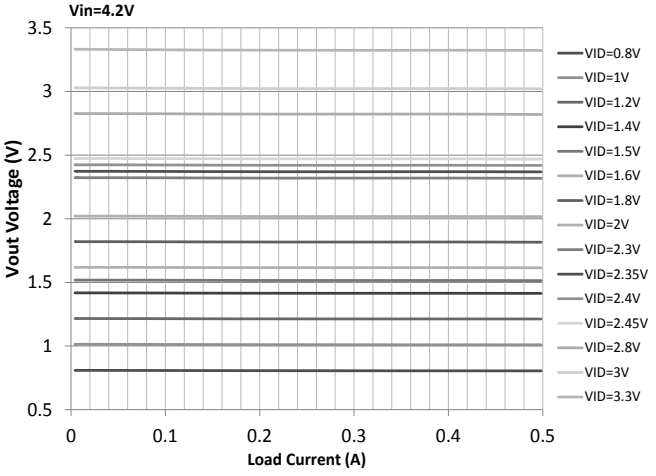
Regulation vs. I_{OUT} Vin=5V



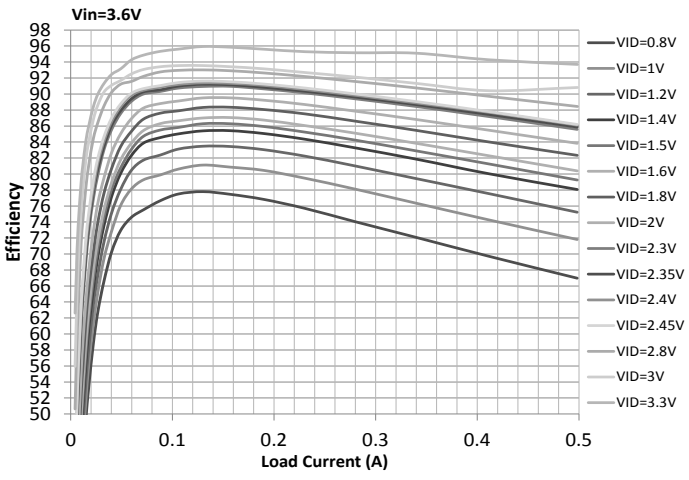
Efficiency vs. I_{OUT} Vin=4.2V



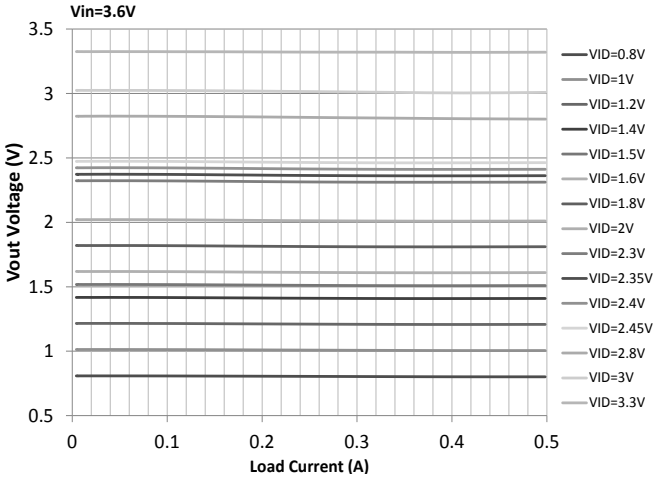
Regulation vs. I_{OUT} Vin=4.2V



Efficiency vs. I_{OUT} Vin=3.6V

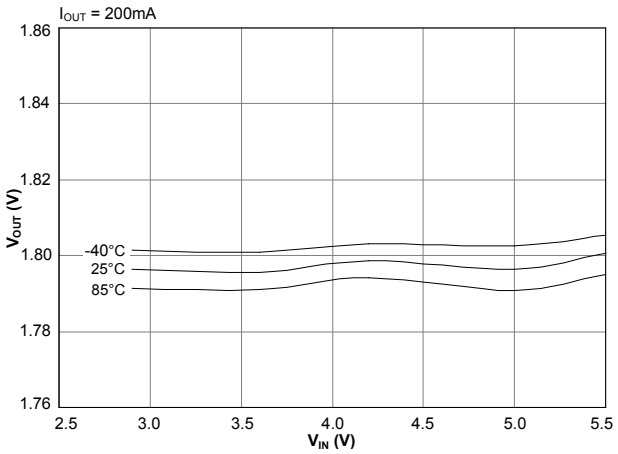


Regulation vs. I_{OUT} Vin=3.6V

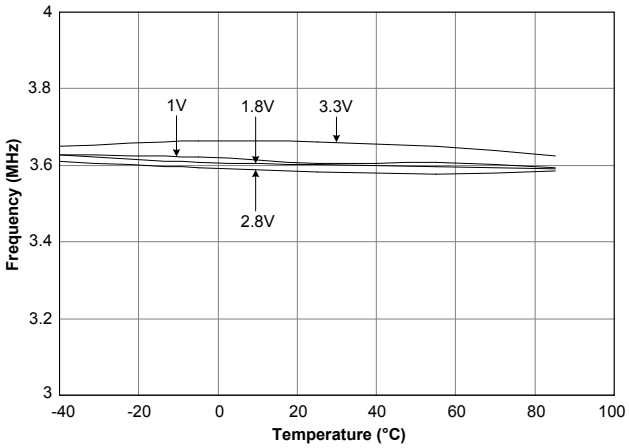


Typical Characteristics (continued)

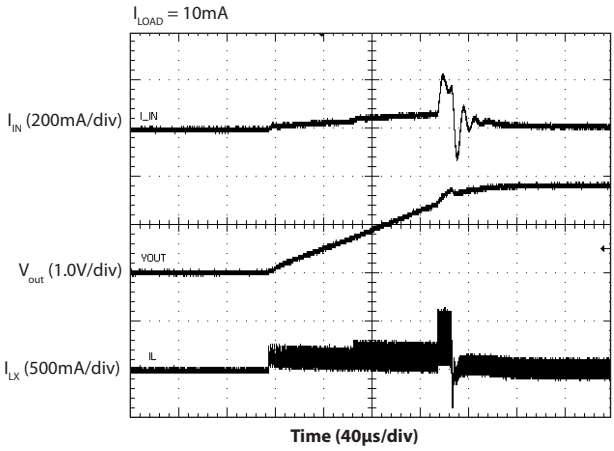
Line Regulation (V_{OUT}=1.8V)



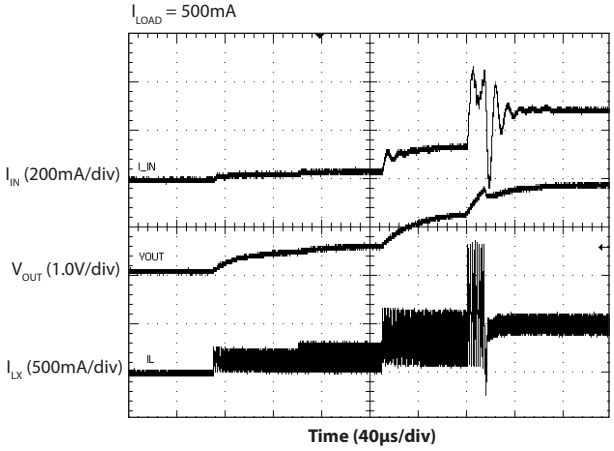
Frequency vs. Temperature



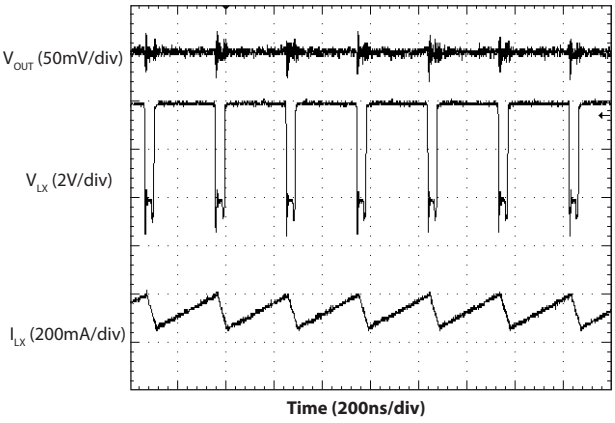
Light Load Soft-start



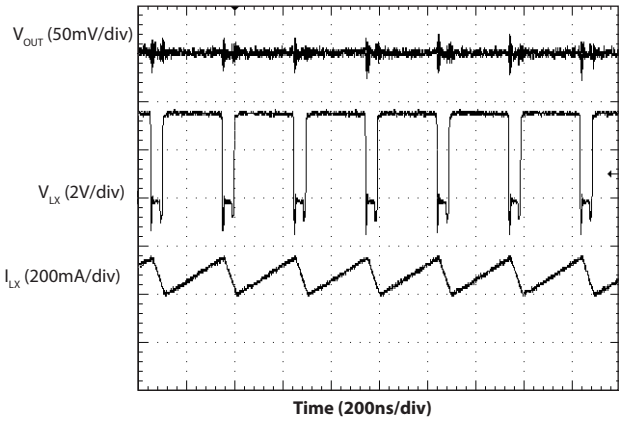
Heavy Load Soft-start



Heavy Load Switching — V_{OUT} = 3.3V

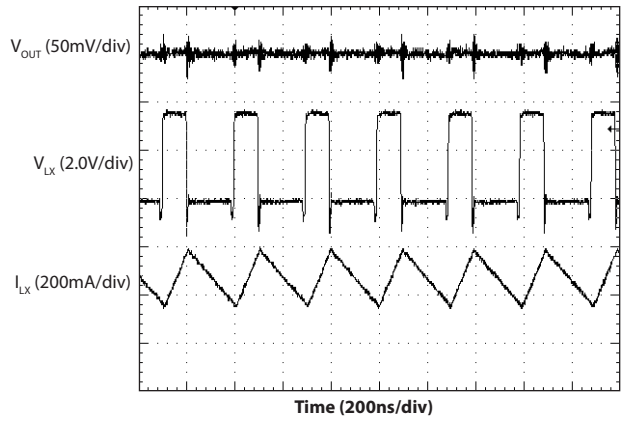


Heavy Load Switching — V_{OUT} = 2.8V

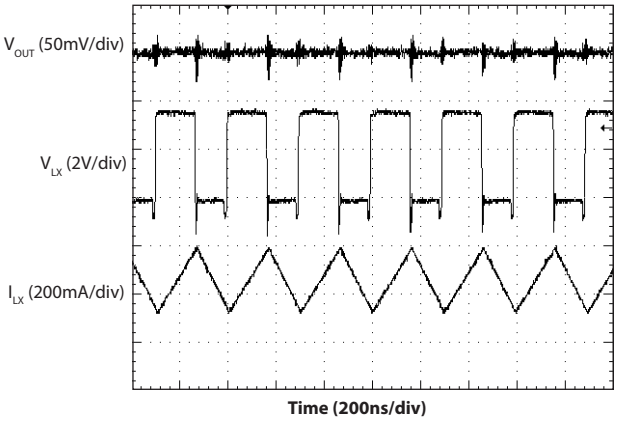


Typical Characteristics (continued)

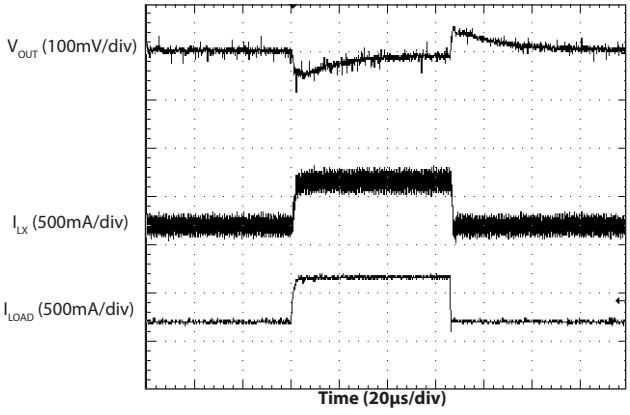
Heavy Load Switching — V_{OUT} = 1.0V



Heavy Load Switching — V_{OUT} = 1.8V

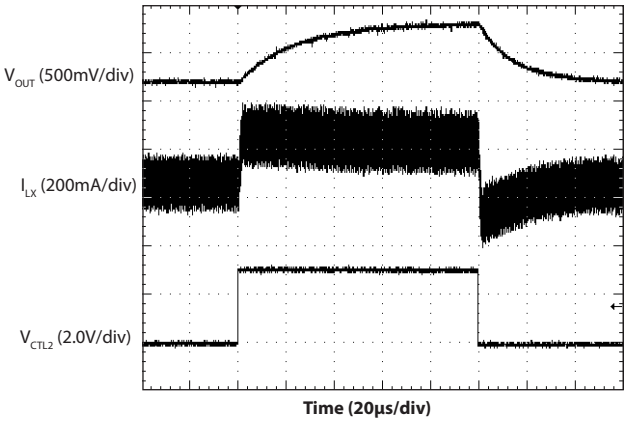


Load Transient Response — 200 to 500mA



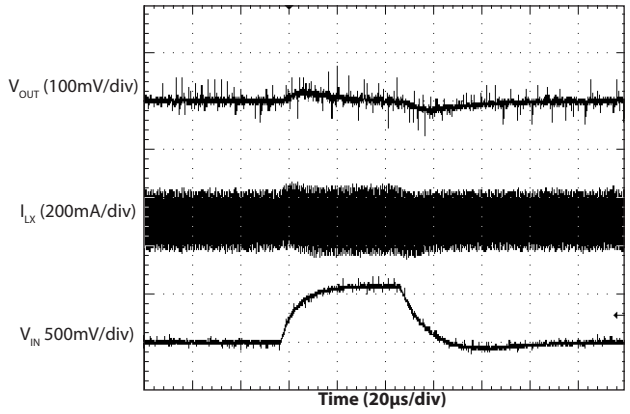
VID Transient Response — PWM

1.2V to 1.8V transition

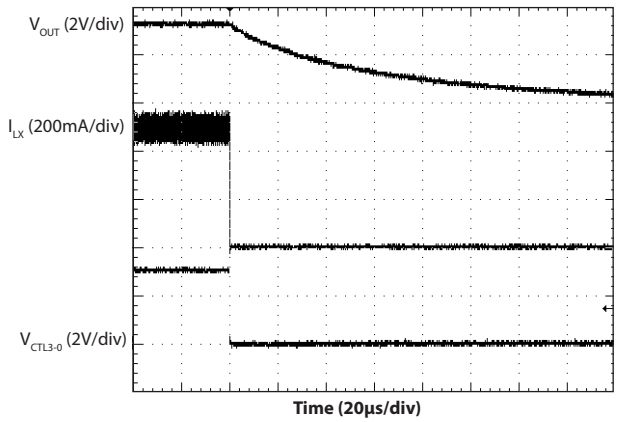


Line Transient Response — PWM

3.5V to 4.0V transition on V_{IN}



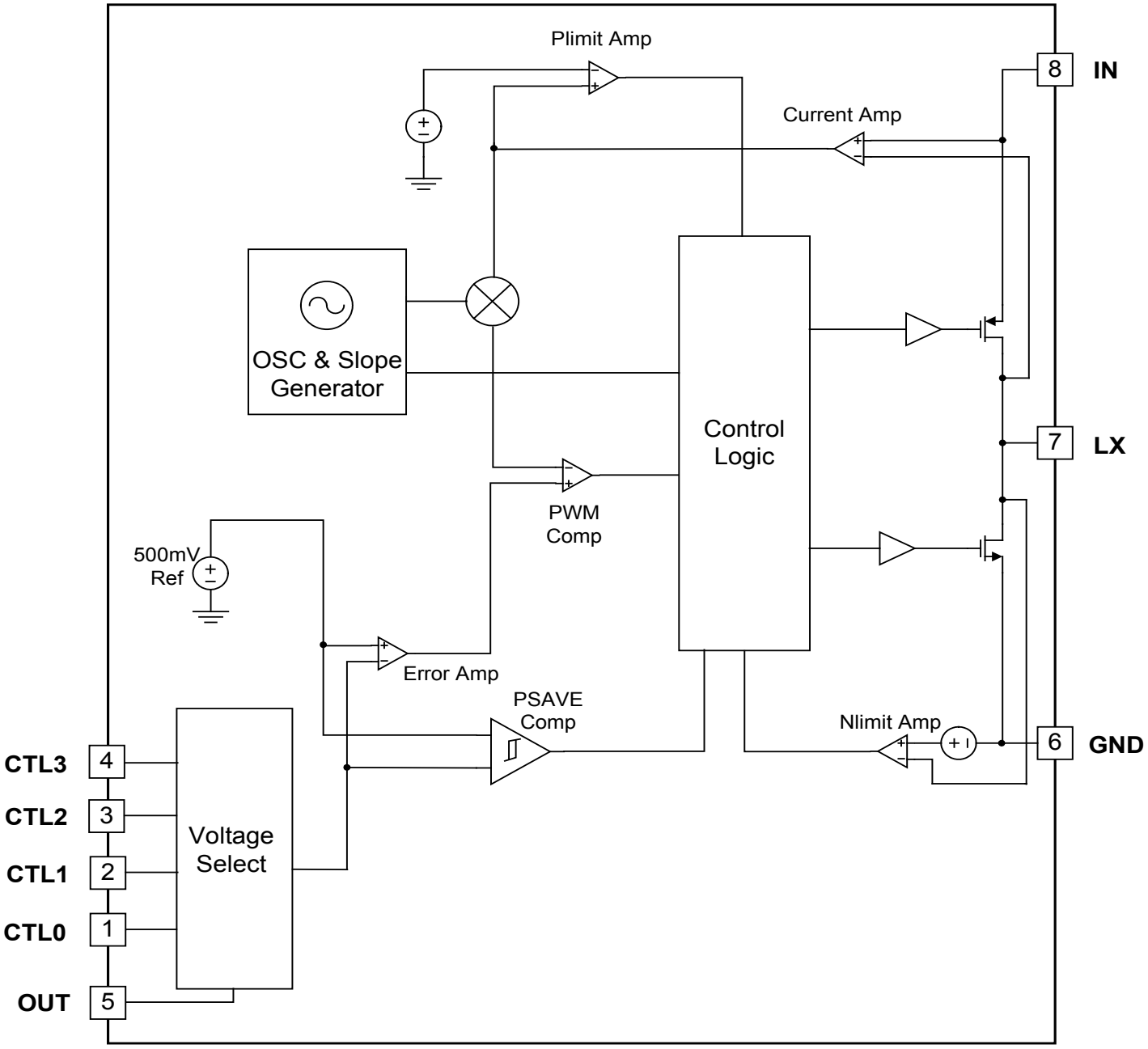
Shutdown Transient Response



Pin Descriptions

Pin	Pin Name	Pin Function
1	CTL2	Control bit 2 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL2 is pulled above the logic high threshold.
2	CTL1	Control bit 1 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL1 is pulled above the logic high threshold.
3	CTL0	Control bit 0 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL0 is pulled above the logic high threshold.
4	OUT	Output voltage sense pin — output voltage regulation point (connection node of inductor and output capacitor).
5	GND	Ground reference and power ground for the SC195F.
6	LX	Switching output — connect an inductor between this pin and the load to filter the pulsed output current.
7	IN	Input power supply pin — connect a bypass capacitor from this pin to GND.
8	CTL3	Control bit 3 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor (> 1MΩ) in place at reset that is removed when CTL3 is pulled above the logic high threshold.

Block Diagram



Applications Information

General Description

The SC195F is a synchronous step-down Pulse Width Modulated (PWM) DC-DC regulator utilizing a 3.5MHz fixed-frequency voltage mode architecture. The device is designed to operate in fixed-frequency PWM mode at all load conditions. The device requires only two capacitors and a single inductor to be implemented in most systems. The switching frequency has been chosen to minimize the size of the inductor and capacitors while maintaining high efficiency. The output voltage is programmable, eliminating the need for external programming resistors. Loop compensation is also internal, eliminating the need for external components to control stability.

Programmable Output Voltage

The SC195F has 15 fixed output voltage levels which can be individually selected by programming the CTL control pins (CTL3-0 — see Table 1 on page 2 for settings). The device is disabled whenever all four CTL pins are pulled low and enabled whenever at least one of the CTL pins is pulled high. This configuration eliminates the need for a dedicated enable pin. Each CTL pin is internally pulled down via 1MΩ if V_{IN} is below 1.5V or if the voltage on the control pin is below the input high voltage. This ensures that the output is disabled when power is applied if there are no inputs to the CTL pins. Each weak pull-down is disabled whenever its pin is pulled high and remains disabled until all CTL pins are pulled low.

The output voltage can be set using different approaches. If a static output voltage is required, the CTL pins can be tied to either IN or GND to set the desired voltage whenever power is applied at IN. If enable control is required, each CTL pin can be tied to either GND or to a microprocessor I/O line to create the desired control code whenever the control signal is forced high. This approach is equivalent to using the CTL pins collectively as a single enable pin. A third option is to connect each of the four CTL pins to individual microprocessor I/O lines. Any of the 15 output voltages can be programmed using this approach. If only two output voltages are needed, the CTL pins can be combined in a way that will reduce the number of I/O lines to 1, 2, or 3, depending on the control code for each desired voltage. Other CTL pins could be hard wired to GND or IN. This option allows dynamic voltage adjustment for systems that reduce the supply voltage at low power state. Note that applying all zeros to the CTL pins when changing the output voltages will temporarily disable the device, so it is important to avoid this combination when dynamically changing levels.

Adjustable Output Voltage Selection

If an output voltage other than one of the 15 programmable settings is needed, an external resistor divider network can be added to the SC195F to adjust the output voltage setting. This network scales the output based on the resistor ratio and the programmed output setting. The resistor values can be determined using the equation

$$V_{OUT} = V_{SET} \times \left[\frac{R_{FB1} + R_{FB2}}{R_{FB2}} \right] + I_{LEAK} \times R_{FB1}$$

where V_{OUT} is the desired output voltage, V_{SET} is the voltage setting selected by the CTL pins, R_{FB1} is the resistor between the output capacitor and the OUT pin, R_{FB2} is the resistor between the OUT pin and ground, and I_{LEAK} is the leakage current into the OUT pin during normal operation. The current into the OUT pin is typically 1µA, so the last term of the equation can be neglected if the current through R_{FB2} is much larger than 1µA. Selecting a resistor value of 10kΩ or lower will simplify the design. If I_{LEAK} is neglected and R_{FB2} is fixed, R_{FB1} can be determined using the equation

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - V_{SET}}{V_{SET}}$$

Inserting resistance in the feedback loop will adversely affect the system's transient performance if feed-forward capacitance is not included in the circuit. The circuit in Figure 1 illustrates how the resistor divider and feed-forward capacitor can be added to the SC195F schematic. The value of feed-forward capacitance needed can be determined using the equation

$$C_{FF} = 4 \times 10^{-6} \times \frac{V_{SET}(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - V_{SET})(V_{SET} - 0.5)}$$

Applications Information (continued)

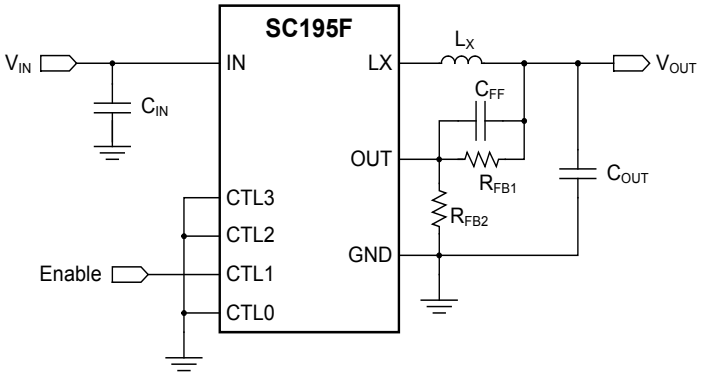


Figure 1 — Application Circuit with External Resistors

To simplify the design, it is recommended to program the output setting to 1.0V, use resistor values smaller than 10kΩ, and include a feed-forward capacitance calculated with the equation above. If the output voltage is set to 1.0V, the previous equation reduces to

$$C_{FF} = 8 \times 10^{-6} \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - 1)}$$

Example:

An output voltage of 1.3V is desired, but this is not a programmable option. What external component values for Figure 1 are needed?

Solution: To keep the circuit simple, set R_{FB2} to 10kΩ so current into the OUT pin can be neglected and set the CTL3-0 pins to 0010 (1.0V setting). The necessary component values for this situation are

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - V_{SET}}{V_{SET}} = 3k\Omega$$

$$C_{FF} = 8 \times 10^{-6} \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}(V_{OUT} - 1)} = 5.69nF$$

PWM and 100% Duty Cycle Operation

In order to start up from pre-charged output voltage, SC195F does not allow inductor current to go negative in soft start stage, refer to the soft start waveforms in the Typical Characteristics page. When the output voltage exceeds 90% of the set point, determined by the CTLx combinations, the device will enter fixed 3.5MHz PWM mode operation. An internal synchronous NMOS rectifier turns on complementary to the top PMOSFET.

The duty cycle (percentage of time PMOS is active) increases as V_{IN} decreases to maintain output voltage regulation. As the input voltage approaches the programmed output voltage, the duty cycle approaches 100% (PMOS always on) and the device enters a pass-through mode until the input voltage increases or the load decreases enough to allow PWM switching to resume.

Protection Features

The SC195F provides the following protection features:

- Current Limited Soft-Start Operation
- Over-Voltage Protection
- Current Limit
- Thermal Shutdown
- Input Voltage Under-Voltage Lockout

Soft-Start with Current Limit

The soft-start sequence is activated after a CTL code transition from an all zeros code to a non-zero code enables the start up process. From the beginning of a start-up process, the internal reference start-up takes typically 50µs, then PMOS current limit is stepped through four levels: 25%, 40%, 60%, and 100%. Each step is maintained for typically 75µs. A complete 4 steps start-up period could take 350µs. Before V_{OUT} reaches 90%, the inductor current is not allowed to go negative. The inductor current is confined between different current limit levels, 25%, 40%, 60%, or 100% to zero.

As V_{OUT} reaches 90% of the target value, the device will transition into a fixed 3.5MHz operation allowing inductor current in both directions.

Due to current limit operation, if the load is heavy or the output capacitor is large, the soft start process may experience all 4 current limit steps before reaching 90% target voltage. This will make the soft start time long. If the load is light and output capacitor is small, the device may only need the first current limit step, reaching 90% of target, and transition into PWM operation. This makes the soft start time shorter.

Applications Information (continued)

Over-Voltage Protection

Over-voltage protection ensures the output voltage does not rise to a level that could damage its load. When V_{OUT} exceeds the regulation voltage by 15%, the PWM drive is disabled. Switching does not resume until V_{OUT} has fallen below the regulation voltage by 2%.

Current Limit

The SC195F switching stage is protected by a current limit function. If the output load exceeds the PMOS current limit for 32 consecutive switching cycles, the device enters fold-back current limit mode and the output current is limited to approximately 150mA. Under these conditions, the output voltage will be the product of I_{FB-LIM} and the load resistance. The load must fall below I_{FB-LIM} for the device to exit fold-back current limit mode. This function makes the device capable of sustaining an indefinite short circuit on its output under fault conditions.

Thermal Shutdown

The SC195F has a thermal shutdown feature to protect the device if the junction temperature exceeds 160°C. During thermal shutdown, the PMOS and NMOS switches are both disabled, tri-stating the LX output. When the junction temperature drops by the hysteresis value (20°C), the device goes through the soft-start process and resumes normal operation.

Input Voltage Under-Voltage Lockout

Under-Voltage Lockout (UVLO) activates when the input power supply voltage drops below the UVLO threshold. This prevents the device from entering an ambiguous state in which regulation cannot be maintained. Hysteresis of approximately 200mV is included to prevent chattering near the threshold.

External Components

Inductor Selection

The SC195F is designed to operate with a suggested 1µH inductor between the LX pin and the OUT pin.

The SC195F converter has internal loop compensation. The compensation is designed to work with a specific single-pole output filter corner frequency defined by the equation

$$f_C = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

where L = 1µH and C_{OUT} = 10µF.

When selecting output filter components, the LC product should not vary over a wide range. Selection of smaller inductor and capacitor values will move the corner frequency, potentially impacting system stability.

It is also important to consider the change in inductance with DC bias current when choosing an inductor. The inductor saturation current is specified as the current at which the inductance drops a specific percentage from the nominal value (approximately 30%). Except for short-circuit or other fault conditions, the peak current must always be less than the saturation current specified by the manufacturer. The peak current is the maximum load current plus one half of the inductor ripple current at the maximum input voltage. Load and/or line transients can cause the peak current to exceed this level for short durations. Maintaining the peak current below the inductor saturation specification keeps the inductor ripple current and the output voltage ripple at acceptable levels. Manufacturers often provide graphs of actual inductance and saturation characteristics versus applied inductor current. The saturation characteristics of the inductor can vary significantly with core temperature. Core and ambient temperatures should be considered when examining the core saturation characteristics.

When the inductor value has been determined, the DC resistance (DCR) must be examined. Efficiency can be optimized by lowering the inductor's DCR as much as possible. Low DCR in an inductor requires either more surface area for the increased wire diameter or fewer turns to reduce the length of the copper winding. Fewer turns requires an inductor core with a larger cross-sectional area in order to maintain the same saturation characteristics. The inductor size must always be considered when examining the inductor DCR to determine the best compromise between DCR and component area on a PCB. Note that the ripple component of the inductor is a small percent-

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age of the DC load. AC losses in the inductor core and winding do not contribute significantly to the total losses.

Magnetic fields associated with the output inductor can interfere with nearby circuitry. This can be minimized by the use of low-noise shielded inductors which use the minimum gap possible to limit the distance that magnetic fields can radiate from the inductor. Shielded inductors, however, typically have a higher DCR and are, therefore, less efficient than a similar sized non-shielded inductor.

Final inductor selection depends on various design considerations such as efficiency, EMI, size, and cost. Table 2 lists the manufacturers of recommended inductor options. The inductors with larger packages tend to provide better overall efficiency, while the smaller package inductors provide decent efficiency with reduced footprint or height. The saturation current ratings and DC characteristics are also shown.

Table 2 — Recommended Inductors

Manufacturer Part Number	L (µH)	DCR (Ω)	Saturation Current (mA)	L at 400mA (µH)	Dimensions LxWxH (mm)
Murata LQM21PN1R0MC0	1.0±20%	0.19	800	0.75	2.0x1.25x0.55
Murata LQM2HPN1R0MJ0	1.0±20%	0.09	1500	0.95	2.5x2.0x1.1
Murata LQM31PN1R0M00	1.0±20%	0.12	1200	0.95	3.2x1.6x0.85
Taiyo Yuden CKP25201R0M-T	1.0±20%	0.08	800	0.88	2.5x2.0x1.0
Toko MDT2012-CR1R0N	1.0±30%	0.08	1350	1.00	2.0x1.25x1.0
FDK MIPSZ2012D1R0	1.0±30%	0.09	1100	1.00	2.0x1.25x1.0
FDK MIPSU2520D1R0	1.0±30%	0.08	1300	0.78	2.5x2.0x0.5
FDK MIPSA2520D1R0	1.3±30%	0.09	1200	1.20	2.5x2.0x1.2
Taiyo Yuden BRC1608T1R0M	1.0±20%	0.18	850	0.90	1.6x0.8x0.8

C_{OUT} Selection

The internal voltage loop compensation in the SC195F limits the minimum output capacitor value to 10µF. This is due to its influence on the the loop crossover frequency, phase margin, and gain margin. Increasing the output capacitor above this minimum value will reduce the crossover frequency and provide greater phase margin.

The output capacitor determines the output voltage ripple and contributes load current during large step load transitions. A capacitor between 10µF and 22µF will usually be adequate in stabilizing the output during large load transitions.

Capacitors with X7R or X5R ceramic dielectric are recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

In addition to ensuring stability, the output capacitor serves other important functions. This capacitor determines the output voltage ripple — as capacitance increases, ripple voltage decreases. It also supplies current during a large load step for a few switching cycles until the control loop responds (typically 3 switching cycles). Once the loop responds, regulation is restored and the desired output is reached. During the period prior to PWM operation resuming, the relationship between output voltage and output capacitance can be approximated using the equation

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f}$$

This equation can be used to approximate the minimum output capacitance needed to ensure voltage does not droop below an acceptable level. For example, a load step from 50mA to 400mA requiring droop less than 50mV would require the minimum output capacitance to be

$$C_{OUT} = \frac{3 \times 0.4}{0.05 \times 4 \times 10^{6}} = 6.0\mu F$$

In this example, using a standard 10µF capacitor would be adequate to keep voltage droop less than the desired

Applications Information (continued)

limit. Note that if the voltage droop limit were decreased from 50mV to 25mV, the output capacitance would need to be increased to at least 12µF (twice as much capacitance for half the droop). Capacitance will decrease from the nominal value when a ceramic capacitor is biased with a DC current, so it is important to select a capacitor whose value exceeds the necessary capacitance value at the programmed output voltage. Check the manufacturer's capacitance vs. DC voltage graphs when selecting an output capacitor to ensure the capacitance will be adequate.

Table 3 lists the manufacturers of recommended output capacitor options.

Table 3 — Recommended Output Capacitors

Manufacturer Part Nunber	Value (µF)	Type	Rated Voltage (VDC)	Dimensions LxWxH (mm) Case Size
Murata GRM188R60J106ME47D	10±20%	X5R	6.3	1.6x0.8x0.8 0603
Murata GRM21BR60J106K	10±10%	X5R	6.3	2.0x1.25x1.25 0805
Taiyo Yuden JMK107BJ106MA-T	10±20%	X5R	6.3	1.6x0.8x0.8 0603
TDK C1608X5R0J106MT	10±20%	X5R	6.3	1.6x0.8x0.8 0603

C_{IN} Selection

The SC195F input current will appear as a pulse DC current. To prevent large input voltage ripple, a low ESR ceramic capacitor is required. A minimum value of 4.7µF should be used. It is important to consider the DC voltage coefficient characteristics when determining the actual required value. For example, a 10µF, 6.3V, X5R ceramic capacitor with 5V DC applied may exhibit a capacitance as low as 4.5µF. The value of required input capacitance is estimated by determining the acceptable input ripple voltage and calculating the minimum value required for C_{IN} using the equation

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{\Delta V}{I_{OUT}}-ESR\right)f}$$

The input voltage ripple is at maximum level when the input voltage is twice the output voltage (50% duty cycle scenario).

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the PMOS switch. Low ESR/ESL X5R ceramic capacitors are recommended for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IN and GND pins of the SC195F. Table 4 lists the recommended input capacitor options from different manufacturers.

Table 4 — Recommended Input Capacitors

Manufacturer Part Nunber	Value (µF)	Type	Rated Voltage (VDC)	Dimensions LxWxH (mm) Case Size
Murata GRM188R60J475K	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603
Murata GRM188R60J106K	10±10%	X5R	6.3	1.6x0.8x0.8 0603
Taiyo Yuden JMK107BJ475KA	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603
TDK C1608X5R0J475KT	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603

PCB Layout Considerations

The layout diagram in Figure 2 shows a recommended PCB top-layer for the SC195F and supporting components. Specified layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following guidelines are recommended for designing a PCB layout:

1. C_{IN} should be placed as close to the IN and GND pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to minimize trace impedance. This will also minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the LX pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit. C_{OUT} and L_X should be connected as close as possible between the LX and GND pins, with a direct return to the GND.

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3. Use a ground plane referenced to the GND pin. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
4. Route the output voltage feedback/sense path away from the inductor and LX node to minimize noise and magnetic interference.
5. Minimize the resistance from the OUT and GND pins to the load. This will reduce errors in DC regulation due to voltage drops in the traces.

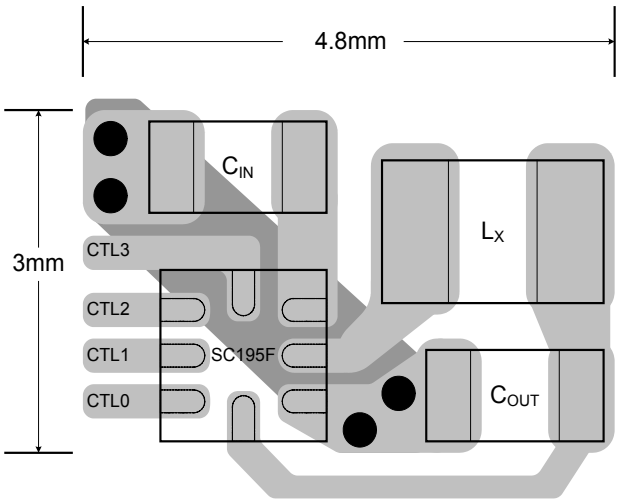
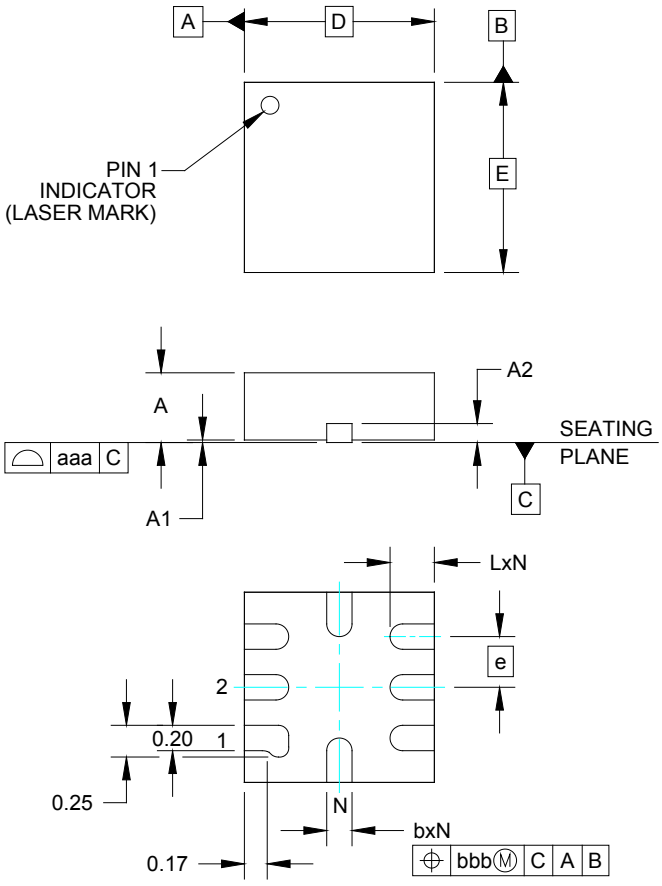


Figure 2 — Recommended PCB Layout

Outline Drawing — MLPQ-UT8

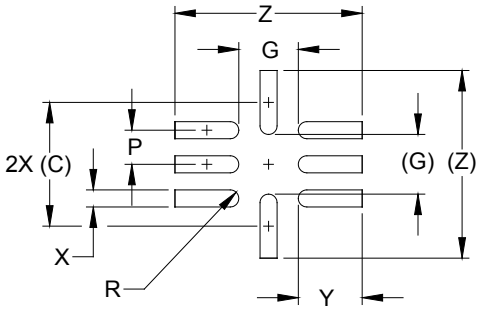


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.1524)	
b	.006	.008	.010	0.15	0.20	0.25
D		.059 BSC			1.50 BSC	
E		.059 BSC			1.50 BSC	
e		.016 BSC			0.40 BSC	
L	0.12	.014	0.16	0.30	0.35	0.40
N		8			8	
aaa		.004			0.10	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Suggested Land Pattern — MLPQ-UT8



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.057)	(1.45)
G	.028	0.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.030	0.75
Z	.087	2.20

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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