

POWER MANAGEMENT

Features

- Input Voltage — 2.9V to 5.5V
- Output Voltage — 0.8V to 3.3V
- Output current capability — 500mA
- Efficiency up to 94%
- 15 Programmable output voltages
- High light-load efficiency via automatic PSAVE mode
- Fast transient response
- Temperature range — -40 to +85°C
- Oscillator frequency — 3.5MHz
- 100% duty cycle capability
- Quiescent current — 38µA typ
- Shutdown Current — 0.1µA typ
- Internal soft-start
- Over-voltage protection
- Current limit and short circuit protection
- Over-temperature protection
- Under-voltage lockout
- Floating control pin protection
- MLPQ-UT8 1.5 x 1.5 x 0.6 (mm) package
- Pb free, Halogen free, and RoHS/WEEE compliant

Applications

- Smart phones and cellular phones
- MP3/Personal media players
- Personal navigation devices
- Digital cameras
- Single Li-ion cell or 3 NiMH/NiCd cell devices
- Devices with 3.3V or 5V internal power rails

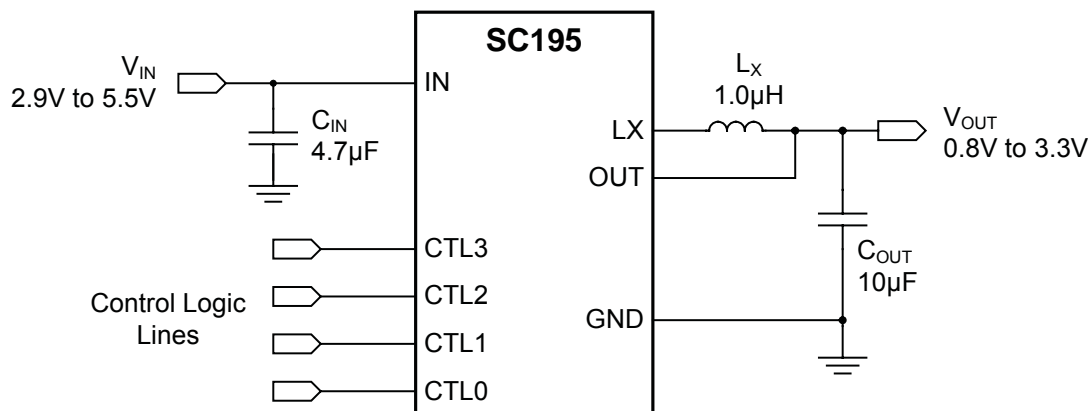
Description

The SC195 is a high efficiency, 500mA step down regulator designed to operate with an input voltage range of 2.9V to 5.5V. Four control logic pins are used to select the output voltage, eliminating the need for external feedback resistors. The control pins allow the output voltage to be set to a single level or controlled dynamically. Fifteen different output voltages can be selected. Pulling all four control pins low disables the output.

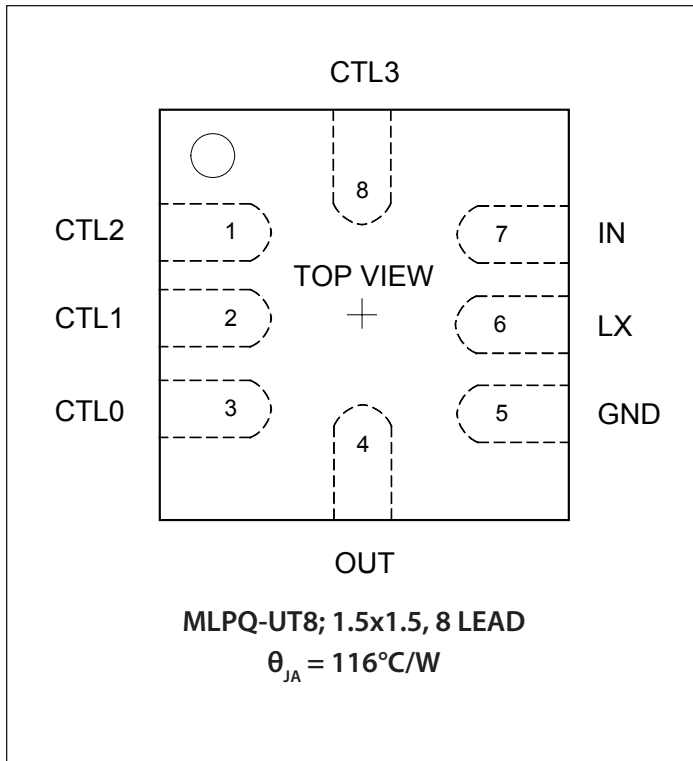
The SC195 operates at a fixed 3.5MHz switching frequency, minimizing the size and cost of external components. A power-save (PSAVE) mode is used to optimize efficiency at light loads for each output setting. Hysteresis is included to prevent chattering between PSAVE and normal pulse-width modulation (PWM) mode.

The SC195 provides short-circuit and thermal protection to safeguard the device under extreme operating conditions. Other features include internal soft-start circuitry, limiting in-rush current, and under-voltage lockout, preventing the device from malfunction when the input voltage drops below the rated minimum level. These features coupled with the tiny 1.5x1.5x0.6 (mm) package make the SC195 a versatile product well suited for portable applications.

Typical Application Circuit



Pin Configuration



Ordering Information

Device	Package
SC195ULTRT ⁽¹⁾⁽²⁾	MLPQ-UT8 1.5x1.5
SC195EVB	Evaluation Board

Notes:

- (1) Available in tape and reel only. A reel contains 3,000 devices.
- (2) Pb free, Halogen free, and RoHS/WEEE compliant

Marking Information

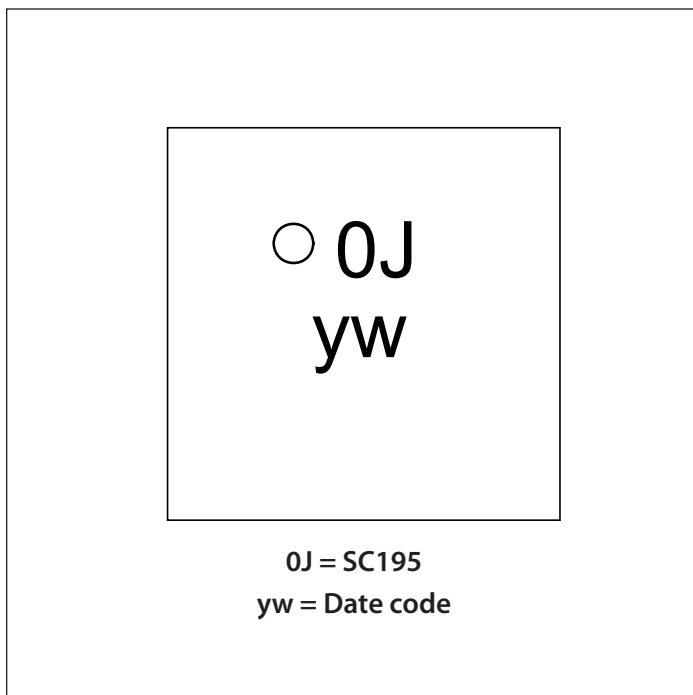


Table 1 – Output Voltage Settings

CTL3	CTL2	CTL1	CTL0	Vout
0	0	0	0	Shutdown
0	0	0	1	0.80
0	0	1	0	1.00
0	0	1	1	1.20
0	1	0	0	1.40
0	1	0	1	1.50
0	1	1	0	1.60
0	1	1	1	1.80
1	0	0	0	1.85
1	0	0	1	1.90
1	0	1	0	2.00
1	0	1	1	2.20
1	1	0	0	2.50
1	1	0	1	2.80
1	1	1	0	3.00
1	1	1	1	3.30

Absolute Maximum Ratings

IN (V)	-0.3 to +6.0
LX Voltage (V).....	-1.0 to $V_{IN} + 0.5$
Other Pins (V).....	-0.3 to $V_{IN} + 0.3$
Output Short Circuit to GND.....	Continuous
ESD Protection Level ⁽¹⁾ (kV)	2.5

Recommended Operating Conditions

Input Voltage Range (V).....	+2.9 to +5.5
Operating Temperature Range (°C)	-40 to +85

Thermal Information

Thermal Resistance, Junction to Ambient ⁽²⁾ (°C/W)....	116
Junction Temperature Range (°C)	-40 to +150
Storage Temperature Range (°C).....	-65 to +150

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:

- (1) Tested according to JEDEC standard JESD22-A114.
- (2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise specified: $V_{IN} = 3.6V$, $C_{IN} = 4.7\mu F$, $C_{OUT} = 10\mu F$, $L_X = 1\mu H$, $V_{OUT} = 1.8V$, $T_{J(MAX)} = 125^\circ C$, $T_A = -40$ to $+85^\circ C$. Typical values are $T_A = +25^\circ C$

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Voltage Range	V_{OUT}		0.8		3.3 ⁽¹⁾	V
Output Voltage Tolerance	V_{OUT_TOL}	$I_{OUT} = 200mA$	-2.0		2.0	%
		PSAVE mode		1.5		
Line Regulation	$\Delta V_{LINEREG}$	$2.9 \leq V_{IN} \leq 5.5V$, $I_{OUT} = 200mA$		0.3		%/V
Load Regulation	$\Delta V_{LOADREG}$	$200mA \leq I_{OUT} \leq 500mA$		-1		%/A
Average Output Current	I_{OUT}		500			mA
Current Limit Threshold	I_{LIMIT}		800		1300	mA
Foldback Current Limit	I_{FB_LIM}	$I_{LOAD} > I_{LIMIT}$		150		mA
Under-Voltage Lockout	V_{UVLO}	Rising V_{IN}			2.9	V
		Hysteresis		200		mV
Quiescent Current	I_Q	No switching, $I_{OUT} = 0mA$		38	60	μA
Shutdown Current	I_{SD}	$V_{CTL\ 0-3} = 0V$		0.1	1.0	μA
LX Leakage Current	I_{LX}	Into LX pin		0.1	1.0	μA
High Side Switch Resistance	R_{DSON_P}	$I_{OUT} = 100mA$		250		m Ω
Low Side Switch Resistance	R_{DSON_N}	$I_{OUT} = 100mA$		350		

Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Frequency	f_{SW}		2.8	3.5	4.2	MHz
Soft-Start	t_{SS}	$V_{OUT} = 90\%$ of final value		100	500	μs
Thermal Shutdown	T_{OT}	Rising temperature		160		$^{\circ}C$
Thermal Shutdown Hysteresis	T_{HYST}			20		$^{\circ}C$
Logic Inputs - CTL0, CTL1, CTL2, and CTL3						
Input High Voltage	V_{IH}		1.2			V
Input Low Voltage	V_{IL}				0.4	V
Input High Current	I_{IH}	$V_{CTL0-3} = V_{IN}$	-2.0		5.0	μA
Input Low Current	I_{IL}	$V_{CTL0-3} = GND$	-2.0		2.0	μA

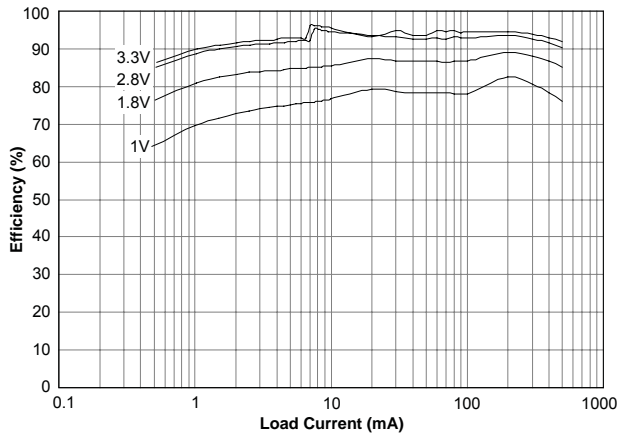
Notes

(1) Maximum output voltage is limited to V_{IN} if the input is less than 3.3V.

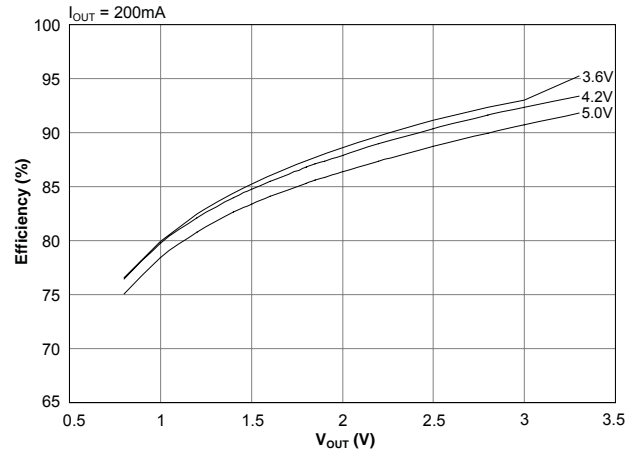
Typical Characteristics

$V_{IN} = 4.0V$ for $V_{OUT} = 3.3V$, $V_{IN} = 3.6V$ for all others. $C_{IN} = 4.7\mu F$, $C_{OUT} = 10\mu F$, $L_X = 1\mu H$, $T_A = 25^\circ C$ unless otherwise noted.

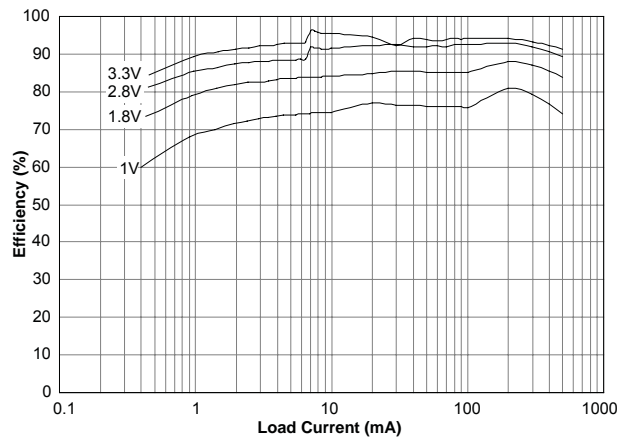
Efficiency vs. I_{OUT} ($T_A = -40^\circ C$)



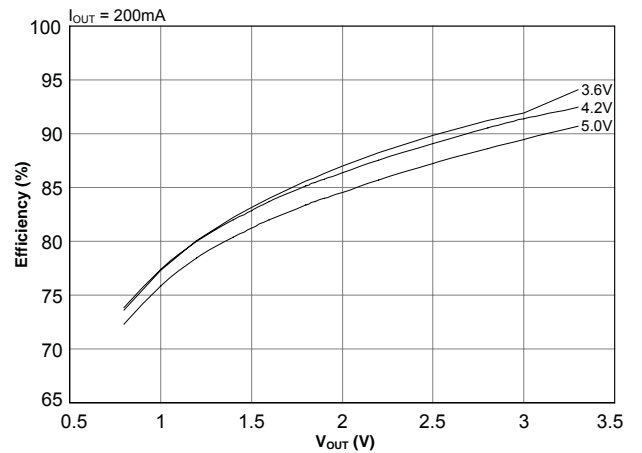
Efficiency vs. V_{OUT} ($T_A = -40^\circ C$)



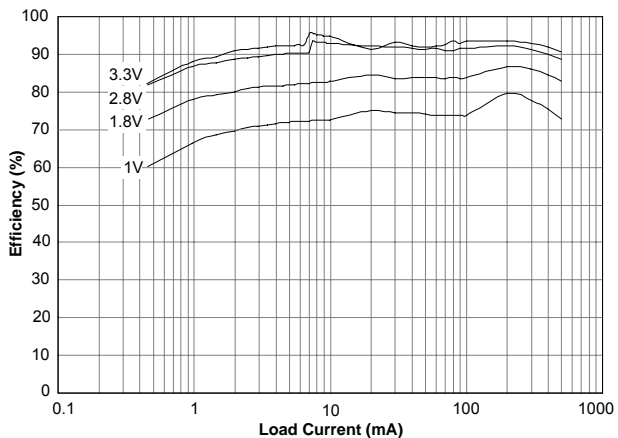
Efficiency vs. I_{OUT} ($T_A = 25^\circ C$)



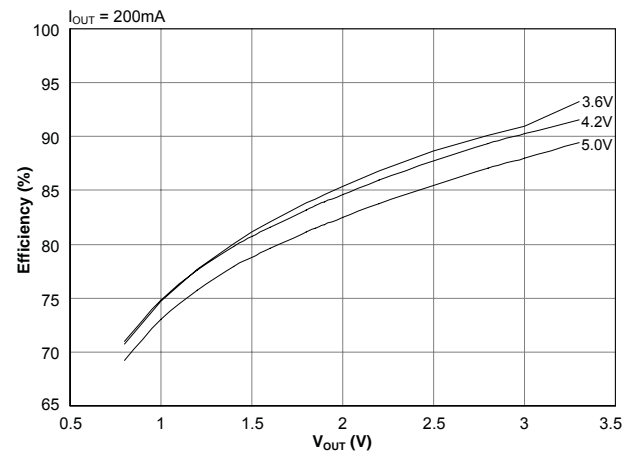
Efficiency vs. V_{OUT} ($T_A = 25^\circ C$)



Efficiency vs. I_{OUT} ($T_A = 85^\circ C$)



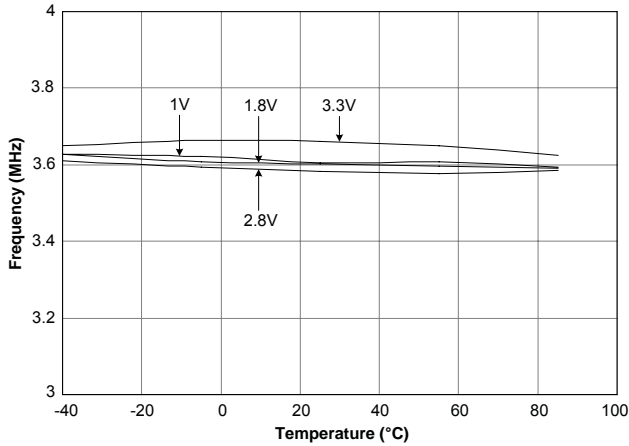
Efficiency vs. V_{OUT} ($T_A = 85^\circ C$)



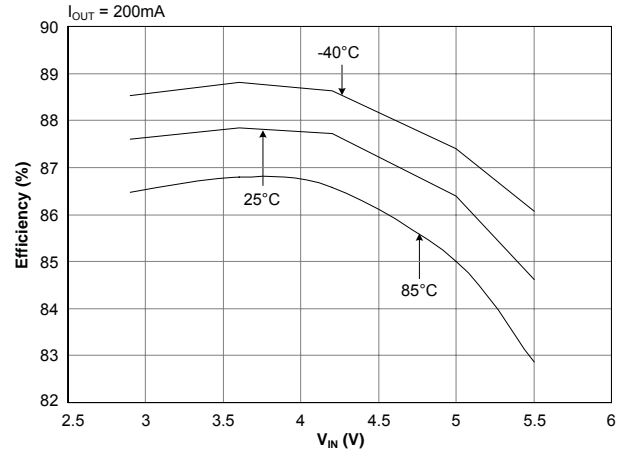
Typical Characteristics (continued)

$V_{IN} = 4.0V$ for $V_{OUT} = 3.3V$, $V_{IN} = 3.6V$ for all others. $C_{IN} = 4.7\mu F$, $C_{OUT} = 10\mu F$, $L_X = 1\mu H$, $T_A = 25^\circ C$ unless otherwise noted.

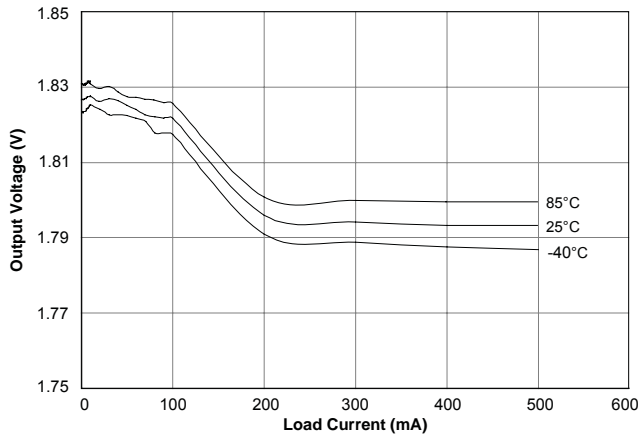
Frequency vs. Temperature



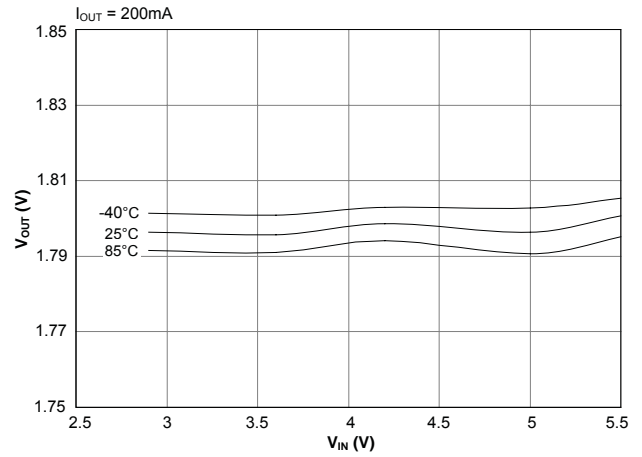
Efficiency vs. V_{IN} ($V_{OUT}=1.8V$)



Load Regulation ($V_{OUT} = 1.8V$)

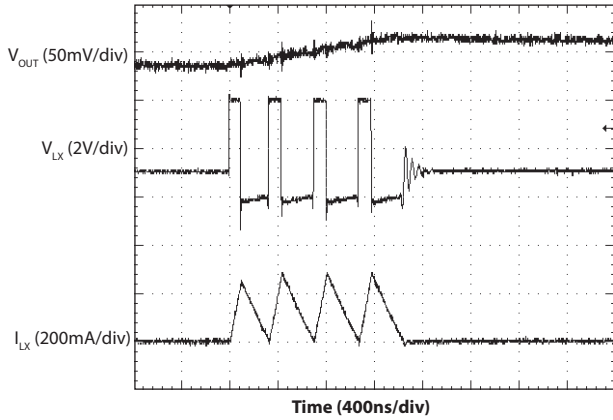


Line Regulation ($V_{OUT}=1.8V$)

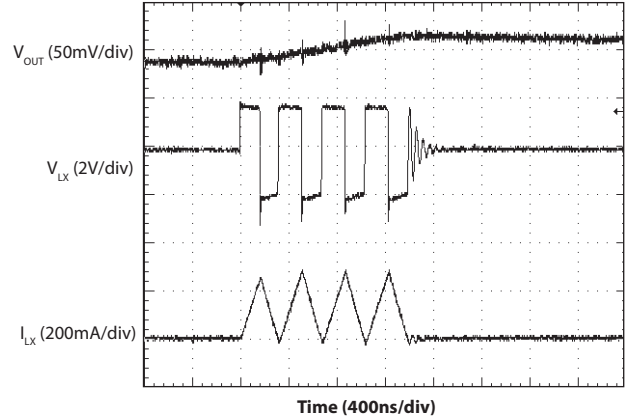


Typical Characteristics (continued)

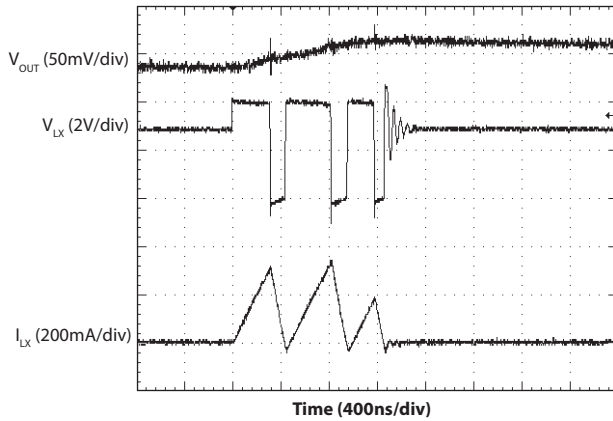
Light Load Switching — $V_{OUT} = 1.0V$



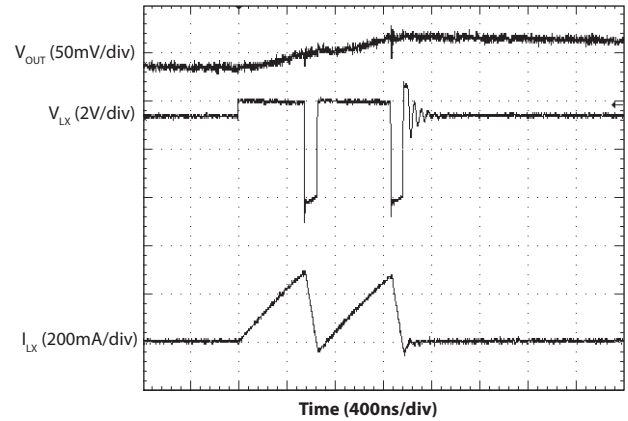
Light Load Switching — $V_{OUT} = 1.8V$



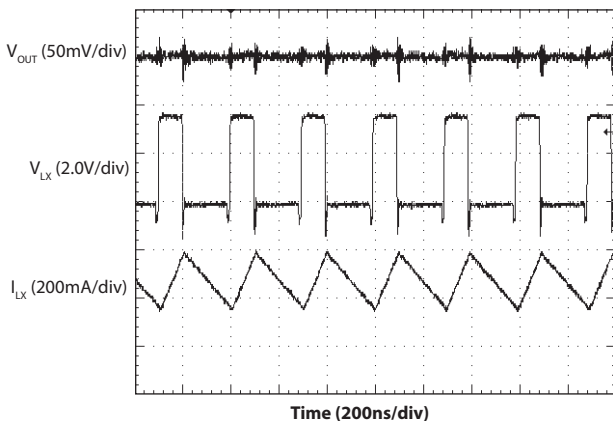
Light Load Switching — $V_{OUT} = 2.8V$



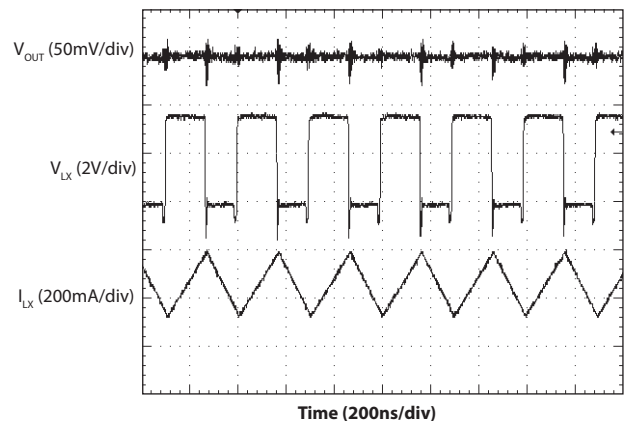
Light Load Switching — $V_{OUT} = 3.3V$



Heavy Load Switching — $V_{OUT} = 1.0V$

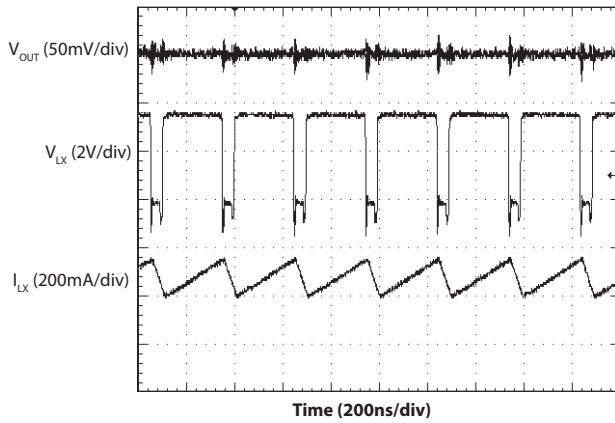


Heavy Load Switching — $V_{OUT} = 1.8V$

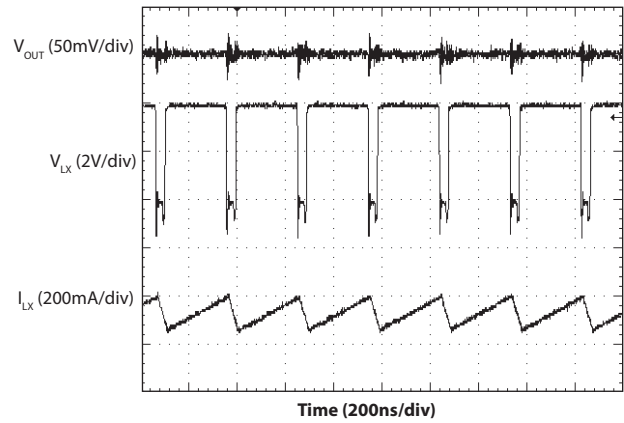


Typical Characteristics (continued)

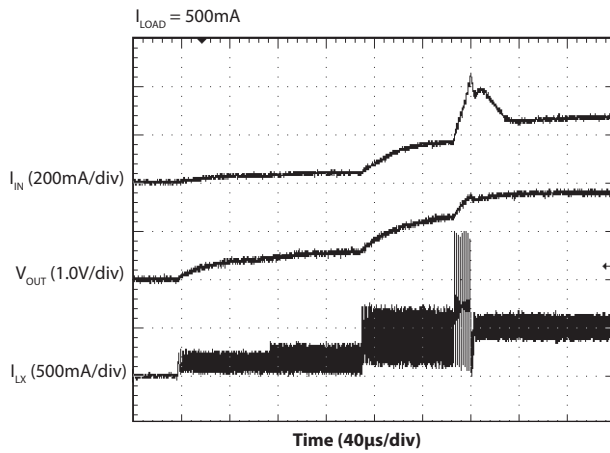
Heavy Load Switching — $V_{OUT} = 2.8V$



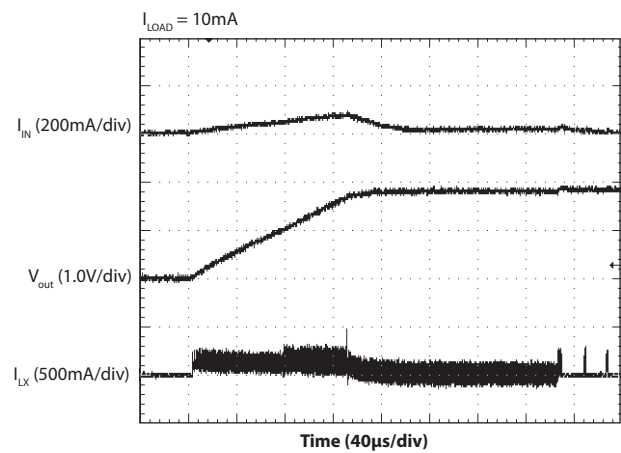
Heavy Load Switching — $V_{OUT} = 3.3V$



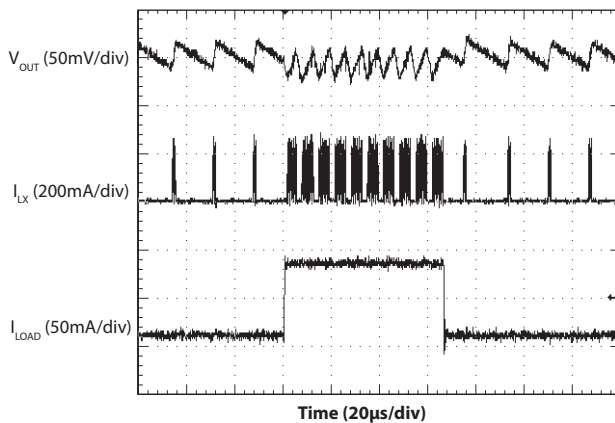
Heavy Load Soft Start



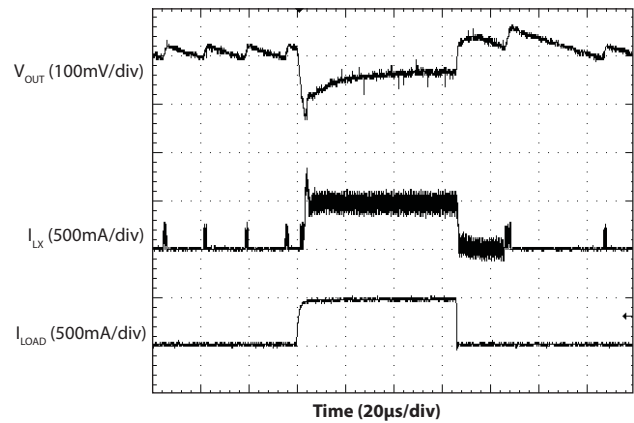
Light Load Soft Start



Load Transient Response — 10 to 80mA

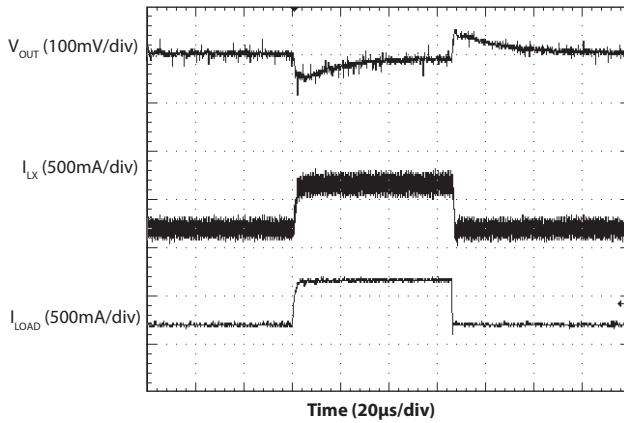


Load Transient Response — 10 to 500mA

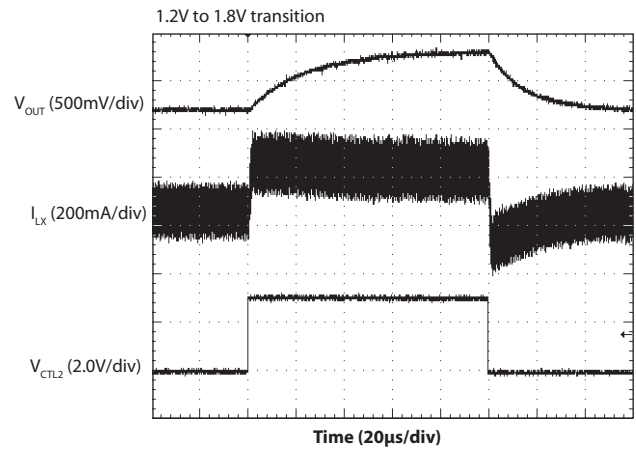


Typical Characteristics (continued)

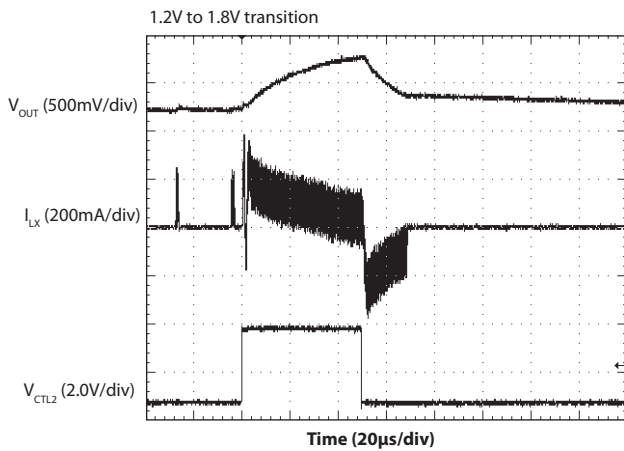
Load Transient Response — 200 to 500mA



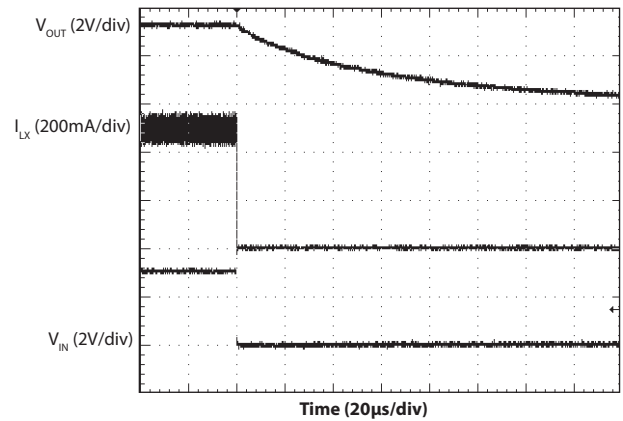
VID Transient Response — PWM



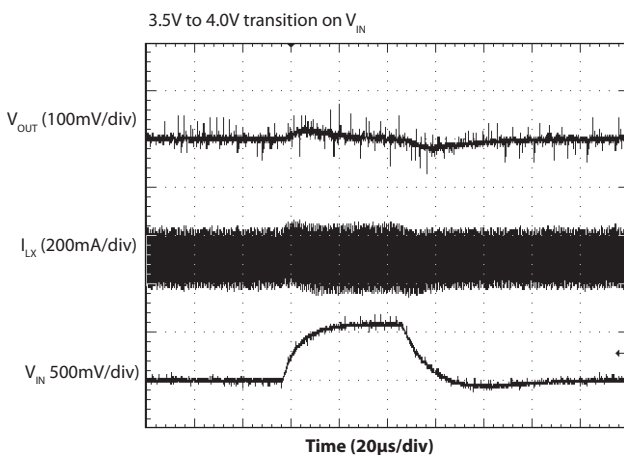
VID Transient Response — PSAVE



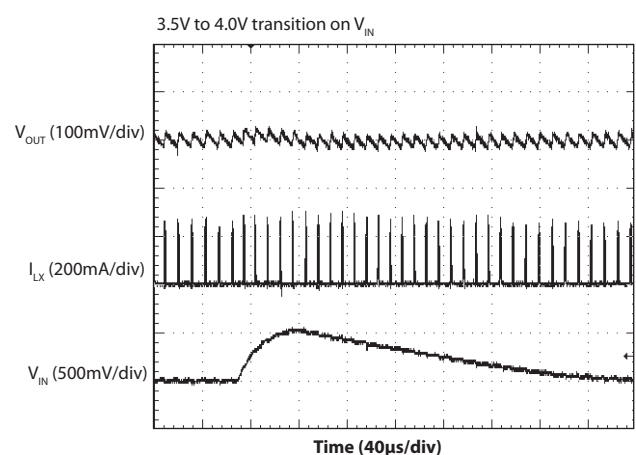
Shutdown Transient Response



Line Transient Response — PWM



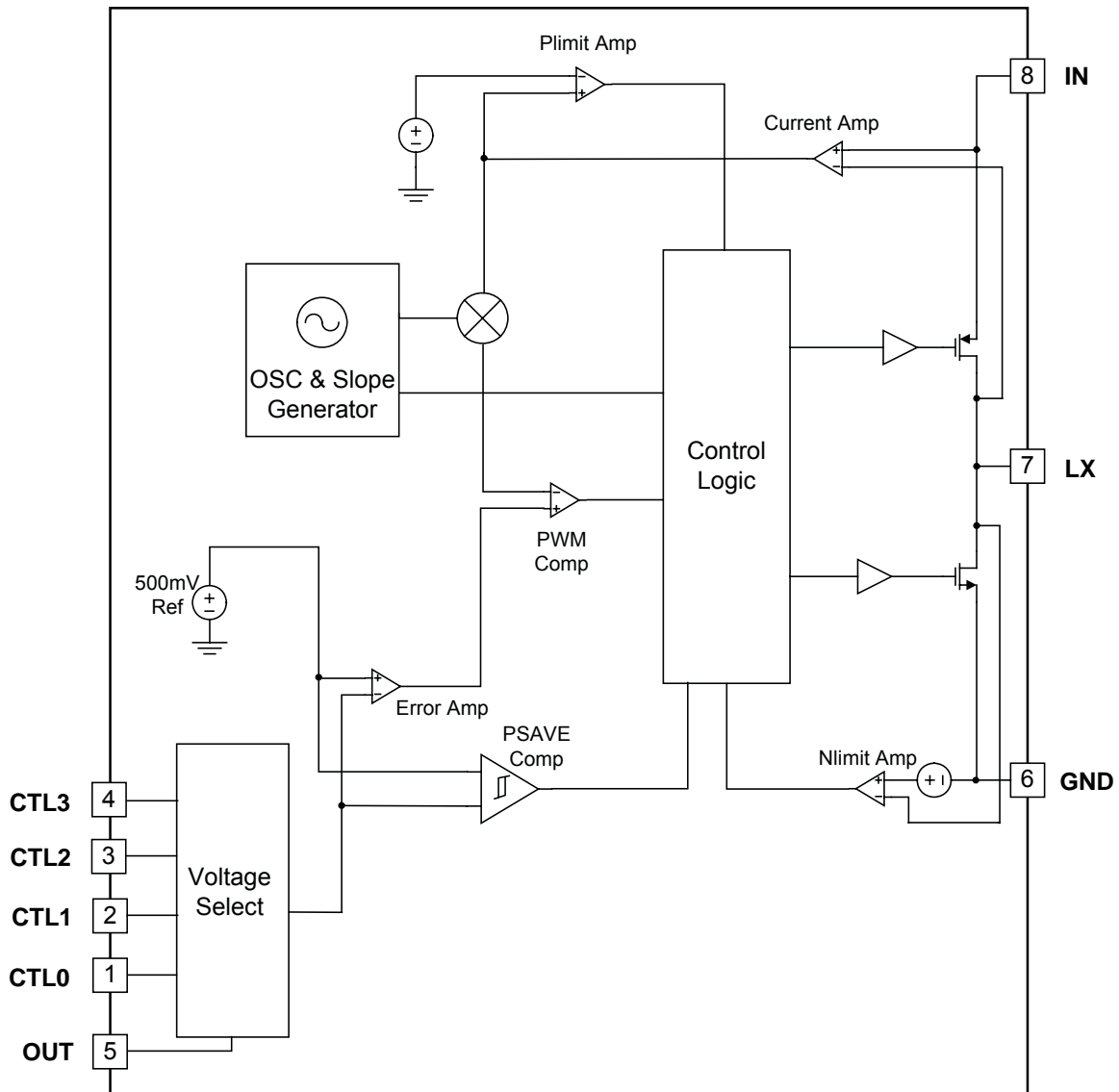
Line Transient Response — PSAVE



Pin Descriptions

Pin	Pin Name	Pin Function
1	CTL2	Control bit 2 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor ($> 1M\Omega$) in place at reset that is removed when CTL2 is pulled above the logic high threshold.
2	CTL1	Control bit 1 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor ($> 1M\Omega$) in place at reset that is removed when CTL1 is pulled above the logic high threshold.
3	CTL0	Control bit 0 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor ($> 1M\Omega$) in place at reset that is removed when CTL0 is pulled above the logic high threshold.
4	OUT	Output voltage sense pin — output voltage regulation point (connection node of inductor and output capacitor).
5	GND	Ground reference and power ground for the SC195.
6	LX	Switching output — connect an inductor between this pin and the load to filter the pulsed output current.
7	IN	Input power supply pin — connect a bypass capacitor from this pin to GND.
8	CTL3	Control bit 3 — see Table 1, page 2, for decoding. This pin has a weak pull-down resistor ($> 1M\Omega$) in place at reset that is removed when CTL3 is pulled above the logic high threshold.

Block Diagram



Applications Information

General Description

The SC195 is a synchronous step-down Pulse Width Modulated (PWM) DC-DC regulator utilizing a 3.5MHz fixed-frequency voltage mode architecture. The device is designed to operate in fixed-frequency PWM mode and enter power save (PSAVE) mode utilizing pulse frequency modulation under light load conditions to maximize efficiency. The device requires only two capacitors and a single inductor to be implemented in most systems. The switching frequency has been chosen to minimize the size of the inductor and capacitors while maintaining high efficiency. The output voltage is programmable, eliminating the need for external programming resistors. Loop compensation is also internal, eliminating the need for external components to control stability.

Programmable Output Voltage

The SC195 has fifteen fixed output voltage levels which can be individually selected by programming the CTL control pins (CTL1-CTL4 — see Table 1 on page 2 for settings). The device is disabled whenever all four CTL pins are pulled low and enabled whenever at least one of the CTL pins is pulled high. This control approach eliminates the need for a dedicated enable pin. Each CTL pin is internally pulled down via $1M\Omega$ if V_{IN} is below 1.5V or if the voltage on the control pin is below the input high voltage. This ensures that the output is disabled when power is applied if there are no inputs to the CTL pins. Each weak pull-down is disabled whenever its pin is pulled high and remains disabled until all CTL pins are pulled low.

The output voltage can be set using different approaches. If a static output voltage is required, the CTL pins can be tied to either IN or GND so that the desired voltage is set whenever power is applied at IN. If enable control is required, each CTL pin can be tied to either GND or to a microprocessor I/O line to create the desired control code whenever the control signal is forced high. This approach is equivalent to using the CTL pins collectively as a single enable pin. A third option is to connect each of the four CTL pins to individual microprocessor I/O lines. Any of the 15 output voltages can be programmed using this approach. If only two output voltages are needed, the CTL pins can be combined in a way that will reduce the number of I/O lines to 1, 2, or 3, depending on the control code for each desired voltage. Other CTL pins could be

hard wired to GND or IN. This option allows dynamic voltage adjustment for systems that reduce the supply voltage when entering sleep states. Note that applying all zeros to the CTL pins when changing the output voltages will temporarily disable the device, so it is important to avoid this combination when dynamically changing levels.

PWM Operation

Normal PWM operation occurs when the output load current exceeds the PSAVE threshold. In this mode, the PMOS high side switch is activated with the duty cycle required to produce the output voltage programmed by the CTL pins. An internal synchronous NMOS rectifier eliminates the need for an external Schottky diode on the LX pin. As V_{IN} decreases, the duty cycle (percentage of time PMOS is active) increases. As the input voltage approaches the programmed output voltage, the duty cycle approaches 100% (PMOS always on) and the device enters a pass-through mode until the input voltage increases or the load decreases enough to allow PWM switching to resume.

Power Save Mode Operation

When the load current decreases below the PSAVE threshold, PWM switching stops and the device automatically enters PSAVE mode. This threshold varies depending on the input voltage and output voltage setting, optimizing efficiency for all possible load currents - whether in PWM or PSAVE mode. While in PSAVE mode, output voltage regulation is controlled by a series of bursts in switching. During a burst, the inductor current is limited to a peak value which controls the on-time of the PMOS switch. After reaching this peak, the PMOS switch is disabled and the inductor current is forced to near 0mA. Switching bursts continue until the output voltage climbs to $V_{OUT} + 2.5\%$ or until the PSAVE current limit is reached. Switching is then stopped to eliminate switching losses, enhancing overall efficiency. Switching resumes when the output voltage reaches the lower threshold of V_{OUT} and continues until the upper threshold again is reached. Note that the output voltage is regulated hysteretically while in PSAVE mode between V_{OUT} and $V_{OUT} + 2.5\%$. The period and duty cycle while in PSAVE mode are solely determined by V_{IN} and V_{OUT} until PWM

Applications Information (continued)

mode resumes. This can result in the switching frequency being much lower than the PWM mode frequency.

If the output load current increases enough to cause V_{OUT} to decrease below the PSAVE exit threshold ($V_{OUT} - 2\%$), the device automatically exits PSAVE and operates in continuous PWM mode. Note that the PSAVE high and low threshold levels are both set at or above V_{OUT} to minimize undershoot when the SC195 exits PSAVE. Figure 1 illustrates the transitions from PWM mode to PSAVE mode and back to PWM mode.

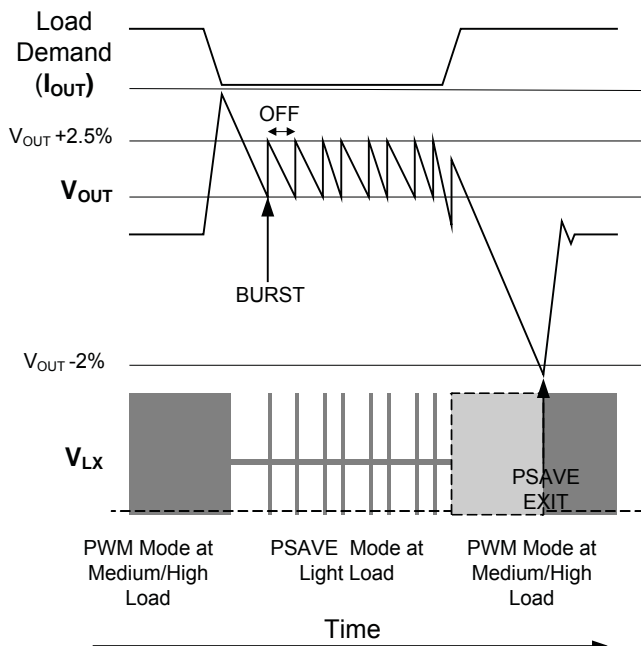


Figure 1 — Transitions Between PWM and PSAVE Modes

Protection Features

The SC195 provides the following protection features:

- Soft-Start Operation
- Over-Voltage Protection
- Current Limit
- Thermal Shutdown
- Under-Voltage Lockout

Soft-Start

The soft-start sequence is activated after a transition from an all zeros CTL code to a non-zero CTL code enables the part. Soft-start is also activated by any overload event that causes the part to shutdown until the overload goes away. At start-up, the PMOS current limit is stepped

through four levels: 25%, 40%, 60%, and 100%. Each step is maintained for 60 μ s following an internal reference start up of 20 μ s, resulting in a total nominal start-up period of 260 μ s. If V_{OUT} reaches 90% of the target within the first 2 steps, the chip continues in PSAVE mode at the end of soft-start; otherwise, it goes into PWM mode. Note the V_{OUT} ripple in PSAVE mode can be larger than the ripple in PWM mode.

Over-Voltage Protection

Over-voltage protection is provided to ensure the output voltage does not rise to a level that could damage its load. When V_{OUT} exceeds the regulation voltage by 15%, the PWM drive is disabled. Switching does not resume until V_{OUT} has fallen below the regulation voltage by 2%.

Current Limit

The SC195 switching stage is protected by a current limit function. If the output load exceeds the PMOS current limit for 32 consecutive switching cycles, the device enters fold-back current limit mode and the output current is limited to approximately 150mA. Under these conditions, the output voltage will be the product of I_{FB-LIM} and the load resistance. The load must fall below I_{FB-LIM} for the device to exit fold-back current limit mode. This function makes the device capable of sustaining an indefinite short circuit on its output under fault conditions.

Thermal Shutdown

The SC195 has a thermal shutdown feature to protect the device if the junction temperature exceeds 160°C. During thermal shutdown, the PMOS and NMOS switches are both disabled, tri-stating the LX output. When the junction temperature drops by the hysteresis value (20°C), the device goes through the soft-start process and resumes normal operation.

Under-Voltage Lockout

Under-Voltage Lockout (UVLO) is enabled when the supply voltage drops below the UVLO threshold. This prevents the device from entering an ambiguous state in which regulation cannot be maintained. Hysteresis of approximately 200mV is included to prevent chattering near the threshold.

Applications Information (continued)

Inductor Selection

The SC195 is designed to operate with a 1μH inductor between the LX pin and the OUT pin. Other values may lead to instability, malfunction, or out-of-specification performance. The specified current levels for PSAVE entry, PSAVE exit, and current limit are dependent on the inductor value.

The SC195 converter has internal loop compensation. The compensation is designed to work with a specific single-pole output filter corner frequency defined by the equation

$$f_c = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

Where, $L = 1\mu\text{H}$ and $C_{OUT} = 10\mu\text{F}$.

When selecting output filter components, the LC product should not vary over a wide range. Selection of smaller inductor and capacitor values will move the corner frequency, potentially impacting system stability.

It is also important to consider the change in inductance with DC bias current when choosing an inductor. The inductor saturation current is specified as the current at which the inductance drops a specific percentage from the nominal value (approximately 30%). Except for short-circuit or other fault conditions, the peak current must always be less than the saturation current specified by the manufacturer. The peak current is the maximum load current plus one half of the inductor ripple current at the maximum input voltage. Load and/or line transients can cause the peak current to exceed this level for short durations. Maintaining the peak current below the inductor saturation specification keeps the inductor ripple current and the output voltage ripple at acceptable levels. Manufacturers often provide graphs of actual inductance and saturation characteristics versus applied inductor current. The saturation characteristics of the inductor can vary significantly with core temperature. Core and ambient temperatures should be considered when examining the core saturation characteristics.

When the inductor value has been determined, the DC resistance (DCR) must be examined. Efficiency can be optimized by lowering the inductor's DCR as much as possible. Low DCR in an inductor requires either more surface area for the increased wire diameter or fewer turns to reduce the length of the copper winding. Fewer turns requires an inductor core with a larger cross-sectional area in order to maintain the same saturation characteristics. The inductor size must always be considered when examining the inductor DCR to determine the best compromise between DCR and component area on a PCB. Note that the ripple component of the inductor is a small percentage of the DC load. AC losses in the inductor core and winding do not contribute significantly to the total losses.

Magnetic fields associated with the output inductor can interfere with nearby circuitry. This can be minimized by the use of low-noise shielded inductors which use the minimum gap possible to limit the distance that magnetic fields can radiate from the inductor. Shielded inductors, however, typically have a higher DCR and are, therefore, less efficient than a similar sized non-shielded inductor.

Final inductor selection depends on various design considerations such as efficiency, EMI, size, and cost. Table 2 lists the manufacturers of recommended inductor options. The inductors with larger packages tend to provide better overall efficiency, while the smaller package inductors provide decent efficiency with reduced footprint or height. The saturation current ratings and DC characteristics are also shown.

Applications Information (continued)

Table 2 — Recommended Inductors

Manufacturer Part Number	L (μH)	DCR (Ω)	Saturation Current (mA)	L at 400mA (μH)	Dimensions LxWxH (mm)
Murata LQM21PN1R0MCO	1.0±20%	0.19	800	0.75	2.0x1.25x0.55
Murata LQM2HPN1R0MJ0	1.0±20%	0.09	1500	0.95	2.5x2.0x1.1
Murata LQM31PN1R0M00	1.0±20%	0.12	1200	0.95	3.2x1.6x0.85
Taiyo Yuden CKP25201R0M-T	1.0±20%	0.08	800	0.88	2.5x2.0x1.0
Toko MDT2012-CR1R0N	1.0±30%	0.08	1350	1.00	2.0x1.25x1.0
FDK MIPSZ2012D1R0	1.0±30%	0.09	1100	1.00	2.0x1.25x1.0
FDK MIPSU2520D1R0	1.0±30%	0.08	1300	0.78	2.5x2.0x0.5
FDK MIPS A2520D1R0	1.3±30%	0.09	1200	1.20	2.5x2.0x1.2
Taiyo Yuden BRC1608T1R0M	1.0±20%	0.18	850	0.90	1.6x0.8x0.8

C_{OUT} Selection

The internal voltage loop compensation in the SC195 limits the minimum output capacitor value to 10μF. This is due to its influence on the the loop crossover frequency, phase margin, and gain margin. Increasing the output capacitor above this minimum value will reduce the cross-over frequency and provide greater phase margin.

The output capacitor determines the output voltage ripple and contributes load current during large step load transitions. A capacitor between 10μF and 22μF will usually be adequate in stabilizing the output during large load transitions.

Capacitors with X7R or X5R ceramic dielectric are recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

The output voltage droop due to a load transient is determined by the capacitance of the ceramic output capacitor. The ceramic capacitor supplies the load current initially until the loop responds. Within a few switching cycles the loop will respond and the inductor current will increase to match the required load. The output voltage droop during

the period prior to the loop responding can be related to the choice of output capacitor by the relationship

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f}$$

This equation determines the minimum value for the output capacitor with respect to load transient performance. Once the inductor current increases its average value to the DC load current, the output voltage recovers. For example, for a step from 100mA to 500mA requiring less than 50mV droop, the output capacitance should be

$$C_{OUT} = \frac{3 \times 0.4}{0.05 \times 4 \times 10^6} = 6.0\mu F$$

The output capacitor RMS current ripple may be calculated from the following equation.

$$I_{RMS} = \frac{1}{2\sqrt{3}} \left(\frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{L \times f \times V_{IN(MAX)}} \right)$$

Table 3 lists the manufacturers of recommended output capacitor options.

Table 3 — Recommended Output Capacitors

Manufacturer Part Number	Value (μF)	Type	Rated Voltage (VDC)	Dimensions LxWxH (mm) Case Size
Murata GRM188R60J106ME47D	10±20%	X5R	6.3	1.6x0.8x0.8 0603
Murata GRM21BR60J106K	10±10%	X5R	6.3	2.0x1.25x1.25 0805

C_{IN} Selection

The SC195 input source current will appear as a DC supply current with a triangular ripple imposed on it. To prevent large input voltage ripple, a low ESR ceramic capacitor is required. A minimum value of 4.7μF should be used. It is important to consider the DC voltage coefficient characteristics when determining the actual required value. It should be noted that a 10μF, 6.3V, X5R ceramic capacitor with 5V DC applied may exhibit a capacitance as low as 4.5μF. The value of required input capacitance is estimated by determining the acceptable input ripple voltage and

Applications Information (continued)

calculating the minimum value required for C_{IN} from the equation

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}{\left(\frac{\Delta V}{I_{OUT}} - ESR \right) f}$$

The input capacitor RMS ripple current varies with the input and output voltage. The maximum input capacitor RMS current is found from the equation

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

The input voltage ripple and RMS current ripple are at maximum levels when the input voltage is twice the output voltage (50% duty cycle scenario).

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the PMOS switch. Low ESR/ESL X5R ceramic capacitors are recommended for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IN and GND pins of the SC195. Table 4 lists the recommended input capacitor options from different manufacturers.

Table 4 — Recommended Input Capacitors

Manufacturer Part Number	Value (μF)	Type	Rated Voltage (VDC)	Dimensions LxWxH (mm) Case Size
Murata GRM188R60J475K	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603
Murata GRM188R60J106K	10±10%	X5R	6.3	1.6x0.8x0.8 0603
Taiyo Yuden JMK107BJ475KA	4.7±10%	X5R	6.3	1.6x0.8x0.8 0603

PCB Layout Considerations

The layout diagram in Figure 2 shows a recommended PCB top-layer for the SC195 and supporting components. Specified layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of the DC-DC converter and can contrib-

ute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following guidelines are recommended for designing a PCB layout:

1. The input capacitor, C_{IN} , should be placed as close to the VIN and GND pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to connect as closely to the IC as possible. This will minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the LX pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit. C_{OUT} and L_X should be connected as close as possible between the LX and GND pins, with a direct return to the GND.
3. Use a ground plane referenced to the GND pin. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
4. Route the output voltage feedback/sense path away from the inductor and LX node to minimize noise and magnetic interference.
5. Minimize the resistance from the OUT and GND pins to the load. This will reduce errors in DC regulation due to voltage drops in the traces.

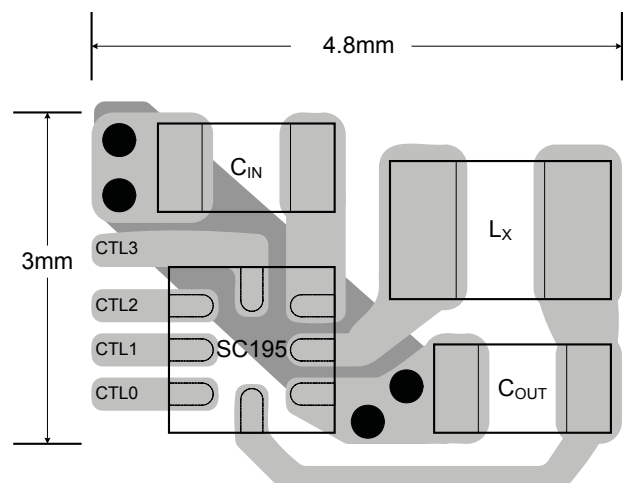
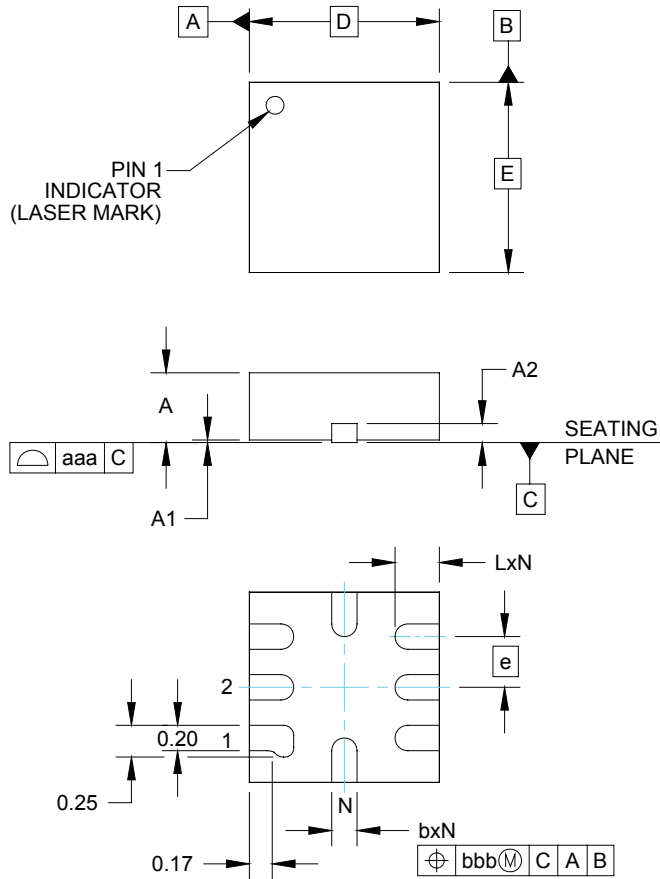


Figure 2 — Recommended PCB Layout

Outline Drawing — MLPQ-UT8

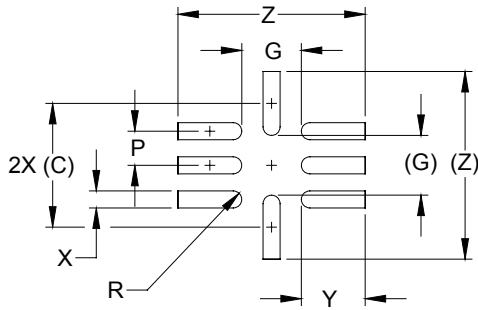


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2	(.006)			(0.1524)		
b	.006	.008	.010	0.15	0.20	0.25
D	.059 BSC			1.50 BSC		
E	.059 BSC			1.50 BSC		
e	.016 BSC			0.40 BSC		
L	0.12	.014	0.16	0.30	0.35	0.40
N	8			8		
aaa	.004			0.10		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern — MLPQ-UT8



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.057)	(1.45)
G	.028	0.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.030	0.75
Z	.087	2.20

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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