



# SC2151A Type-C/ PD and DPDM Fast Charge Controller with CC/CV Internal Feedback Compensation Integrated

## 1 Description

SC2151A is a Type-C / PD and DPDM fast charge controller, with internal feedback compensation integrated. It complies with the latest Type-C and PD 3.0 standards and supports the proprietary high voltage fast charge protocols with DPDM interface. It targets for the wall adapters and travel adapters applications.

SC2151A minimizes external components by integrating USB PD baseband PHY, Type-C detection, DPDM PHY, VBUS discharging paths, VCONN supply, programmable feedback compensation, voltage and current sense, 10-bit high performance ADC, dual 10-bit DACs, NMOS gate driver, I2C interface and protection circuits. It contains a 32-bit high performance micro-controller core with 24kByte OTP and 2kByte RAM, which provides cost effective solutions to many applications.

SC2151A supports various protection mechanisms including Over Voltage Protection (OVP), Under Voltage Protection (UVP), Over Current Protection (OCP), Short Circuit Protection (SCP), Over Temperature Protection (OTP), DPDM Over Voltage Protection (DPDM OVP), CC Over Voltage Protection (CCOVP), VCONN Over Voltage (VCONN OVP), VCONN Over Current (VCONN OCP) and VCONN Short Protection (VCONN SCP), so to effectively ensure stable and reliable operation of system.

The SC2151A is available in 16-pin QFN package.

## 2 Features

- **USB Type-C**
  - Support Type-C DFP protocols
  - Configurable resistor  $R_P$
- **USB Power Delivery**
  - Support DFP / UFP / DRP USB PD 3.0
  - Hardware BMC transmitter and receiver
  - Full feature physical layer
  - Hardware CRC
  - Hardware reset
  - Integrate PD 3.0 protocol engine
  - Integrate VCONN and support SOP' for e-marker
- **DPDM Fast Charging Interface**
  - Integrate firmware controlled DPDM interface
  - Support Apple charging, BC1.2, DCP, HVDCP, FC, AFC, FCP, SCP, VOOC, UART, I2C and other proprietary charging protocols
- **Power**
  - Wide operation range: 3.3V to 22V (26V tolerant)
  - Integrate programmable feedback compensation
- **MCU Subsystem**
  - Integrated 32-bit high performance MCU core
  - 24kByte OTP and 2kByte RAM
  - Support I2C interface and multiple I/Os
  - Support sleep mode
- **Analog Block**
  - Dual DACs for voltage regulation and current regulation
  - 10-bit ADC to monitor the voltage / current / other signals
  - Integrated current sense amplifier
  - Integrated NMOS gate driver
  - Integrated VBUS discharging paths at both sides of isolation MOS
  - Integrated temperature sense module
- **Protections**
  - On chip OVP, UVP, SCP, VCONN OVP, VCONN OCP, VCONN SCP, OTP, DPDM OVP, CC OVP
  - VBUS to CC / DPDM short protection
  - GND to CC / DPDM short protection
- **Package**
  - 16-pin QFN, 4mm x 4mm x 0.75mm

## 3 Applications

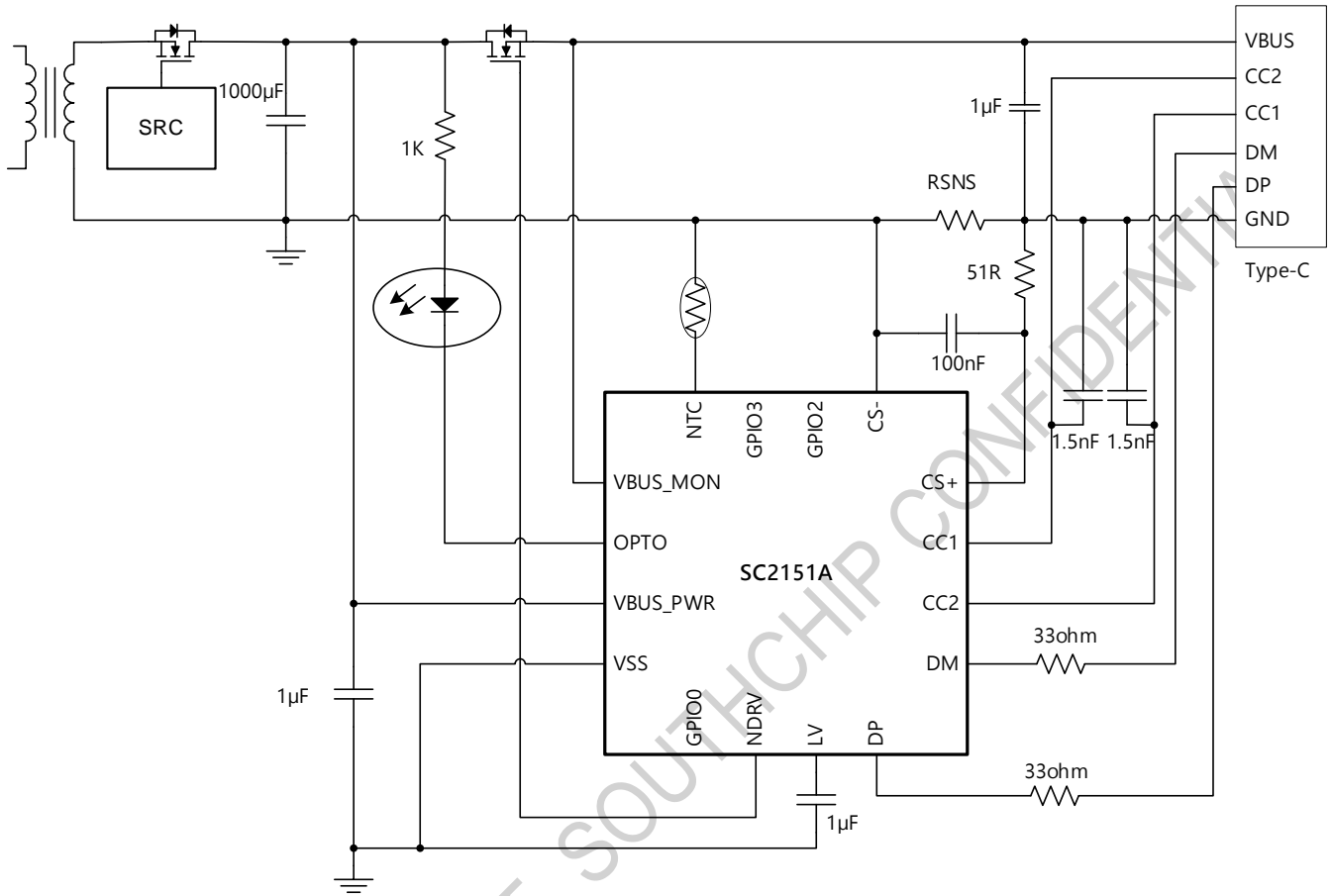
- Wall adapters
- Travel adapters

## 4 Device Information

| Part Number | Package | Body Size          |
|-------------|---------|--------------------|
| SC2151AQDER | QFN-16  | 4mm x 4mm x 0.75mm |



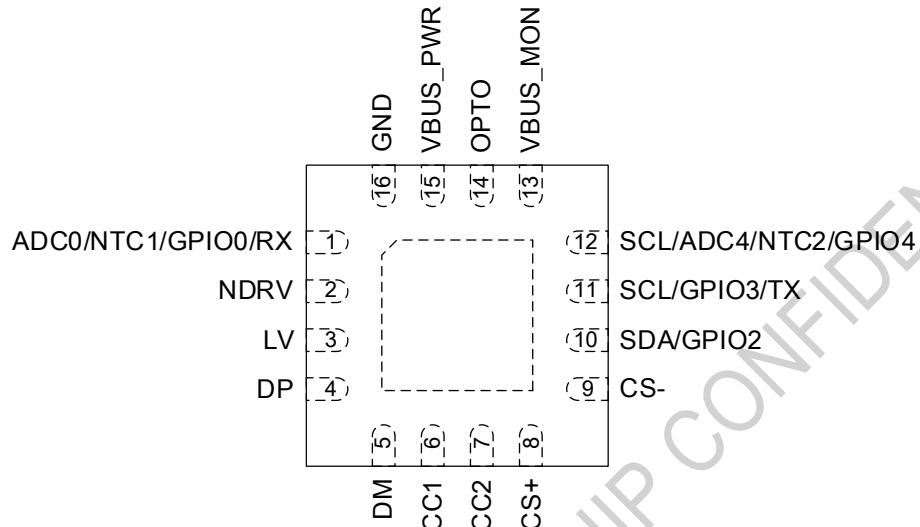
### 5 Typical Application Diagram





6 Terminal Configuration and Functions

TOP VIEW of SC2151A



| TERMINAL |       | I/O | DESCRIPTION  |
|----------|-------|-----|--|
| NUMBER   | NAME  |     |  |
| 1        | ADC0  | I   | ADC input channel 0  |
|          | NTC1  | I   | Remote thermal sensor connection node for external temperature monitoring  |
|          | GPIO0 | I/O | General purpose input and output port 1  |
|          | RX    | I   | Universal Asynchronous Receiver/Transmitter (UART), input port.  |
| 2        | NDRV  | O   | N-MOS driver. Connect this pin to the gate of isolation MOS.   |
| 3        | LV    | I/O | Internal LDO output. Connect a 1µF ceramic capacitor between this pin and ground   |
| 4        | DP    | I/O | USB DP line of the fast charging interface   |
| 5        | DM    | I/O | USB DM line of the fast charging interface   |
| 6        | CC1   | I/O | Type-C connector configuration channel 1, used to detect a device plug event, determine the cable orientation, transmit or receive PD protocols and configured as the output of VCONN supply |
| 7        | CC2   | I/O | Type-C connector configuration channel 2, used to detect a device plug event, determine the cable orientation, transmit or receive PD protocols and configured as the output of VCONN supply |
| 8        | CS+   | I   | Positive input of current sense amplifier  |
| 9        | CS-   | I   | Negative input of current sense amplifier  |



|    |             |     |   |
|----|-------------|-----|---|
| 10 | SDA         | I/O | I2C interface data line, I2C interface of SC2151A supports master mode and slave mode   |
|    | GPIO2       | I/O | General purpose input and output port 2   |
| 11 | SCL         | I/O | I2C interface clock line. I2C interface of SC2151A supports master mode and slave mode, and clock line can be configured to pin 11 and pin 12   |
|    | GPIO3       | I/O | General purpose input and output port 3   |
|    | TX          | O   | Output port of universal asynchronous receiver/transmitter module   |
| 12 | SCL         | I/O | I2C interface clock line. I2C interface of SC2151A supports master mode and slave mode, and clock line can be configured to pin 11 and pin 12   |
|    | ADC4        | I   | ADC input channel 4   |
|    | NTC2        | I   | Remote thermal sensor connection node for external temperature monitoring   |
|    | GPIO4       | I/O | General purpose input and output port 4   |
| 13 | VBUS_MON    | I   | Connected to the VBUS line of the USB Type-C port. It is also used to sense the VBUS voltage of the port and is internally connected to the discharge path  |
| 14 | OPTO        | O   | Current sink output for optocoupler connection  |
| 15 | VBUS_PWR    | I   | Power supply pin of this IC which should be connected to VBUS power node. It is also used to sense the VBUS voltage and is internally connected to the discharge path. It is recommended to connect at least 1 $\mu$ F bypass capacitor from this pin to ground close to the IC |
| 16 | GND         | I/O | Ground of IC  |
| 17 | Thermal Pad | -   | Connect pad to GND  |



## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|   |  | MIN  | MAX | Unit |
|---|--|------|-----|------|
| Voltage range at terminals <sup>(2)</sup> | NDRV   | -0.3 | 31  | V    |
|   | VBUS_PWR, VBUS_MON, OPTO, CC1, CC2   | -0.3 | 26  | V    |
|   | DP, DM   | -0.3 | 12  | V    |
|   | ADC0/NTC1/GPIO0/TX, LV, CS+, CS-, SDA/GPIO2, SCL/GPIO3/TX, SCL/ADC4/NTC2/GPIO4 | -0.3 | 5.5 | V    |
|   | Operating junction temperature   | -40  | 150 | °C   |
|   | Storage temperature  | -65  | 150 | °C   |
| T <sub>L</sub>                            | Lead temperature   |      | 260 | °C   |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

### 7.2 Thermal Information

| THERMAL RESISTANCE <sup>(1)</sup> |  | QFN-16 (4mmX4mm) | UNIT |
|-----------------------------------|--|------------------|------|
| $\theta_{JA}$                     | Junction to ambient thermal resistance | TBD              | °C/W |
| $\theta_{JC}$                     | Junction to case thermal resistance    | TBD              | °C/W |

(1) Measured on JESD51-7, 4-layer PCB.

### 7.3 Handling Ratings

| PARAMETER          | DEFINITION                                |          | MIN  | MAX | UNIT |
|--------------------|---|----------|------|-----|------|
| ESD <sup>(1)</sup> | Human-body Model (HBM) <sup>(2)</sup>     | All pins | -2   | 2   | kV   |
|                    | Charged-device Model (CDM) <sup>(3)</sup> | All pins | -750 | 750 | V    |

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.4 Recommended Operating Conditions

|                       |  | MIN | TYP | MAX                 | UNIT |
|-----------------------|--|-----|-----|---------------------|------|
| V <sub>BUS_PWR</sub>  | VBUS_PWR operation voltage                             | 3.3 |     | 22                  | V    |
| C <sub>VBUS_PWR</sub> | Bulk capacitor at VBUS_PWR pin                         |     |     | 1600 <sup>(4)</sup> | μF   |
| C <sub>VBUS_MON</sub> | Bulk capacitor at VBUS_MON pin for Type-C applications | 1   |     | 10                  | μF   |



|                |                                |     |  |     |    |
|----------------|--------------------------------|-----|--|-----|----|
| T <sub>A</sub> | Operating ambient temperature  | -40 |  | 85  | °C |
| T <sub>J</sub> | Operating junction temperature | -40 |  | 125 | °C |

(4) It is recommended to add external discharge circuit on VBUS\_PWR node if the bulk capacitance at VBUS\_PWR node is higher than 1600μF.

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### 7.5 Electrical Characteristics

T<sub>J</sub>= 25°C unless otherwise noted.

| PARAMETER                            | TEST CONDITIONS                                     | MIN   | TYP   | MAX   | UNIT |
|--------------------------------------|---|---|-------|-------|------|
| <b>SUPPLY VOLTAGE (VBUS_PWR Pin)</b> |   |   |       |       |      |
| V <sub>BUS_PWR</sub>                 | VBUS_PWR supply range                               | 3.3   |       | 22    | V    |
| V <sub>BUS_PWR_POR</sub>             | VBUS_PWR power on threshold                         |   | 3.3   | 3.35  | V    |
| V <sub>BUS_PWR_UVLO</sub>            | VBUS_PWR UVLO threshold                             | 3.05  | 3.1   |       | V    |
| I <sub>q_ACT</sub>                   | Quiescent current in active mode                    |   | 10    |       | mA   |
| I <sub>q_SBY1</sub>                  | Quiescent current in standby mode1                  |   | 2     |       | mA   |
| I <sub>q_SBY2</sub>                  | Quiescent current in standby mode 2                 |   | 400   |       | μA   |
| I <sub>DIS_VBUS_PWR</sub>            | Discharging current at VBUS_PWR                     |   |       | 150   | mA   |
| V <sub>BUS_PWR_OVP</sub>             | VBUS_PWR OVP rising threshold                       | fb_sel_uvp_th = 00b                                       |       | 115   | %    |
|                                      |   | fb_sel_uvp_th = 01b                                       |       | 110   | %    |
|                                      |   | fb_sel_uvp_th = 10b                                       |       | 115   | %    |
|                                      |   | fb_sel_uvp_th = 11b                                       |       | 120   | %    |
| t <sub>VBUS_PWR_OVP</sub>            | VBUS_PWR over-voltage deglitch time                 | ovp_dgl_sel = 0   |       | 4     | μs   |
|                                      |   | ovp_dgl_sel = 1   |       | 40    | μs   |
| t <sub>DPDM_OVP</sub>                | DPDM over-voltage deglitch time                     | dpdm_ovp_dgl_sel = 0                                      |       | 4     | μs   |
|                                      |   | dpdm_ovp_dgl_sel = 1                                      |       | 40    | μs   |
| V <sub>BUS_PWR_UVP</sub>             | VBUS_PWR UVP falling threshold                      | fb_sel_uvp_th = 01b                                       |       | 75    | %    |
|                                      |   | fb_sel_uvp_th = 10b                                       |       | 85    | %    |
|                                      |   | fb_sel_uvp_th = 11b                                       |       | 95    | %    |
| t <sub>VBUS_PWR_UVP</sub>            | VBUS_PWR under-voltage deglitch time                | uvp_dgl_sel = 00b   |       | 10    | μs   |
|                                      |   | uvp_dgl_sel = 01b   |       | 30    | μs   |
|                                      |   | uvp_dgl_sel = 10b   |       | 50    | μs   |
|                                      |   | uvp_dgl_sel = 11b   |       | 70    | μs   |
| V <sub>MON_SCP_TH</sub>              | VBUS_MON short circuit protection falling threshold | 3.2   |       |       | V    |
| <b>NMOS GATE DRIVER</b>              |   |   |       |       |      |
| V <sub>DRV</sub>                     | Driving voltage                                     | V <sub>GATE</sub> -V <sub>BUS_MON</sub> , VBUS_PWR ≥ 3.3V |       | 5     | V    |
| V <sub>CLAMP_GS</sub>                | Driver clamp voltage                                |   | 7     |       | V    |
| <b>ADC</b>                           |   |   |       |       |      |
| V <sub>ADC_REF</sub>                 | Reference voltage for ADC                           | 2.244   | 2.248 | 2.252 | V    |



|                                       |  |   |        |       |      |    |
|---------------------------------------|--|---|--------|-------|------|----|
| N <sub>ADC</sub>                      | Resolution                                       |   | 10     | Bits  |      |    |
| R <sub>SAMPLE</sub>                   | ADC sample rate                                  |   | 50     | ksps  |      |    |
| K <sub>ADC_VBUS_PWR</sub>             | Ratio from VBUS_PWR voltage sense                |   | 1/10   |       |      |    |
| K <sub>ADC_VBUS_MON</sub>             | Ratio from VBUS_MON voltage sense                |   | 1/10   |       |      |    |
| K <sub>ADC_CSNS</sub>                 | Ratio from the output of current sense amplifier |   | 1      |       |      |    |
| K <sub>ADC_DPDM</sub>                 | Ratio from DP/DM                                 |   | 1/4    |       |      |    |
| K <sub>ADC_0, K<sub>ADC_4</sub></sub> | Ratio from ADC0 or ADC4 voltage sense            |   | 1      |       |      |    |
| K <sub>ITC</sub>                      | Internal temperature sense coefficient           |   | 2.819  | mV/°C |      |    |
| V <sub>ITC_27°C</sub>                 | Internal temperature sense output at 27 °C       |   | 733.94 | mV    |      |    |
| ADC <sub>VBUS_PWR</sub>               | Range  |   | 3.3    | 22    | V    |    |
|                                       | LSB  |   |        | 21.95 | mV   |    |
|                                       | Error  | VBUS = 3.3V ~ 9V                                    |        | -50   | 50   | mV |
|                                       |  | VBUS = 9V ~ 21V                                     |        | -100  | 100  | mV |
| ADC <sub>DP, ADC<sub>DM</sub></sub>   | Range  |   | 0      | 5     | V    |    |
|                                       | LSB  |   |        | 8.78  | mV   |    |
|                                       | Error  | Full range  |        | -150  | 150  | mV |
| ADC <sub>GPIO</sub>                   | Range  |   | 0      | 2.248 | V    |    |
|                                       | LSB  |   |        | 2.195 | mV   |    |
|                                       | Error  | Full range  |        | -5    | 5    | mV |
| INL                                   | Integral non-linearity                           |   | -1.0   | 1.0   | LSB  |    |
| DNL                                   | Differential non-linearity                       |   | -1.0   | 1.0   | LSB  |    |
| <b>CVDAC</b>                          |  |   |        |       |      |    |
| R <sub>FB_VBUS_PWR</sub>              | VBUS_PWR Divider Resistance                      | R <sub>UP</sub> + R <sub>DOWN</sub> on VBUS_PWR pin | 2      |       | MΩ   |    |
| N <sub>DAC_CV</sub>                   | CV loop V <sub>REF</sub> resolution              |   | 10     |       | Bits |    |
| V <sub>VBUS_PWR_ADJ_RANGE</sub>       | VBUS_PWR adjust range                            |   | 3.3    | 21    | V    |    |
| V <sub>VBUS_PWR_STEP_VOLT</sub>       | VBUS_PWR adjust voltage per step                 |   | 20     |       | mV   |    |
| V <sub>DAC_ZERO_VOLT</sub>            | VBUS_PWR voltage at VDAC code = 0                |   | 2000   |       | mV   |    |
| <b>CCDAC</b>                          |  |   |        |       |      |    |
| N <sub>DAC_CC</sub>                   | CC loop I <sub>REF</sub> resolution              |   | 10     |       | Bits |    |
| V <sub>REF_IDAC</sub>                 | IDAC reference voltage                           |   | 1.2    |       | V    |    |
| V <sub>REF_IDAC_STEP</sub>            | IDAC step voltage                                |   | 1.172  |       | mV   |    |
| <b>CURRENT SENSE</b>                  |  |   |        |       |      |    |
| G <sub>CSNS</sub>                     | Gain of current sense amplifier                  | cs_sel_20x = 1                                      | 20     |       |      |    |
|                                       |  | cs_sel_20x = 1                                      | 40     |       |      |    |





|                               |   |  |       |       |       |    |
|-------------------------------|---|--|-------|-------|-------|----|
| V <sub>OCP</sub>              | OCP threshold                                   | Calculated as $I_{BUS} * R_{SNS}$ , $I_{BUS}$ is the output current of VBUS and $R_{SNS}$ is the sense resistor placed between CS+ pin and CS- pin | 45    |       | mV    |    |
| V <sub>OCP_DT</sub>           | OCP deglitch time                               |  | 200   |       | ms    |    |
| V <sub>CS_OUT_OFFSET</sub>    | Input offset voltage of current sense amplifier | G <sub>CSNS</sub> = 40   | 250   |       | μV    |    |
|                               |   | G <sub>CSNS</sub> = 20   | 500   |       | μV    |    |
| <b>TYPE-C/PD PROTOCOLS</b>    |   |  |       |       |       |    |
| I <sub>CC_80μA</sub>          | CC1/2 pull up current                           | CSRC_I = 00b   | 64    | 80    | 96    | μA |
| I <sub>CC_180μA</sub>         | CC1/2 pull up current                           | CSRC_I = 01b   | 165.6 | 180   | 194.4 | μA |
| I <sub>CC_330μA</sub>         | CC1/2 pull up current                           | CSRC_I = 10b   | 303.6 | 330   | 356.4 | μA |
| R <sub>CC_open</sub>          | CC1/2 open impedance                            | CC1/2 in disable status  | 126   |       |       | kΩ |
| V <sub>CC_0P2_th_src</sub>    | CC1/2 0.2V comparison threshold                 | CC1/2 as source  | 0.15  | 0.2   | 0.25  | V  |
| V <sub>CC_0P4_th_src</sub>    | CC1/2 0.4V comparison threshold                 | CC1/2 as source  | 0.35  | 0.4   | 0.45  | V  |
| V <sub>CC_0P66_th_src</sub>   | CC1/2 0.66V comparison threshold                | CC1/2 as source  | 0.61  | 0.66  | 0.7   | V  |
| V <sub>CC_0P8_th_src</sub>    | CC1/2 0.8V comparison threshold                 | CC1/2 as source  | 0.75  | 0.8   | 0.85  | V  |
| V <sub>CC_1P23_th_src</sub>   | CC1/2 1.23V comparison threshold                | CC1/2 as source  | 1.18  | 1.23  | 1.28  | V  |
| V <sub>CC_1P6_th_src</sub>    | CC1/2 1.6V comparison threshold                 | CC1/2 as source  | 1.5   | 1.6   | 1.65  | V  |
| V <sub>CC_2P6_th_src</sub>    | CC1/2 2.6V comparison threshold                 | CC1/2 as source  | 2.45  | 2.6   | 2.75  | V  |
| V <sub>TH_CCOVP_RISING</sub>  | CCx OVP detection                               | CCOVP rising threshold   | 7.2   |       |       | V  |
| V <sub>TH_CCOVP_FALLING</sub> | CCx OVP release                                 | CCOVP falling threshold  | 7.0   |       |       | V  |
| Z <sub>Driver</sub>           | PD data Tx output impedance                     |  | 33    |       | 75    | Ω  |
| V <sub>Swing</sub>            | High level voltage for CC PD data               |  | 1.05  | 1.125 | 1.2   | V  |
| <b>VCONN SWITCH</b>           |   |  |       |       |       |    |
| V <sub>VCONN</sub>            | VCONN input voltage                             |  | 3     |       | 5.5   | V  |
| R <sub>VCONN</sub>            | VCONN switch on resistance                      | LV ≥ 3.3V  |       |       | 40    | Ω  |
| I <sub>VCONN</sub>            | VCONN current capability                        |  | 35    |       |       | mA |
| I <sub>VCONN_OCP</sub>        | VCONN over current                              | Rising threshold   | 70    |       |       | mA |
| <b>PROTOCOL INTERFACES</b>    |   |  |       |       |       |    |
| R <sub>SHORT</sub>            | DP DM short resistance                          | VBUS_PWR = 5V ~ 21V  |       |       | 40    | Ω  |
| V <sub>3.3V</sub>             | DPDM 3.3V buffer output voltage                 | VBUS_PWR = 5V ~ 21V  | 3.2   | 3.3   | 3.4   | V  |
| V <sub>2.7V</sub>             | DPDM 2.7V buffer output voltage                 | VBUS_PWR = 5V ~ 21V  | 2.6   | 2.7   | 2.8   | V  |
| V <sub>1.96V</sub>            | DPDM 1.96V buffer output voltage                | VBUS_PWR = 5V ~ 21V  | 1.9   | 2     | 2.1   | V  |
| V <sub>TH_3V</sub>            | VTH3V comparator threshold at DPDM pin          | VBUS_PWR = 5V ~ 21V  | 2.9   | 3     | 3.1   | V  |



|                           |  |  |      |       |      |    |
|---------------------------|--|--|------|-------|------|----|
| V <sub>TH_2.2V</sub>      | VTH2.2V comparator threshold at DPDM pin   | VBUS_PWR = 3.3V ~ 21V                                  | 2.1  | 2.2   | 2.3  | V  |
| V <sub>TH_1.35V</sub>     | VTH1.35V comparator threshold at DPDM pin  | VBUS_PWR = 3.3V ~ 21V                                  | 1.25 | 1.35  | 1.45 | V  |
| V <sub>TH_0.425V</sub>    | VTH0.425V comparator threshold at DPDM pin | VBUS_PWR = 3.3V ~ 21V                                  | 0.35 | 0.425 | 0.5  | V  |
| V <sub>TH_0.325V</sub>    | VTH0.325V comparator threshold at DPDM pin | VBUS_PWR = 3.3V ~ 21V                                  | 0.25 | 0.325 | 0.4  | V  |
| R <sub>OUT_30k</sub>      | Output resistance of DP or DM buffer       |  | 24   | 30    | 36   | kΩ |
| I <sub>OUT_0P6V</sub>     | 0.6V current capability, sink/BC1.2, DP/DM |  | 250  |       |      | μA |
| R <sub>DP/DM_DWN</sub>    | DP/DM pull down resistance                 | source/HVDCP, DM                                       | 16   | 20    | 24   | kΩ |
| R <sub>DP/DM_LKG</sub>    | DP/DM leakage                              |  | 300  | 500   | 800  | kΩ |
| V <sub>DATA_HIGH</sub>    | DP/DM data output high voltage             | Slave data output high, VBUS ≥ 3.3V, data_high_sel = 0 | 3    | 3.3   | 3.6  | V  |
|                           |  | Slave data output high, VBUS ≥ 3.3V, data_high_sel = 1 | 1.6  | 1.8   | 2.0  | V  |
| V <sub>DATA_LOW</sub>     | DP/DM data output low voltage              | Slave data output low                                  |      |       | 0.2  | V  |
| I <sub>OH_DM_3P3V</sub>   | 3.3V current capability, DM                |  | 5    |       |      | mA |
| V <sub>IH_TH</sub>        | DPDM input data rising threshold           | dpdm_in_refh_sel = 000b                                | 0.7  | 0.8   | 0.86 | V  |
|                           |  | dpdm_in_refh_sel = 001b                                | 1.1  | 1.2   | 1.3  | V  |
|                           |  | dpdm_in_refh_sel = 010b                                | 1.3  | 1.4   | 1.5  | V  |
|                           |  | dpdm_in_refh_sel = 011b                                | 1.7  | 1.8   | 1.9  | V  |
|                           |  | dpdm_in_refh_sel = 100b                                | 1.8  | 1.9   | 2.0  | V  |
|                           |  | dpdm_in_refh_sel = 101b                                | 2.0  | 2.1   | 2.2  | V  |
|                           |  | dpdm_in_refh_sel = 110b                                | 2.2  | 2.3   | 2.4  | V  |
|                           |  | dpdm_in_refh_sel = 111b                                | 2.4  | 2.5   | 2.6  | V  |
| V <sub>IL_TH</sub>        | DPDM input data falling threshold          | dpdm_in_refl_sel = 000b                                | 0.5  | 0.6   | 0.7  | V  |
|                           |  | dpdm_in_refl_sel = 001b                                | 0.9  | 1     | 1.1  | V  |
|                           |  | dpdm_in_refl_sel = 010b                                | 1    | 1.1   | 1.2  | V  |
|                           |  | dpdm_in_refl_sel = 011b                                | 1.4  | 1.5   | 1.6  | V  |
|                           |  | dpdm_in_refl_sel = 100b                                | 1.7  | 1.8   | 1.9  | V  |
|                           |  | dpdm_in_refl_sel = 101b                                | 1.8  | 1.9   | 2.0  | V  |
|                           |  | dpdm_in_refl_sel = 110b                                | 2.1  | 2.2   | 2.3  | V  |
|                           |  | dpdm_in_refl_sel = 111b                                | 2.2  | 2.3   | 2.4  | V  |
| V <sub>TH_DPDMOV</sub>    | Source/DPDM OVP detection                  | DPDMOV rising threshold                                | 4.5  | 4.75  | 5    | V  |
| t <sub>DPDM_OVP</sub>     | DPDM over-voltage deglitch time            | dpdm_ovp_dgl_sel = 0                                   |      | 4     |      | μs |
|                           |  | dpdm_ovp_dgl_sel = 1                                   |      | 40    |      | μs |
| t <sub>DATA_RISING</sub>  | Data output from low to high               |  |      | 0.3   | 1    | μs |
| t <sub>DATA_FALLING</sub> | Data output from high to low               |  |      | 0.3   | 1    | μs |
| t <sub>UI</sub>           | Unit interval time                         |  | 144  | 160   | 176  | μs |



|                       |   |   |       |         |       |             |
|-----------------------|---|---|-------|---------|-------|-------------|
| $t_{PING\_ST}$        | Adapter transmit slave ping duration time       |   | 2304  | 2560    | 2816  | $\mu s$     |
| $t_{PING\_SR}$        | Adapter receive master ping duration            |   | 2304  | 2560    | 2816  | $\mu s$     |
| $t_{PSR}/t_{PST}$     | Ping received and transmit ratio                |   | 99    | 100     | 101   | %           |
| $t_{AD}$              | Terminal attach deglitch                        |   | 450   | 500     | 550   | $\mu s$     |
| $t_{DD}$              | Terminal detach deglitch                        | dp_to_set = 00b   | 0.475 | 0.5     | 0.525 | ms          |
|                       |   | dp_to_set = 01b   | 0.95  | 1       | 1.05  | ms          |
|                       |   | dp_to_set = 10b   | 1.9   | 2       | 2.1   | ms          |
|                       |   | dp_to_set = 11b   | 3.8   | 4       | 4.2   | ms          |
| <b>THERMAL SENSOR</b> |   |   |       |         |       |             |
| $V_{NTC}$             | NTC open loop voltage                           | In NTC mode   |       | 2.248   |       | V           |
| $I_{NTC}$             | External NTC temperature detection bias current | ntc_c_sel = 00b   |       | 100     |       | $\mu A$     |
|                       |   | ntc_c_sel = 01b   |       | 20      |       |             |
|                       |   | ntc_c_sel = 10b   |       | 4       |       |             |
|                       |   | ntc_c_sel = 11b   |       | Disable |       |             |
| $T_{DIE}$             | Internal temperature sensor range               |   | -20   |         | 105   | $^{\circ}C$ |
| $T_{ERR}$             | Thermal sensor error                            |   | -10   |         | 10    | $^{\circ}C$ |
| <b>SYSTEM CLOCK</b>   |   |   |       |         |       |             |
| $f_{HF\_OSC}$         | High frequency OSC                              |   |       | 24      |       | MHz         |
| $f_{LF\_OSC}$         | Low frequency OSC                               |   |       | 500     |       | kHz         |
| <b>GPIO PINS</b>      |   |   |       |         |       |             |
| $V_{IH\_GPIO}$        | Input voltage high threshold                    | VBUS_PWR = 3.3V ~ 21V, measured as VIO                                    |       |         | 1.6   | V           |
| $V_{IL\_GPIO}$        | Input voltage low threshold                     | VBUS_PWR = 3.3V ~ 21V, measured as VIO                                    | 0.5   |         |       | V           |
| $V_{OH\_GPIO}$        | Output high voltage                             | VBUS_PWR = 6V, apply 4mA sink current from IO pin to GND externally       | 4.4   |         |       | V           |
| $V_{OL\_GPIO}$        | Output low voltage                              | VBUS_PWR = 6V, apply 10mA source current from VDD_5V to IO pin externally |       |         | 0.5   | V           |
| $V_{PU}$              | Pull up resistor value at GPIO pin              | VBUS_PWR = 3.3V ~ 21V   |       | 5.6     |       | K $\Omega$  |
| $V_{PD}$              | Pull down resistor value at GPIO pin            | VBUS_PWR = 3.3V ~ 21V   |       | 5.6     |       | K $\Omega$  |



## 8 Detailed Description

### 8.1 Power Supply

SC2151A contains an internal high-voltage LDO which supports wide input range. VBUS\_PWR is the power supply input pin of internal LDO. It converts voltage on VBUS\_PWR to 5V and supplies internal modules.

For applications, VBUS\_MON should be connected to the VBUS on USB port, and VBUS\_PWR should be connected to internal VBUS node.

### 8.2 NMOS Gate Driver

The Type-C and USB PD specifications require the VBUS isolation implementation for the Type-C port. SC2151A provides NMOS gate drive to control the isolation MOSFET between the internal VBUS node and the Type-C port.

The gate drivers are controlled by register bits. The voltage VGS is clamp to 7V. The IC provides 4 different pull-up capabilities from 80kΩ to 300kΩ, and 2 pull-down capabilities at 2kΩ or 15kΩ, so to suit different MOSFETs.

### 8.3 VBUS Discharging Paths

The IC integrates two VBUS discharging paths from VBUS\_MON and VBUS\_PWR pins to ground respectively. The two paths help drain the residual charge on the bulk capacitors to meet the application requirements. The typical equivalent impedance of discharge path on VBUS\_MON pin is 1kΩ. Discharging path on VBUS\_PWR pin is a constant current from 45mA to 150mA, which can be configured by registers. The discharging paths are turned on/off through register settings.

### 8.4 ADC

In the Type-C, USB PD or other quick charge applications, it is necessary to monitor the VBUS voltage and current. The SC2151A integrates a 10-bit Successive Approximation Analog to Digital Converter (SAR ADC) with a reference voltage of 2.248V at a sampling rate of 50kHz.

The ADC supports 7-channel input as below. For VBUS\_MON and VBUS\_PWR, an internal ratio of 1/10 is built in. The ratio of DPDM channel is 1/4.

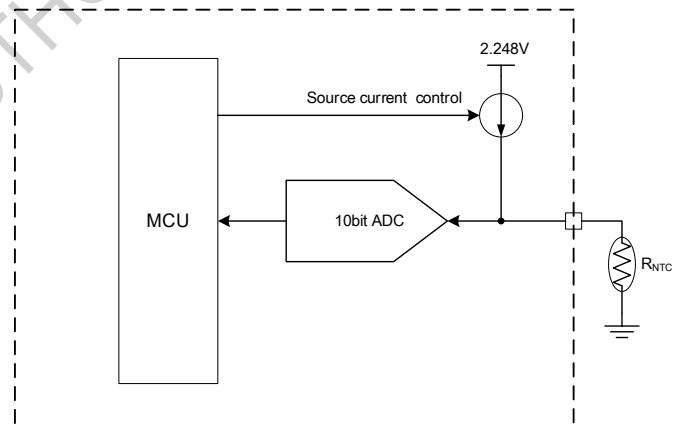
The Internal Temperature Sense (ITS) unit converts the temperature to voltage. Users can get the die temperature by sampling the channel. The ratio of voltage to temperature is 2.819mV/°C and the output of ITS is 733.94mV at the temperature of 27°C.

Table 1. ADC input channel

| ADC_CH_SEL[2:0] | Input Signal     | Note   |
|-----------------|------------------|--|
| 000             | 1/10 x VBUS_PWR  | With 1/10 internal divider                                 |
| 001             | 1/10 x VBUS_MON  | With 1/10 internal divider                                 |
| 010             | VRSNS × 40 or 20 | The gain of current sense amplifier can be set as 40 or 20 |
| 011             | ADC0             |  |
| 100             | ADC4             |  |
| 101             | 1/4 x DP/DM      | With 1/4 internal divider                                  |
| 110             | ITS              | Internal temperature sense                                 |

### 8.5 External Temperature Sense

SC2151A provides two ports to support external temperature sense. As shown in the figure, each of NTC pins source current on the R<sub>NTC</sub>, and the voltage can be sampled by 10-bit ADC. Source current can be configured as 100μA, 20μA or 4μA. The over-temperature protection will be triggered if the voltage is below an over-temperature protection threshold for a programmed time delay.



### 8.6 CV CC Control Loop

SC2151A contains 2 DACs and 2 error amplifiers to regulate output voltage and current. For voltage regulation, VDAC is a 10-bit DAC with internal 2.048V reference voltage. SC2151A supports at least 20mV per step for VBUS output voltage regulation. The adjust time ranges from 20 μs to 250 μs which can be set by firmware.

VBUS output regulation should be as the following equation.

$$V_{REG} = 2 + VDAC\ code * 0.020$$

For example, if VDAC code = 150, the output voltage V<sub>REG</sub> = 5V.



SC2151A integrates a low side current sense amplifier for constant current regulation and output current sampling. The gain of the amplifier can be configured as 40 or 20. For 5mohm application, SC2151A supports up to 5A constant current regulation.

The IDAC is 10-bit with 1.2V reference. The regulation current ( $I_{REG}$ ) is decided by IDAC code, sense resistance ( $R_{SNS}$ ) and the gain of current sense amplifier ( $G_{SNS}$ ). The relationship between these parameters should be as follows.

$$I_{REG} = \frac{IDAC\ code \times 1.2}{(2^{10} \times R_{SNS} \times G_{SNS})}$$

For example, if  $R_{SNS} = 5m\Omega$ ,  $G_{SNS} = 40$ , IDAC code = 512,  $I_{REG} = 3A$ .

## 8.7 DPDM Interface

The SC2151A integrates DPDM interface which can be configured as discharging out port (provider). The DPDM interfaces is available for USB-A port applications or Type-C port applications. It supports Apple-2.4A, BC1.2 DCP, HVDCP, FCP, SCP, VOOC and other proprietary fast charging protocols.

DP and DM pins can be configured flexible for different applications. SC2151 supports Apple-2.4A mode, which broadcasts 2.7V voltage on both DP and DM pins with 30kohm output impedance. If 2.4A mode advertisement on DPDM is enabled, it is recommended that VBUS should be able to supply at least 2.4A of current.

SC2151A can be also configured as a dedicated charging port (DCP), which complies with the BC1.2 specification. When DCP mode is enabled, SC2151 shorts DP and DM pin through a 20ohm resistor.

## 8.8 CC Interface

SC2151A can be configured as source only. It presents  $R_p$  on CC1 and CC2, waiting for a sink to attach and pull down the voltage on the pin. Once an attachment is detected, SC2151A will apply VBUS voltage and broadcast source capabilities.

Current source presented on CC can be configured to 330 $\mu$ A, 180 $\mu$ A and 80 $\mu$ A. Each of the CC pins contains comparators to decide CC\_RD and CC\_RA attachment.

### 8.8.1 VCONN Switch

SC2151 contains VCONN switch for powering e-marker. If an e-marker cable is attached, CC\_RA can be detected by comparator on CC pin. VCONN switch can be turned on by

firmware to supply the e-marker through CC line. SC2151 can supply up to 70mA output capability.

When VCONN switch is turned on, SC2151 will continuously monitor current on CC pin. If VCONN output current is above 70mA, VCONN over-current flag will be set, and VCONN switch can be turned off by firmware. SC2151 supports reverse current protection on VCONN switch to avoid damage if CC pin is short to VBUS.

## 8.9 USB PD Protocol

SC2151A provides USB PD physical layer for PD protocol communication. Once the insertion direction of TYPE-C port is detected by CC comparator, SC2151A can select either CC1 or CC2 channels to send and receive PD packets. The firmware controls the PD packets.

## 8.10 Protections

### 8.10.1 OVP, UVP and SCP

The SC2151A monitors the VBUS voltage in real time. Once the voltage exceeds the OVP threshold for a programmed time, the OVP flag is set and interrupt is generated automatically. It also monitors VBUS voltage for under-voltage protection (UVP). Once VBUS voltage drops below UVP threshold for a programmed time, the UVP flag is set and an interrupt is generated. Once voltage on VBUS drops below 3.2V, Short-Circuit Protection (SCP) will be triggered. An interrupt will be generated and the SCP flag will be set.

The OVP threshold, UVP threshold and the detection deglitch time can be configured through registers. The OVP threshold can be configured as 110%, 115% and 120% of the setting voltage. The deglitch time can be configured as 4 $\mu$ s or 40 $\mu$ s.

### 8.10.2 Protection for DPDM

The IC supports over-voltage protection of the DP/DM pin. Once it detects any of the DP and DM voltage exceeding 4.75V, the IC will report the over-voltage status and generate an interrupt.

### 8.10.3 Protection for CC

SC2151A continuously monitors CC voltage. Once CC over-voltage detected, SC2151A will launch CC Over-Voltage Protection (CC OVP). The CCOVP flag will be set if the voltage on CC1 or CC2 is over 7.2V and will be clear after voltage falls below 7V. The OVP interrupt will be triggered if interrupt enable control bit is set.



If each of the protections including OVP, UVP, SCP, DPDMOVP and CCOVP is detected, SC2151A can drive isolation MOS off by register setting.

## 8.11 MCU Controller

### 8.11.1 Clock

The SC2151A integrates a 24MHz high frequency clock and a 500kHz low frequency clock. Under normal working condition, high frequency and low frequency clocks work simultaneously. When in sleep mode, only the 500kHz clock works to reduce the power consumption.

### 8.11.2 Modes

The SC2151A supports three operating modes: active mode, standby mode and sleep mode. In active mode, each function module operates normally. In standby mode, MCU stops, each module can be turned on and MCU restarts once any of the interrupts is triggered. In sleep mode, only the 500kHz low frequency clock works, and all other functions are turned off. The quiescent current can be as low as 400  $\mu$ A in sleep mode.

After entering sleep mode, the system can be awakened by interruptions, including GPIO interrupts, DPDM interrupts, watchdog interrupts, and the timer interrupts with the 500kHz clock source.

### 8.11.3 GPIO

GPIO has input/output direction settings, internal pull-up/pull-down resistor settings, and interrupt edge settings. Please see register map for details.

### 8.11.4 Interrupts

The IC supports various interrupts, including Timer0 interrupt, ADC interrupt, I2C interrupts, DPDM interrupts, analog interrupts, WDT interrupt, IOx interrupt.

### 8.11.5 Timer

The SC2151A integrates one general timer. The clock source can be configured as 24MHz high frequency oscillator or 500kHz low frequency oscillator.

The timer is a count-up counter, counting cycle and clock can be configured by registers. Overflow flag will be set and interrupt will be generated once timer0 counts to the end of cycle.

### 8.11.6 UART

UART can support Tx function and Rx function. The baud rate can be set from 9600 bit/s to 921600 bit/s.

### 8.11.7 I2C

The SC2151A contains one I2C interface which can be configured as a master interface and a slave interface. The I2C slave address is (0x84/0x85).

### 8.11.8 Watchdog

The watchdog is a 16-bit counter with 1000Hz clock source (divided from 500kHz clock). Once the watchdog is enabled, the watchdog counter starts with the value of zero and counts up. The control register WDT\_CTRL can be used to select whether an interrupt or reset signal, or both occurs when the counter overflows (counting to WDT\_INIT).

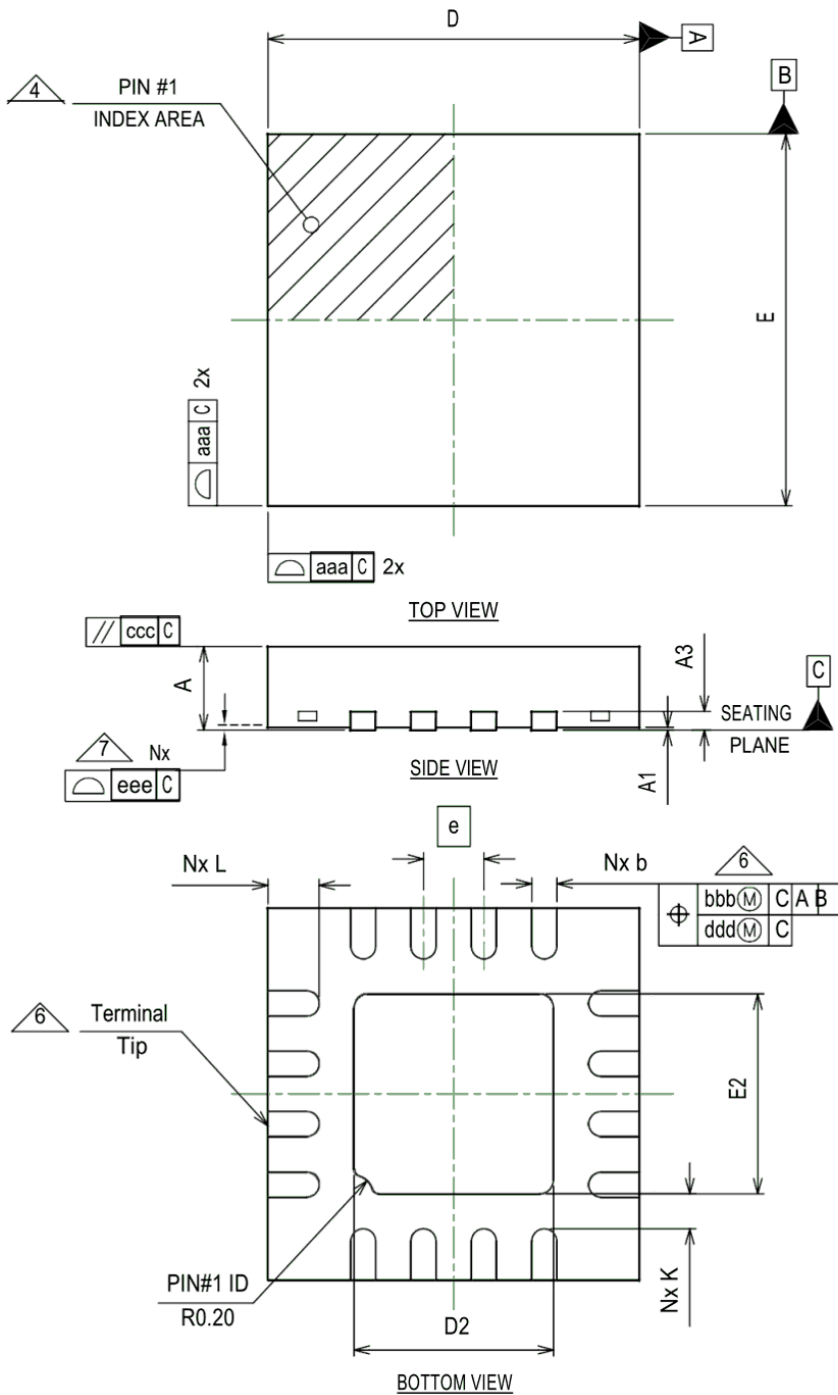
### 8.11.9 Programming

The SC2151A can be programmed through I2C interface.



PACKAGE

QFN-16 0404 x 0.75



| Thickness Symbol | W        |          |         |
|------------------|----------|----------|---------|
|                  | MINIMUM  | NOMINAL  | MAXIMUM |
| A                | 0.70     | 0.75     | 0.80    |
| A1               | 0.00     | 0.02     | 0.05    |
| A3               | ---      | 0.20 Ref | ---     |
| b                | 0.25     | 0.30     | 0.35    |
| D                | 3.95     | 4.00     | 4.05    |
| E                | 3.95     | 4.00     | 4.05    |
| e                | 0.65 BSC |          |         |
| D2               | 2.00     | 2.15     | 2.25    |
| E2               | 2.00     | 2.15     | 2.25    |
| K                | 0.20     | ---      | ---     |
| L                | 0.45     | 0.55     | 0.65    |
| aaa              | 0.05     |          |         |
| bbb              | 0.10     |          |         |
| ccc              | 0.10     |          |         |
| ddd              | 0.05     |          |         |
| eee              | 0.08     |          |         |
| N                | 16       |          |         |
| ND               | 4        |          |         |
| NE               | 4        |          |         |