SC2315(文件编号：S&CIC0382) 2-Channel Audio Processor IC

Description

SC2315 is a two-channel digital audio processor utilizing CMOS Technology. Volume, Bass, Treble and Balance Controls are incorporated into a single chip. Loudness Function is also provided to build a highly effective electronic audio processor having the highest performance and reliability with the least external components. All functions are programmable using the I^2C Bus. The pin assignments and application circuit are optimised for easy PCB layout and cost saving advantage for audio application. Housed in a 20-pin DIP/SO Package, SC2315 is pin-to-pin compatible with TDA7315 and is very similar in performance with the later.

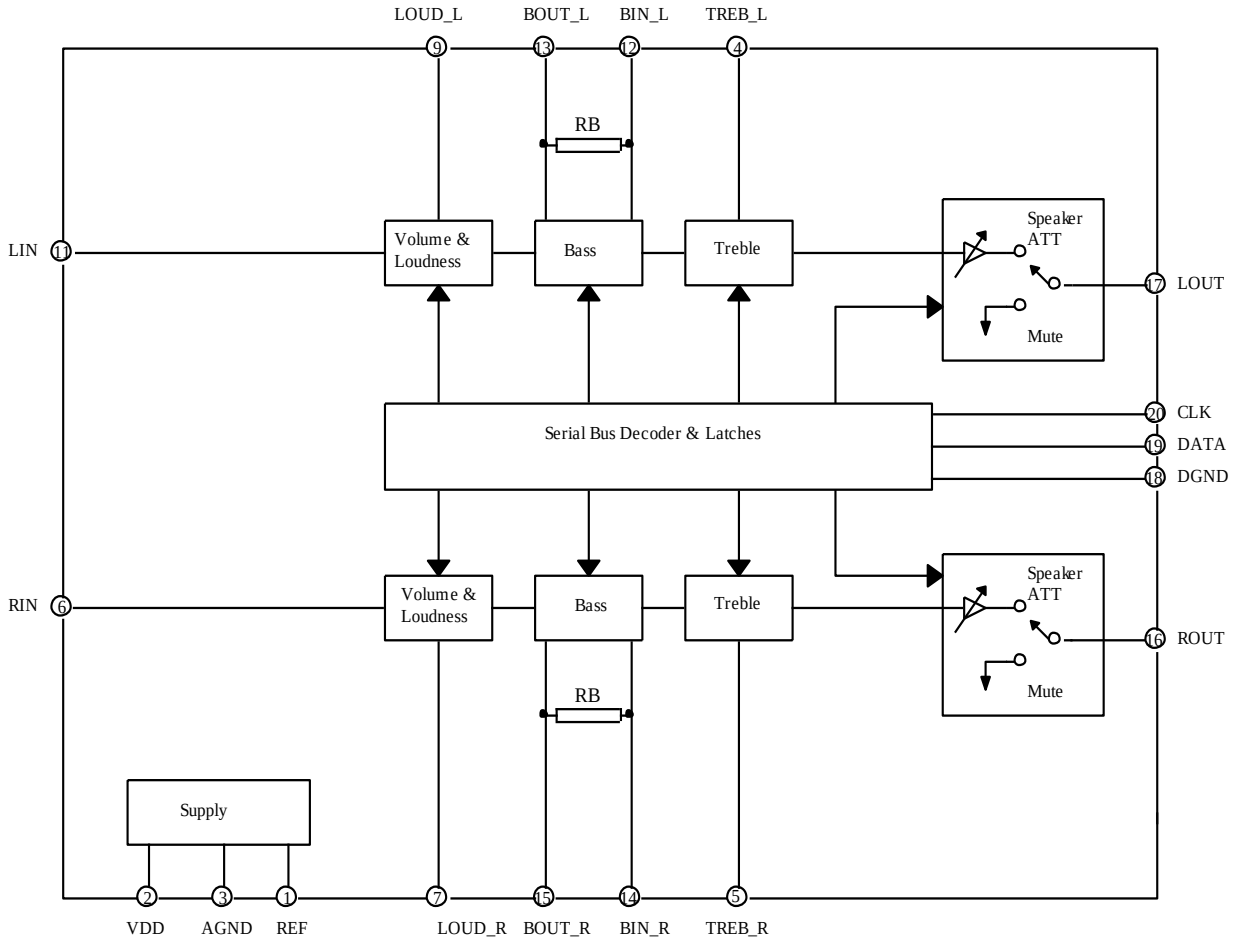
Features

- CMOS Technology
- Least External Components
- Treble and Bass Control
- Loudness Function
- Input/Output for External Noise Reduction System/Equalizer
- 2 Independent Speaker Controls for Balance Function
- Independent Mute Function
- Volume Control in 1.25 dB/step
- Low Distortion
- Low Noise and DC Stepping
- Controlled by I^2C Bus Micro-Process
- Pin-to-pin Compatible with TDA7315

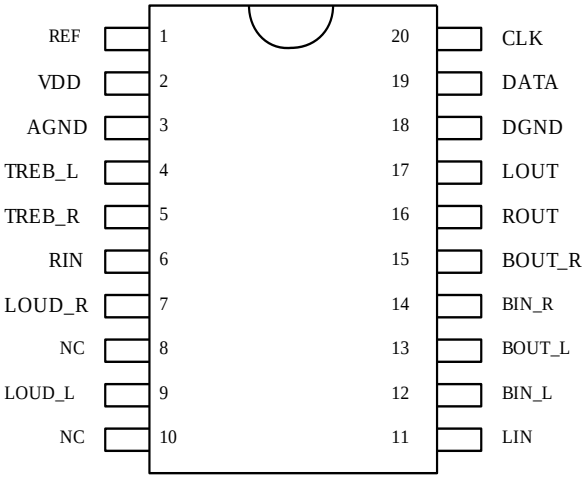
Application

- Car Stereo (Audio)
- Hi-Fi Audio System
- Can be used in all I^2C System Application

Block Diagram



Pin Configuration



Pin Description

Pin No.	Pin Name	I/O	Description
1	REF	-	Analog Reference Voltage (1/2 VDD
2	VDD	-	Supply Input Voltage
3	AGND	-	Analog Ground
4	TREB_L	I	Left Channel Input for Treble Controller
5	TREB_R	I	Right Channel Input for Treble Controller
6	RIN	I	Audio Processor Right Channel Input
7	LOUD_R	I	Right Channel Loudness Input
9	LOUD_L	I	Left Channel Loudness Input
11	LIN	I	Audio Processor Left Channel Input
12	BIN_L	I	Left Bass Controller Input Channel
13	BOUT_L	O	Left Bass Controller Output Channel
14	BIN_R	I	Right Channel Input for Bass Controller
15	BOUT_R	O	Right Channel Output for Bass Controller
16	ROUT	O	Right Speaker Output
17	LOUT	O	Left Speaker Output
18	DGND	-	Digital Ground
19	DATA	I	Control Data Input
20	CLK	I	Clock Input for Serial Data Transm ission
8,10	NC	-	No Connection

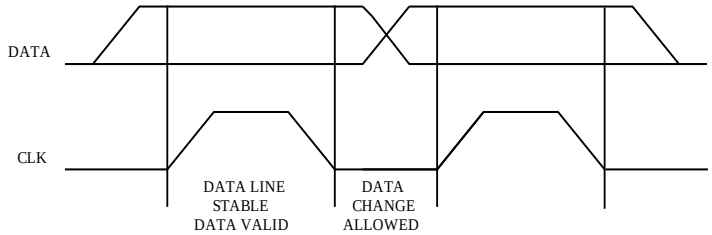
Functional Description

I^2C Bus Interface

Data are transmitted to and from the microprocessor to the SC2315 via the DATA and CLK. The DATA and CLK make up the BUS Interface

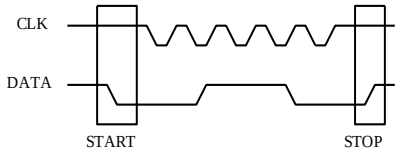
Data Validity

A data on the DATA Line is considered valid and stable only when the CLK Signal is in HIGH state. The HIGH and LOW State of the DATA Line can only change when the CLK signal is LOW. Please refer to the figure below.



Start and Stop Conditions

A Start Condition is activated when 1) the CLK is set to HIGH and 2) DATA shifts from HIGH to LOW State. The Stop Condition is activated when 1) CLK is set to HIGH and 2) DATA shifts from LOW to HIGH State. Please refer to the timing diagram below.



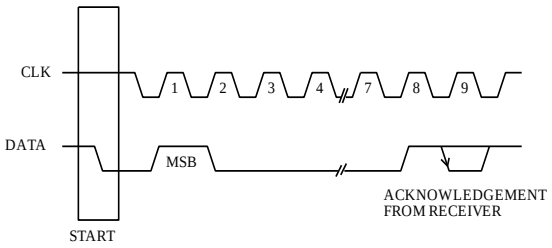
Byte Format

Every byte transmitted to the DATA Line consist of 8 bits. Each byte must be followed by and Acknowledge Bite. The MSB is transmitted first.

Acknowledge

During the Achnowledge Clock Pulse, the master (μ P) puts a resistive HIGH level on the DATA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the DATA line during the Acknowledge Clock Pulse so that the DATA Line is in a Stable Low State during this Clock Pulse.

Please refer to the diagram below.



The audio processor that has been addressed has to generate an acknowledge after receiving each byte, otherwise, the DATA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

Transmission without Acknowledge

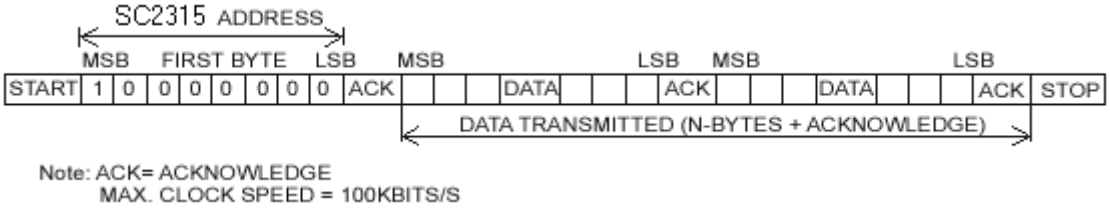
If you want to avoid the acknowledge detection of the audio processor, a simpler μ P transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are gteater chances of faulty operation as well as decrease in noise immunity.

Interface Protocol

The interface protocol consists of the following:

- A Start Condition
- A Chip Address Byte including the SC2315 address. The 8th Bit of the Byte must be “0”.
- A Data Sequence (N-Bytes + Acknowledge)
- A Stop Condition

Please refer to the diagram below:



Software Specification

SC2315 Address

SC2315 Address is shown below:

1 MSB	0	0	0	0	0	0	0 LSB

Data Bytes

MSB							**LSB**	**FUNCTION**
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	0	0	B1	B0	A2	A1	A0	Speaker ATT L
1	0	1	B1	B0	A2	A1	A0	Speaker ATT R
0	1	0	*	*	L	*	*	Loudness Control
0	1	1	0	C3	C2	C1	C0	Bass Control
0	1	1	1	C3	C2	C1	C0	Treble Control

Where Ax=1.25 dB steps; Bx=10dB steps; Cx=2dB steps; *=no effect

Volume

The table below gives a detailed description of the Volume Data Bytes. For example, a volume of –37.5 dB is given by 00011110.

MSB							LSB	功能
0	0	B2	B1	B0	A2	A1	A0	Volume1.25dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

Speaker Attenuators

The table below gives a detailed description of the speaker attenuators data bytes. For example, an attenuation of 30dB on the Speaker L(Left) is given by: 10011000.

MSB							LSB	Function
1	0	0	B1	B0	A2	A1	A0	Speaker L
1	0	1	B1	B0	A2	A1	A0	Speaker R
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

Loudness Function

The following table shows the detailed description of the Loudness Function. For example, when the Loudness Function is turned ON, the format is – 01000000

MSB							LSB	Function
0	1	0	*	*	L	*	*	Loudness Control
					0			Loudness ON
					1			Loudness OFF

Note: *=No Effect

Bass and Treble Data Bytes

The following table shows a detailed description of the Bass and Treble Data Byte. For example a Treble at –12dB is given by: 01110001.

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

Unit:dB

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
Vs	Operating Supply Voltage	10.5	V
Tamb	Operating Ambient Temperature	-20 to 75	℃
Tstg	Storage Temperature Range	-40 to +125	℃

Quick Reference Data

Symbol	Parameter	Min	Typ	Max	Unit
Vs	Supply Voltage	6	9	10	V
V_{CL}	Max. Input Signal Handing	2	2.5		Vrms
THD	Total harmonic Distortion (V=1Vrms, f=1KHz)		0.03	0.07	%
S/M	Signal to Noise ratio		95		dB
Sc	Channel Separation (f=1KHz)		85		dB
	Volume Control 1.25dB setp	-75		0	dB
	Bass & Treble Control 2dB setp	-14		+14	dB
	Balance Control 1.25dB setp	-37.5		0	dB
	Mute Attenuation		95		dB

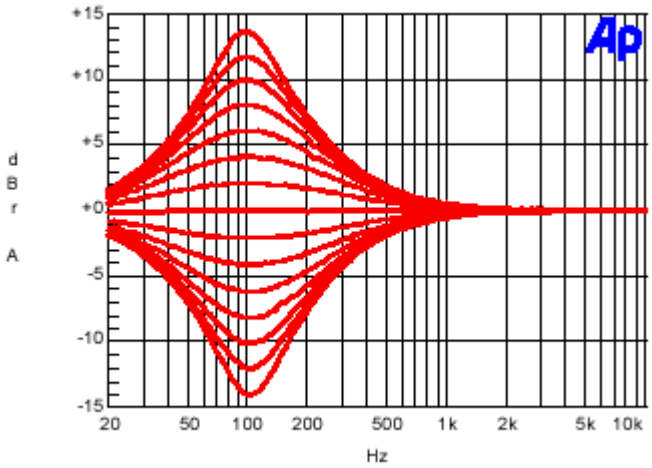
Electrical Characteristics

(Unless specified: Tamb=25℃, Vc=9V, RL=100KΩ, Rg=600Ω, all controls flat (G=0), f=1KHz)

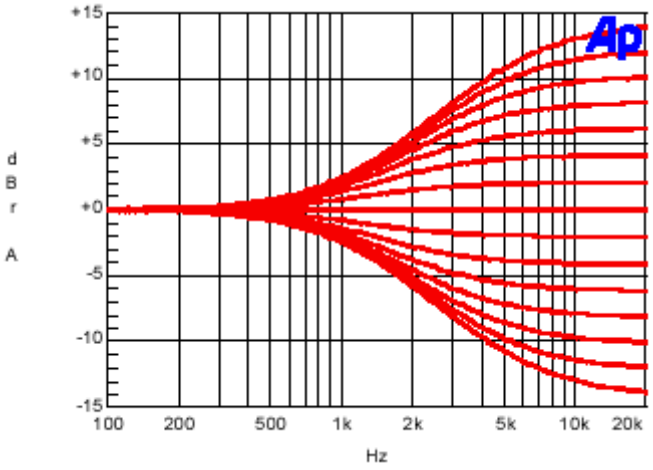
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply						
V_{CC}	Supply Voltage		6	9	10	V
Is	Supply Current			30	40	mA
Volume Control						
R_{IV}	Input Resistance		15	25	35	KΩ
C_{RANGE}	Control Range		70	75	80	dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation		70	75	80	dB
A_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation Set Error	AV=0 to –20dB AV=-20 to -60dB	-1.25 -3.0	0	1.25 2	dB dB
Speaker Attenuators						
C_{RANGE}	Control Range		35	37.5	40	dB
S_{STEP}	Step Resolution		0.5	1.25	1.5	dB
E_A	Attenuation Set Error				1.5	dB
A_{MUTE}	Output Mute Attenuation		90	95		dB
Bass Control(1)						
Gb	Control Range	Max. Boost/Cut	±12	±14	±16	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		40	50	60	KΩ

Treble Control (1)						
Gt	Control Range	Max. Boost/Cut	±13	±14	±15	dB
T_{STEP}	Step Resolution		1	2	3	dB
Audio Outputs						
V_{OCL}	Clipping Level	d=0.3%	2	2.5		Vrms
R_{OUT}	Output Resistance		-	40	45	Ω
V_{OUT}	DC Voltage Level		4.2	4.5	4.8	V
R_L	Load Impedance		10			K Ω
General						
e_{NO}	Output Noise	BW=20-20KHz, flat Output Muted All gains=0dB		 -100 -95		 dBV dBV
		A Curve All Gains=0dB		-98		dBV
S/N	Signal to Noise Ratio	All Gains=0dB Vo=1Vrms		95		dB
d	Distortion	AV=0, VIN=1Vrms AV=0dB, VIN=0.2Vrims		0.03 0.03	0.07 0.05	% %
Sc	Channel Separation Left/Right		80	90		dB
Bus Inputs						
VIL	Input Low Voltage				1	V
VIH	Input High Voltage		3			V
VIN	Input Current		-5		+5	uA
VO	Output Voltage SDA Acknowledge	Io=1.6mA			0.4	V

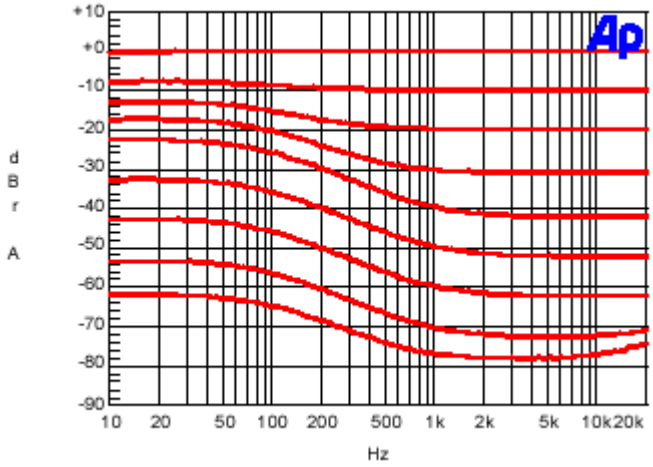
Note: (1) For the Bass and Treble Response, please refer to the diagram below. The center frequency and quality of the resonance behavior can be selected by the external circuitry. A standard first order bass response can realized by a standard feedback network..



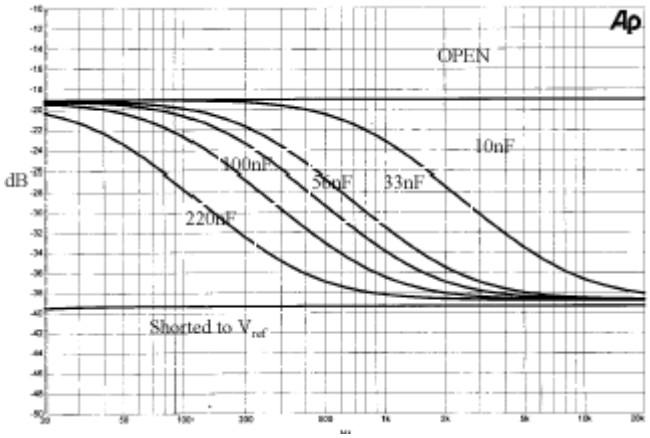
Bass Control



Treble Control

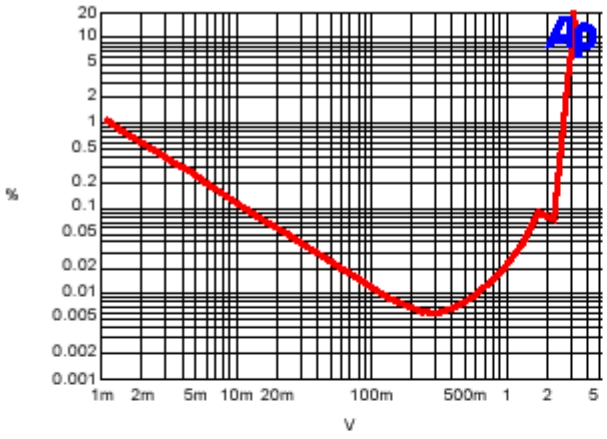


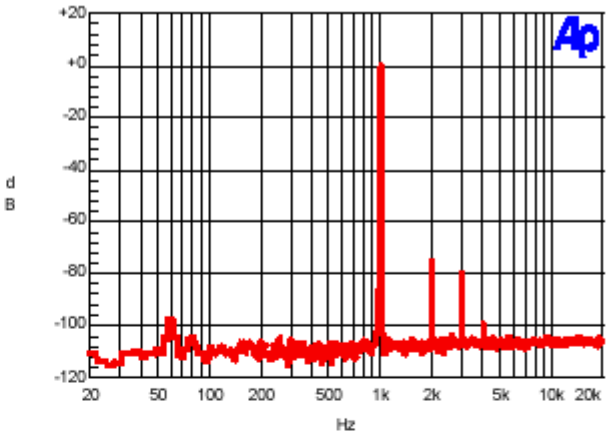
Volume control with loudness



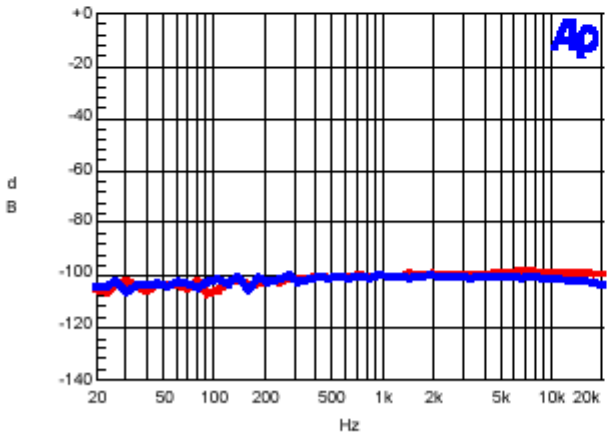
SC2315 C10, C11 对响度的频率响应图(Volume=-40dB, All other control flat)

Electrical Characteristic Diagrams



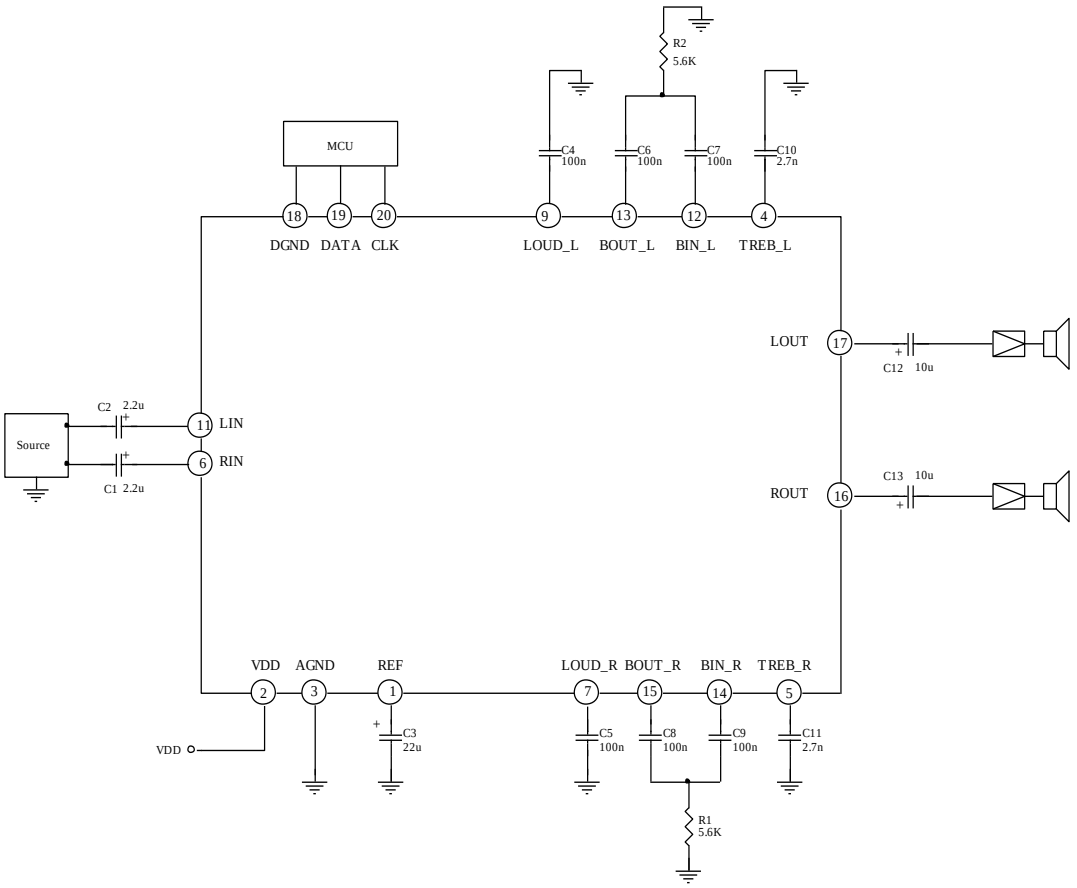


Total Harmonic Distortion and Amplitude 1vrms Output FFT Analysis



Left and Right Channel Crosstalk

Application Circuit

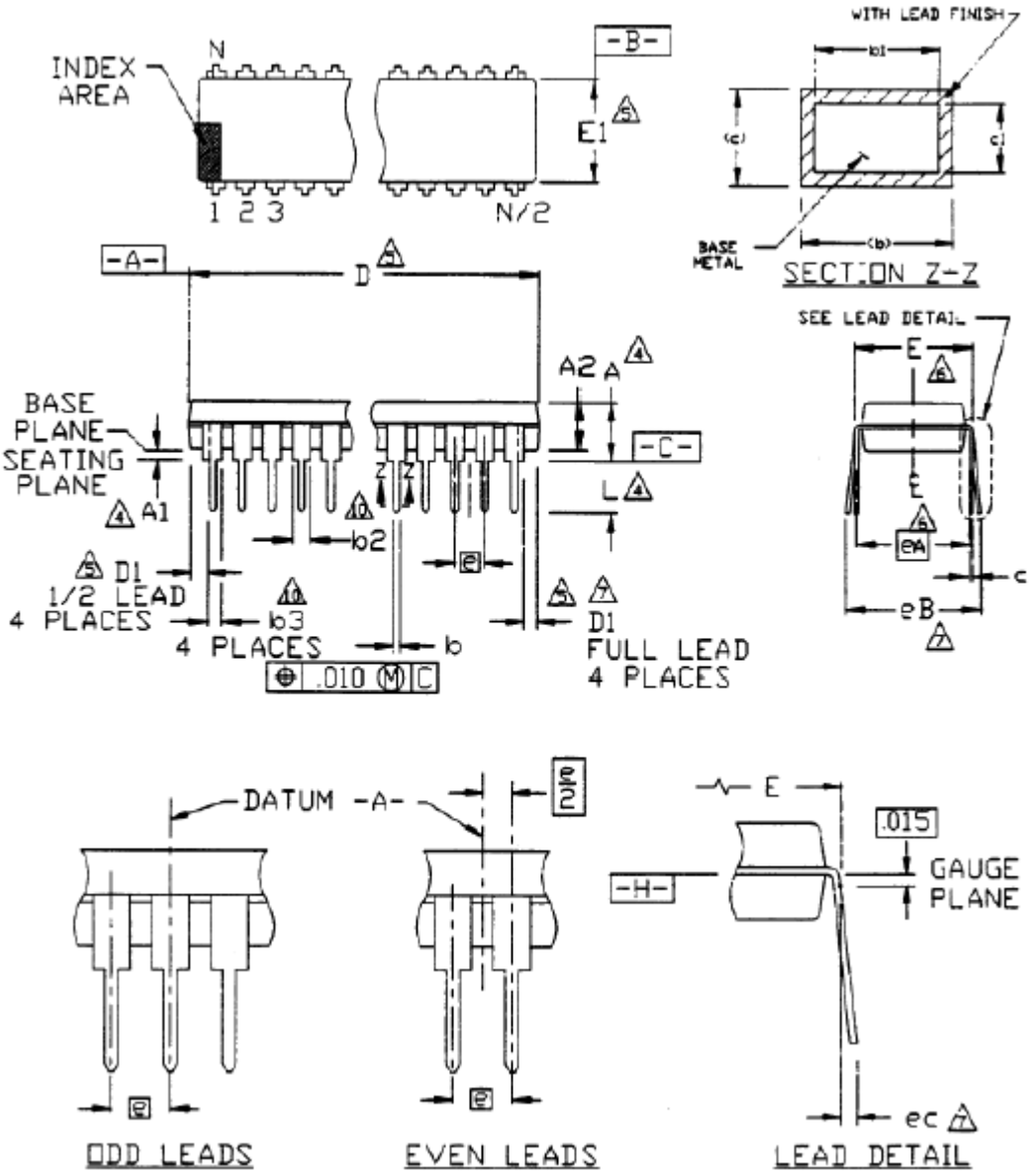


Order Information

Valid Part Number	Package Type	Top Code
SC2314	20 Pins，SO Package（300mil）	SC2314
SC2314-D	20 Pins， DI Package（300mil）	SC2314-D

Package Information

20 Pins, DIP Package (300mil)



Symbol	Dimensions in Inches		
	Min.	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.980	-1.030	1.060
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 BSC		
eA	0.300 BSC		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

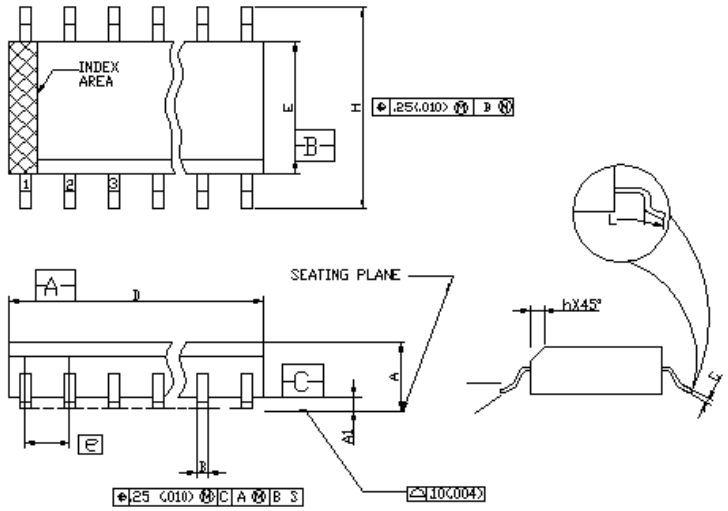
Notes:

1. All dimensions are in INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension A, “A1” and “L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. “D”, “D1”, and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. E and “eA” measured with the leads constrained to be perpendicular to datum -C-.
6. “eB” and “eC” are measured at the lead tips with the leads constrained.
7. “N” is the number of terminal positions (N=16)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. “b2” and “b3” maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010” (0.25mm).
10. Distance between leads including dambar protrusions to be 0.005 inch minimum.
11. Datum plane -H- coincident with the bottom of lead where lead exits body.
12. Refer to JEDEC MS-001 Variation AD.

JEDEC is the registered trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

SC2315(文件编号：S&CIC0382) 2-Channel Audio Processor IC

20 Pins, SO Package (300mil)



Symbol	Min	Nom	Max
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	12.60		13.00
E	7.40		7.60
e		1.27 bsc	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
α	0°		8°

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusion shall not exceed 025mm (0.010 in) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of terminal for soldering to a substrate.
6. N is the number of terminal positions (N=20).
7. The lead width B as measured 0.36mm (0.014in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension: MILLIMETER
9. Refer to JEDEC MS-013 Variation AC.

JEDEC is the registered trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION