

### POWER MANAGEMENT

#### Description

The SC2447 is a versatile high-frequency dual phase PWM step-down controller optimized for Philips and Renesas DrMOS™. Both phases are capable of sourcing or sinking load currents, making the SC2447 suitable for networking system power and DDR applications.

The SC2447 employs fixed frequency, continuous-conduction peak current-mode control for easy compensation and fast transient response.

The SC2447 can be used to generate two independent outputs (up to 30A per output) or a single 60A output with shared phase current. The PWM signals are 180° out of phase to minimize input/output ripple.

Either inductor DC resistance or precision sense resistor can be used for current-mode control. Inductor DC resistance sensing has the advantage of being lossless.

Each phase has individual closed-loop soft-start and overload shutdown timer. The SC2447 powers up neatly with pre-biased output. It has tri-state shutdown and hiccup overload protection. In two-phase single-output configuration, the master timer controls the soft-start and overload shutdown functions. The SC2447 is in a lead-free, WEEE and RoHS compliant, TSSOP-28 package.

#### Features

- ◆ 2-Phase Step-down Controller optimized for Philips or Renesas DrMOS™
- ◆ Out of Phase Operation for Low Input Current Ripple
- ◆ Outputs Source and Sink Current
- ◆ Fixed Frequency Peak Current-Mode Control
- ◆ Lossless Inductor DCR Current Sensing
- ◆ Optional Resistor Current-Sensing for Precise Current-Limit
- ◆ Dual 30A Outputs or 2-Phase 60A Single Output Operation
- ◆ Wide Input Voltage Range: 4.65V to 15V
- ◆ Individual Closed-Loop Soft-Start, Overload Shutdown Timer and Enable
- ◆ Output Voltage as Low as 0.5V
- ◆ Starts into Pre-Bias Output
- ◆ Tri-State PWM Output during Shutdown
- ◆ Programmable Frequency Up to 1MHz Per Phase
- ◆ External Synchronization
- ◆ TSSOP-28 Lead-free Package. Fully WEEE and RoHS Compliant

#### Applications

- ◆ Telecommunication Power Supplies
- ◆ DDR Memory Power Supplies
- ◆ Graphic Power Supplies
- ◆ Servers and Base Stations

#### Typical Application Circuit

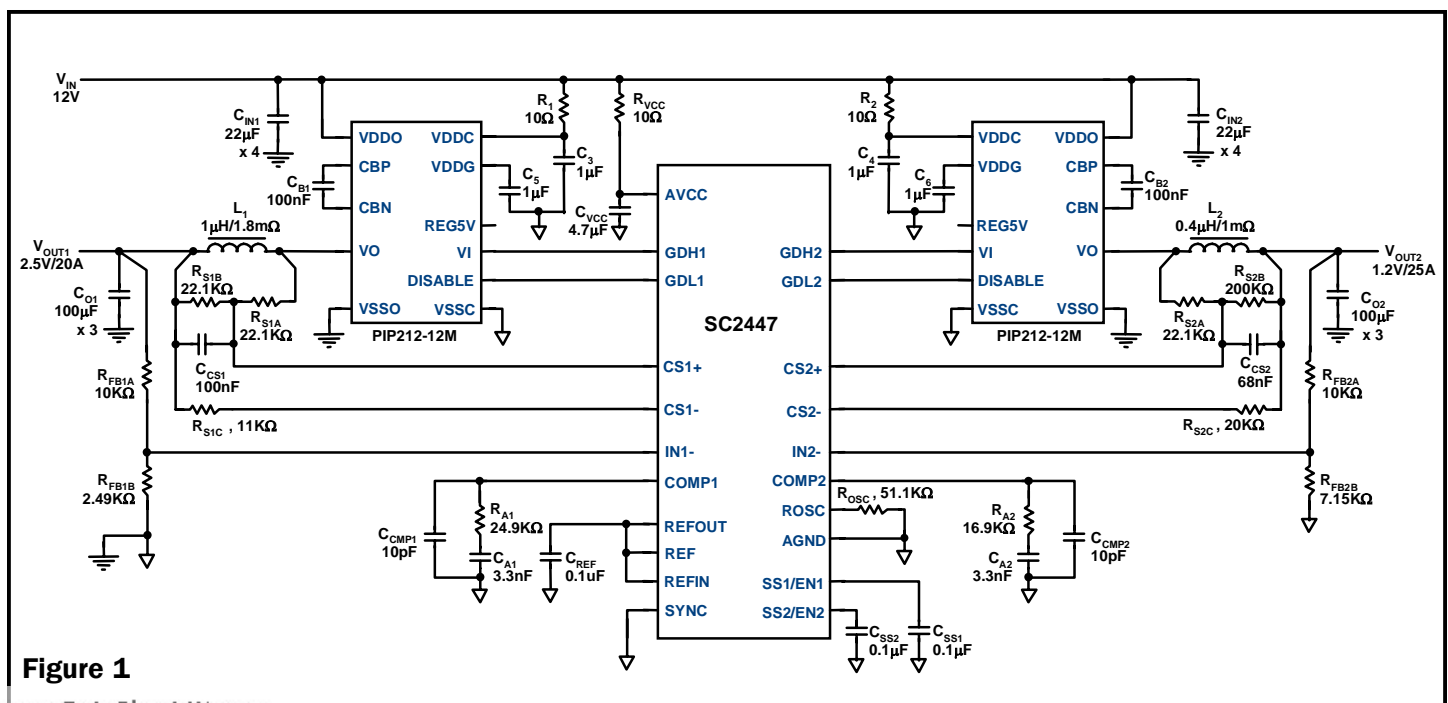
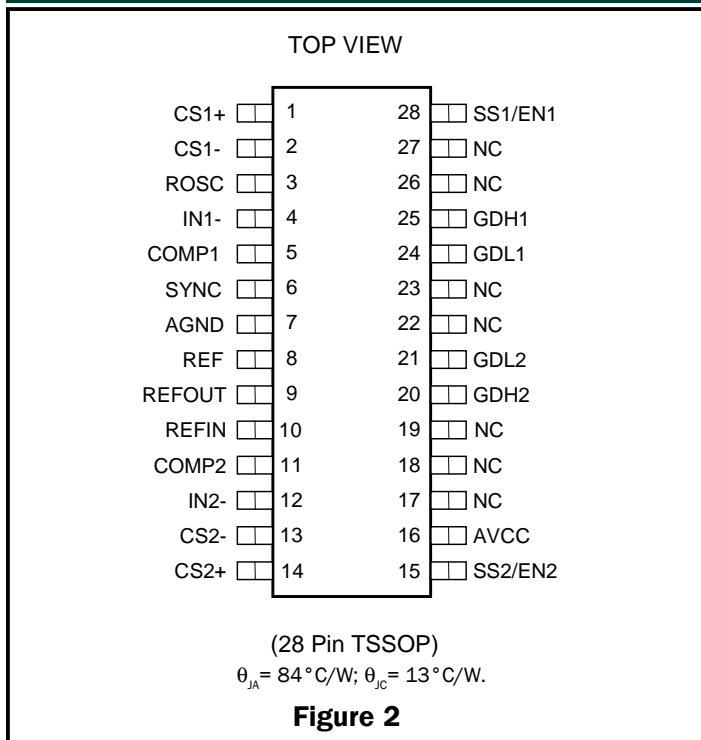


Figure 1

**POWER MANAGEMENT**
**Pin Configurations**

**Ordering Information**

Device	Top Mark	Package
SC2447TSTRT <sup>(1)(2)</sup>	SC2447	TSSOP-28
SC2447EVB	Evaluation Board	

**Notes:**

(1) Only available in tape and reel packaging. A reel contains 2500 devices for TSSOP package.

(2) Lead free product. This product is fully WEEE and RoHS compliant.

**Absolute Maximum Rating**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum Ratings	Units
Supply Voltage	AVCC	-0.3 to 16	V
Gate Outputs GDH1, GDH2, GDL1, GDL2 voltages	$V_{GDH1}, V_{GDH2}, V_{GDL1}, V_{GDL2}$	-0.3 to 6	V
IN1-, IN2- Voltages	$V_{IN1-}, V_{IN2-}$	-0.3 to AVCC+0.3	V
REF <sub>OUT</sub> Voltages	$V_{REF}, V_{REFOUT}$	-0.3 to 6	V
REF, REF <sub>IN</sub> Voltage	$V_{REFIN}$	-0.3 to AVCC+0.3	V
COMP1, COMP2 Voltages	$V_{COMP1}, V_{COMP2}$	-0.3 to AVCC+0.3	V
CS1+, CS1-, CS2+ and CS2- Voltages	$V_{CS1+}, V_{CS1-}, V_{CS2+}, V_{CS2-}$	-0.3 to AVCC+0.3	V
SYNC Voltage	$V_{SYNC}$	-0.3 to AVCC+0.3	V
SS1/EN1 AND SS2/EN2 Voltages	$V_{SS1}, V_{SS2}$	-0.3 to 6	V
Storage Temperature Range	$T_{STG}$	-60 to 150	°C
Lead Temperature (Soldering) 10 sec	$T_{LEAD}$	260	°C
Junction Temperature	$T_J$	150	°C
ESD Rating (Human Body Model)	ESD	2	kV

**POWER MANAGEMENT**
**Recommended Operating Conditions**

The performance is not guaranteed if exceeding the specifications below.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AVCC Operating Voltage	AVCC		4.65		15	V
Ambient temperature Range	$T_A$		-40		85	°C
Junction Temperature Range	$T_J$		-40		125	°C

**Electrical Characteristics**

 Unless specified: AVCC = 12V, SYNC = 0,  $R_{osc} = 51.1k\Omega$ ,  $-40^\circ C < T_A = T_J < 125^\circ C$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Undervoltage Lockout</b>						
AVCC Start Threshold	$AVCC_{TH}$	AVCC Increasing		4.50	4.65	V
AVCC Start Hysteresis	$AVCC_{HYST}$			0.2		V
AVCC Operating Current	$I_{CC}$	AVCC = 12V		8	15	mA
AVCC Quiescent Current in UVLO		$AVCC = AVCC_{TH} - 0.2V$		2.5		mA
<b>Channel 1 Error Amplifier</b>						
Input Common-Mode Voltage Range <sup>(1)</sup>			0		3	V
Inverting Input Voltage Range <sup>(1)</sup>			0		AVCC	V
Input Offset Voltage		0 ~ 70°C		±1	±3	mV
Non-Inverting Input Bias Current	$I_{REF}$			-100	-250	nA
Inverting Input Bias Current	$I_{IN1-}$			-100	-250	nA
Amplifier Transconductance	$G_{M1}$			170		$\mu\Omega^{-1}$
Amplifier Open-Loop Gain	$a_{OL1}$			65		dB
Amplifier Unity Gain Bandwidth <sup>(1)</sup>				5		MHz
Minimum COMP1 Switching Threshold		$V_{CS1+} = V_{CS1-} = 0$ Increasing $V_{SS1}$		1.7		V
Amplifier Output Sink Current		$V_{IN1-} = 1V, V_{COMP1} = 2.5V$		11		$\mu A$
Amplifier Output Source Current		$V_{IN1-} = 0, V_{COMP1} = 2.5V$		8.5		$\mu A$
<b>Channel 2 Error Amplifier</b>						
Input Common-mode Voltage Range <sup>(1)</sup>			0		3	V
Inverting Input Voltage Range <sup>(1)</sup>			0		AVCC	V
Input Offset Voltage		0 ~ 70°C		±1	±3	mV

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

 Unless specified: AVCC = 12V, SYNC = 0, R<sub>osc</sub> = 51.1kΩ, -40°C < T<sub>A</sub> = T<sub>J</sub> < 125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Non-inverting Input Bias Current	I <sub>REFIN</sub>			-100	-250	nA
Inverting Input Bias Current	I <sub>IN2-</sub>			-150	-380	nA
Inverting Input Voltage for 2-Phase Single Output Operation			2.5			V
Amplifier Transconductance	G <sub>M2</sub>			170		μΩ <sup>-1</sup>
Amplifier Open-Loop Gain	a <sub>OL2</sub>			65		dB
Amplifier Unity Gain Bandwidth <sup>(1)</sup>				5		MHz
Minimum COMP2 Switching Threshold		V <sub>CS2+</sub> = V <sub>CS2-</sub> = 0 V <sub>SS2</sub> Increasing		1.7		V
Amplifier Output Sink Current		V <sub>COMP2</sub> = 2.5V		11		μA
Amplifier Output Source Current		V <sub>COMP2</sub> = 2.5V		8.5		μA
<b>Oscillator</b>						
Channel Frequency	f <sub>CH1</sub> , f <sub>CH2</sub>	0 ~ 70°C	450	500	550	kHz
Synchronizing Frequency <sup>(1)</sup>			2.1f <sub>CH</sub>			kHz
SYNC Input High Voltage			1.5			V
SYNC Input Low Voltage					0.5	V
SYNC Input Current	I <sub>SYNC</sub>	V <sub>SYNC</sub> = 0.2V V <sub>SYNC</sub> = 2V			1 50	μA
Channel Maximum Duty Cycle	D <sub>MAX1</sub> , D <sub>MAX2</sub>			88		%
Channel Minimum Duty Cycle	D <sub>MIN1</sub> , D <sub>MIN2</sub>				0	%
<b>Current-limit Comparators</b>						
Input Common-Mode Range			0		AVCC - 1.5	V
Cycle-by-cycle Peak Current Limit	V <sub>ILIM1+</sub> , V <sub>ILIM2+</sub>	V <sub>CS1-</sub> = V <sub>CS2-</sub> = 0.5V, Sourcing Mode, 0 ~ 70°C	42.5	50	57.5	mV
Positive Current-Sense Input Bias Current	I <sub>CS1+</sub> , I <sub>CS2+</sub>	V <sub>CS1+</sub> = V <sub>CS1-</sub> = 0 V <sub>CS2-</sub> = V <sub>CS2+</sub> = 0		-0.7	-2	μA
Negative Current-Sense Input Bias Current	I <sub>CS1-</sub> , I <sub>CS2-</sub>	V <sub>CS1+</sub> = V <sub>CS1-</sub> = 0 V <sub>CS2+</sub> = V <sub>CS2-</sub> = 0		-0.7	-2	μA
<b>PWM Outputs</b>						
Peak Source Current	G <sub>DL1+</sub> , G <sub>DL2</sub> , G <sub>DH1+</sub> , G <sub>DH2</sub>	AVCC = 12V		10		mA
Peak Sink Current	G <sub>DL1+</sub> , G <sub>DL2</sub> , G <sub>DH1+</sub> , G <sub>DH2</sub>	AVCC = 12V		8		mA

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

 Unless specified: AVCC = 12V, SYNC = 0, R<sub>osc</sub> = 51.1kΩ, -40°C < T<sub>A</sub> = T<sub>J</sub> < 125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage		Source I <sub>o</sub> = 1.2mA, 0 ~ 70°C	4.1		5	V
Output Low Voltage		Sink I <sub>o</sub> = 1mA	0		0.4	V
Maximum Tri-State Leakage Current		GDH in High Impedance State			2	μA
Propagation delay time from current sense inputs to PWM output <sup>(1)</sup>	T <sub>DLPWM</sub>	T <sub>A</sub> = 25°C		85		ns
<b>Soft-Start, Overload Hiccup and Enable</b>						
Soft-Start Charging Current	I <sub>SS1</sub> , I <sub>SS2</sub>	V <sub>SS1</sub> = V <sub>SS2</sub> = 1.5V		9.5		μA
Overload Hiccup Enabling Voltage		V <sub>SS1</sub> and V <sub>SS2</sub> Increasing		3.2		V
Soft-Start Discharging Current at Over Current Condition	I <sub>SS1(DIS)</sub> , I <sub>SS2(DIS)</sub>	V <sub>IN1</sub> = 0.5V <sub>REF</sub> , V <sub>IN2</sub> = 0.5V <sub>REFIN</sub> , V <sub>SS1</sub> = V <sub>SS2</sub> > 2.85V		37		μA
		V <sub>IN1</sub> = 0.5V <sub>REF</sub> , V <sub>IN2</sub> = 0.5V <sub>REFIN</sub> , V <sub>SS1</sub> = V <sub>SS2</sub> < 2.85V		7.5		μA
Overload Hiccup Threshold Voltage		V <sub>SS1</sub> and V <sub>SS2</sub> Decreasing		2.85		V
Overload Hiccup Recovery Soft-Start Voltage	VSSRCV1, VSSRCV2	VSS1 and VSS2 Decreasing		0.5		V
PWM Output Disable SS/EN Voltage					0.6	V
PWM Output Enable SS/EN Voltage				1.2	1.5	V
<b>Internal 0.5V Reference Buffer</b>						
Output Voltage	V <sub>REFOUT</sub>	I <sub>REFOUT</sub> = -1mA, 0°C < T <sub>A</sub> = T <sub>J</sub> < 70°C	495	500	505	mV
Load Regulation		0 < I <sub>REFOUT</sub> < -5mA		0.05		%/mA
Line Regulation		AVCC <sub>TH</sub> < AVCC < 15V, I <sub>REFOUT</sub> = -1mA			0.02%	%V

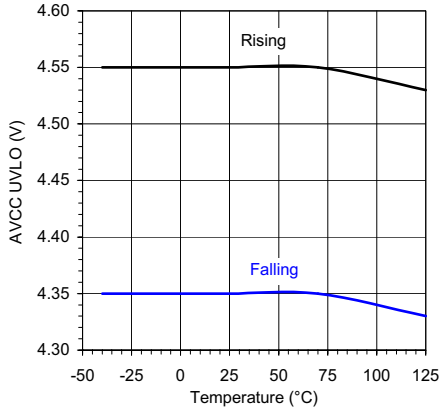
Notes:

(1) Guaranteed by design, not tested in production.

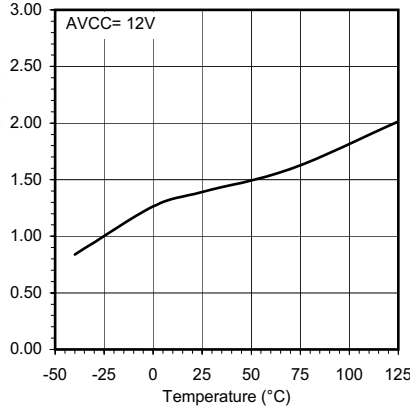
**POWER MANAGEMENT**

**Typical Performance Characteristics**

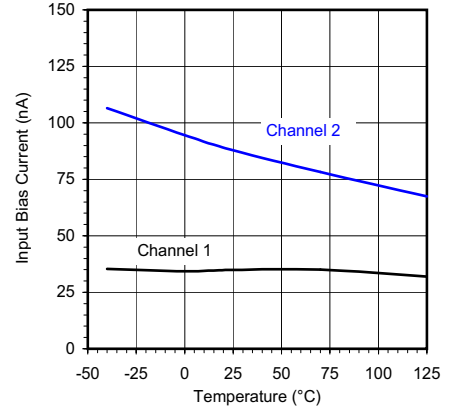
**UVLO Thresholds vs Temperature**



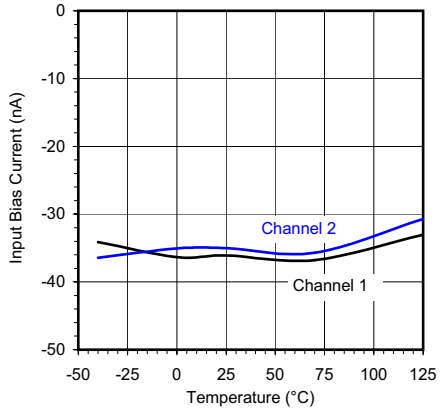
**Error Amplifier Input Offset Voltage vs Temperature**



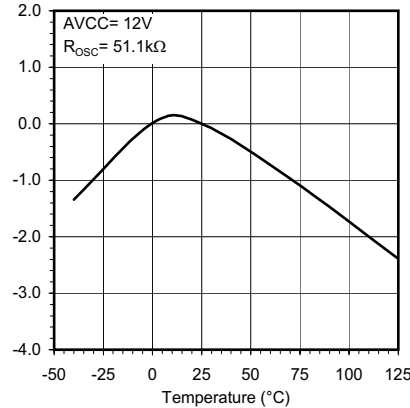
**Error Amplifier Inverting Input Bias Current vs Temperature**



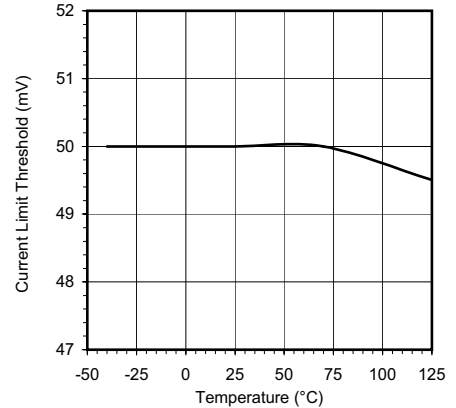
**Error Amplifier Non-inverting Input Bias Current vs Temperature**



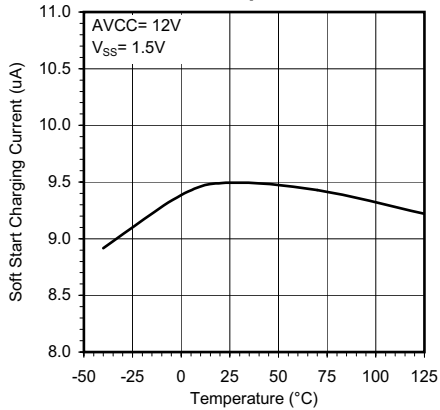
**Switching Frequency Variation vs Temperature**



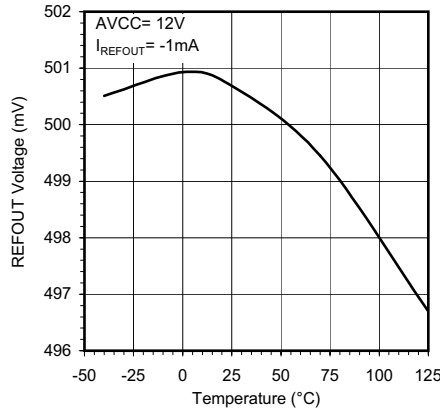
**Source Current Limit Threshold vs Temperature**



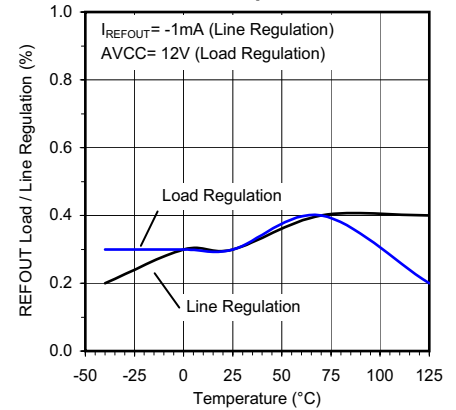
**Soft-Start Charging Current vs Temperature**



**REFOUT vs Temperature**

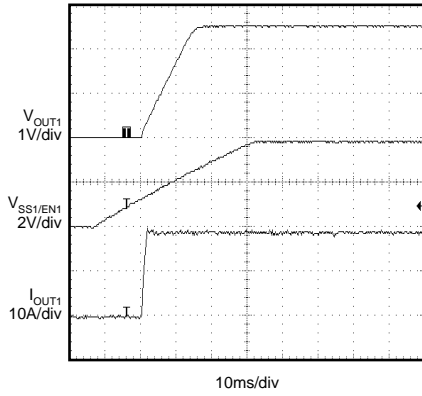
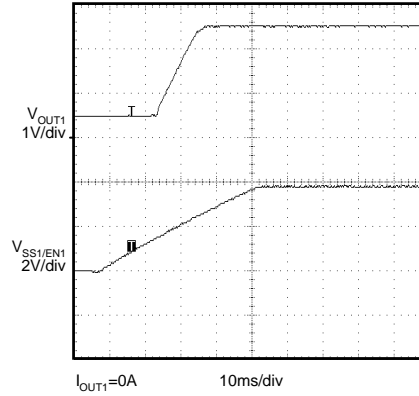
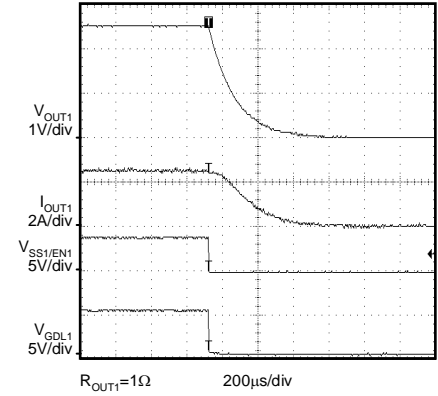
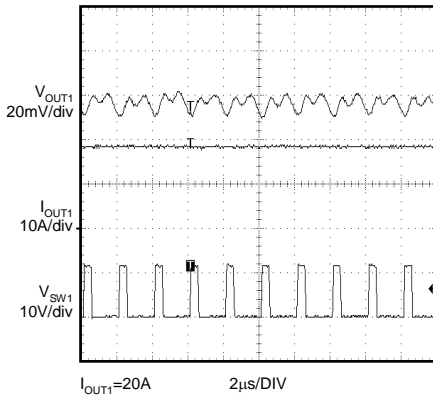
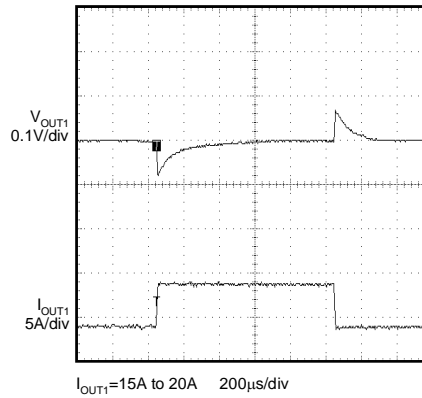
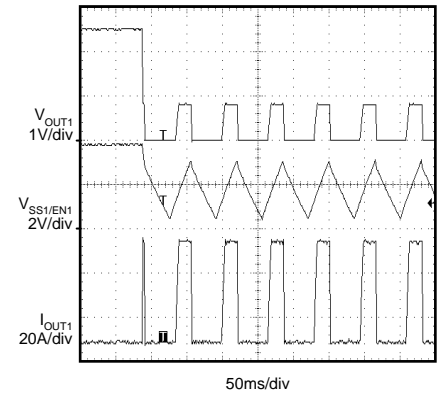
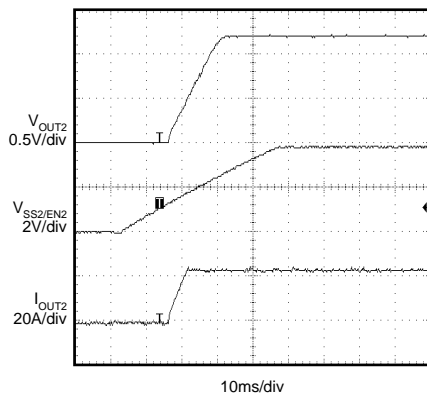
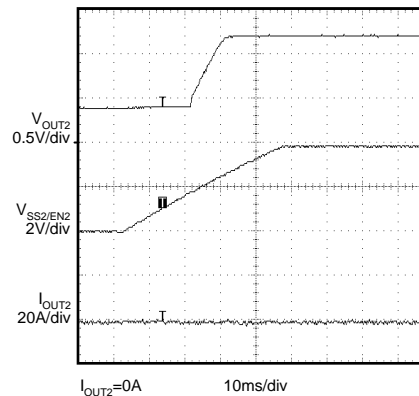
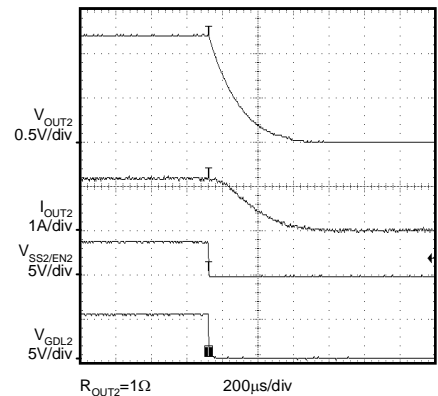


**REFOUT Load/Line Regulation vs Temperature**



**POWER MANAGEMENT**
**Typical Application Circuit Performance**

Circuit Conditions: 2-Output Configuration as in Figure 16.  $V_{IN} = 12V$ ,  $V_{OUT1} = 2.5V$ ,  $V_{OUT2} = 1.2V$ ,  $R_{OSC} = 51.1k\Omega$ ,  $SYNC = 0$ , and  $T_A = 25^\circ C$ .

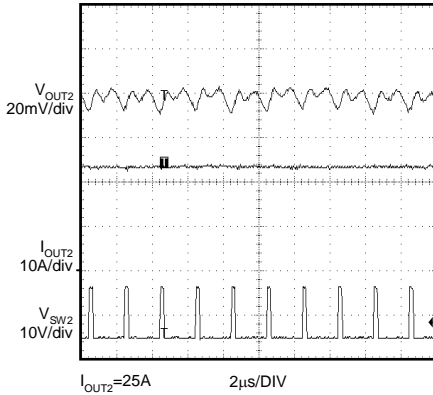
**Soft-Start Up ( $V_{OUT1}$ )**

**Pre-biased Start Up ( $V_{OUT1}$ )**

**Shutdown ( $V_{OUT1}$ )**

**Output Voltage Ripple ( $V_{OUT1}$ )**

**Load Transient Response ( $V_{OUT1}$ )**

**Overload Hiccup ( $V_{OUT1}$ )**

**Soft-Start Up ( $V_{OUT2}$ )**

**Pre-biased Start Up ( $V_{OUT2}$ )**

**Shutdown ( $V_{OUT2}$ )**


**POWER MANAGEMENT**

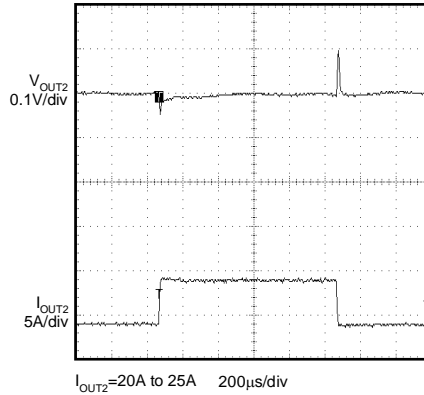
**Typical Application Circuit Performance**

Circuit Conditions: 2-Output Configuration as in Figure 16.  $V_{IN} = 12V$ ,  $V_{OUT1} = 2.5V$ ,  $V_{OUT2} = 1.2V$ ,  $R_{OSC} = 51.1k\Omega$ , SYNC = 0, and  $T_A = 25^\circ C$ .

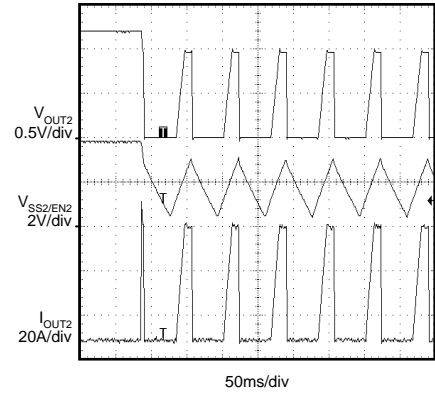
**Output Voltage Ripple ( $V_{OUT2}$ )**



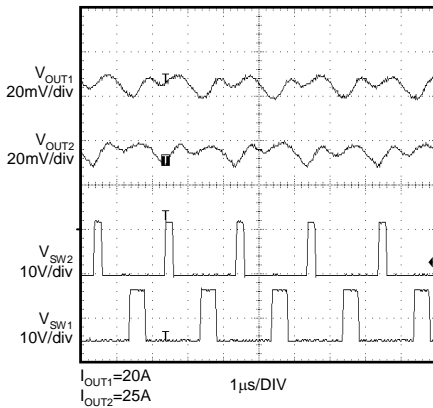
**Load Transient Response ( $V_{OUT2}$ )**



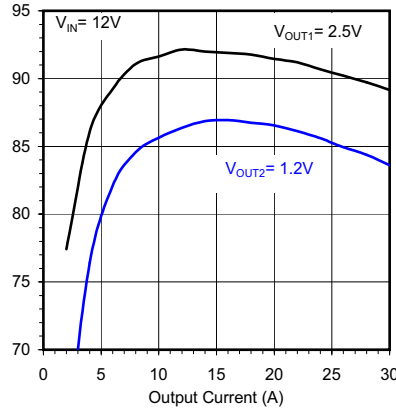
**Overload Hiccup ( $V_{OUT2}$ )**



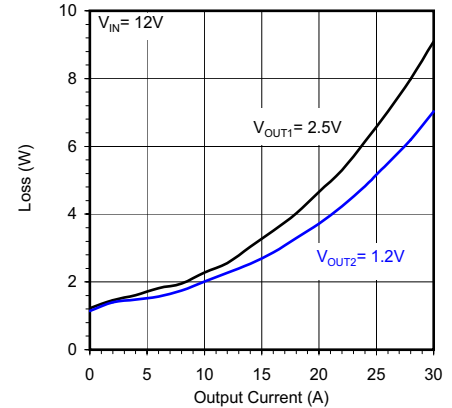
**Output Voltage Ripple  $V_{OUT1}$  &  $V_{OUT2}$**



**Efficiency @ Fsw= 500kHz  
2.5V & 1.2V**

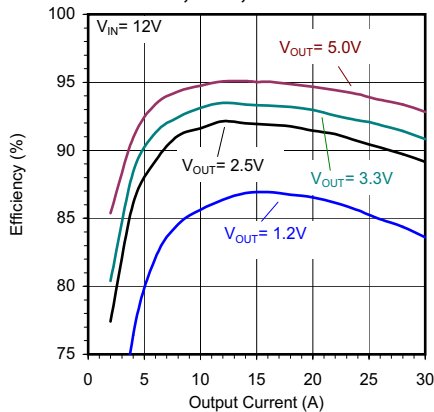


**Loss @ Fsw= 500kHz  
2.5V & 1.2V**

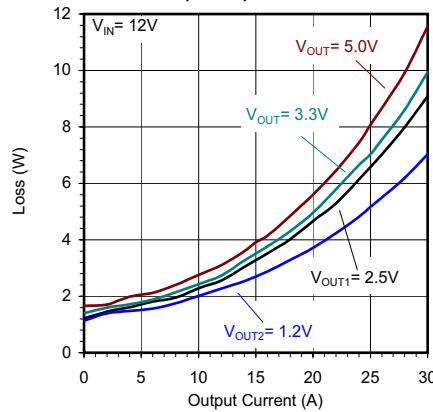


Circuit Conditions: 2-Output Configuration,  $V_{IN} = 12V$ ,  $L_{OUT} = 0.4\mu H$  for  $V_{OUT} = 1.2V$ ,  $L_{OUT} = 1\mu H$  for  $V_{OUT} = 2.5V, 3.3V$ , and  $5.0V$ ,  $R_{OSC} = 51.1k\Omega$ , and  $T_A = 25^\circ C$ .

**Efficiency @ Fsw= 500kHz  
5.0V, 3.3V, 2.5V & 1.2V**



**Loss @ Fsw= 500kHz  
5.0V, 3.3V, 2.5V & 1.2V**



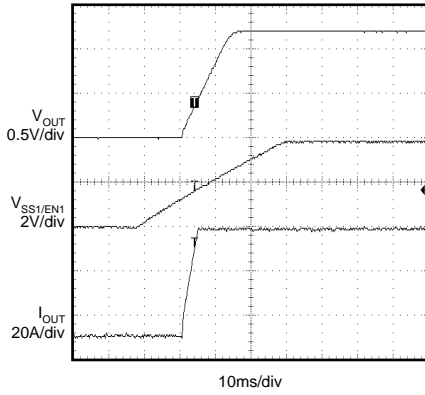


**POWER MANAGEMENT**

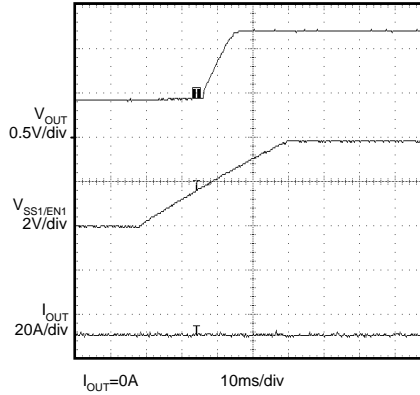
**Typical Application Circuit Performance**

Circuit Conditions: 2-Phase Configuration as in Figure 17,  $V_{IN} = 12V$ ,  $V_{OUT} = 1.2V$ ,  $R_{OSC} = 51.1k\Omega$ , SYNC = 0, and  $T_A = 25^\circ C$ .

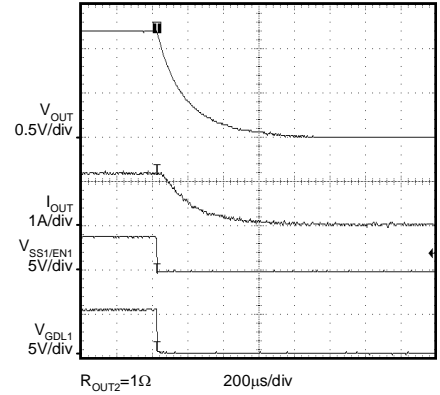
**Soft-Start Up**



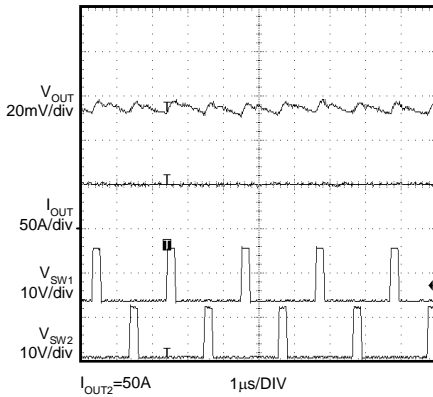
**Pre-biased Start Up ( $V_{OUT}$ )**



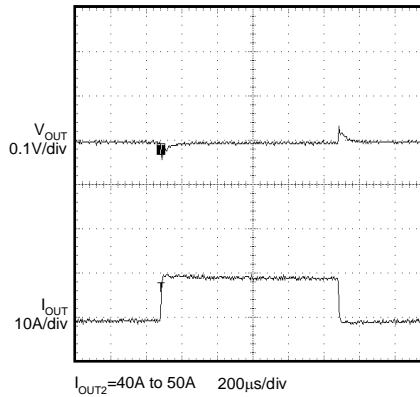
**Shutdown ( $V_{OUT}$ )**



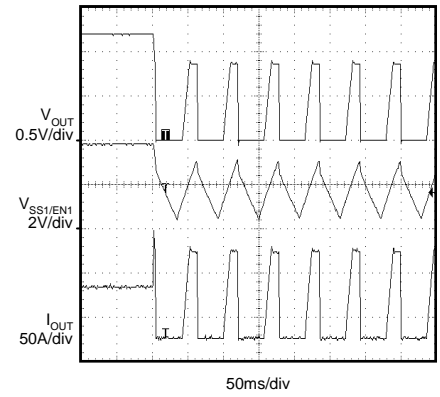
**Output Voltage Ripple ( $V_{OUT}$ )**



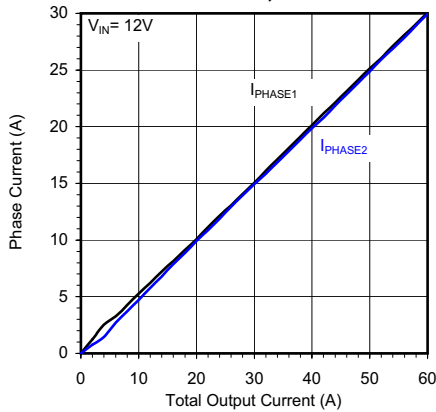
**Load Transient Response ( $V_{OUT}$ )**



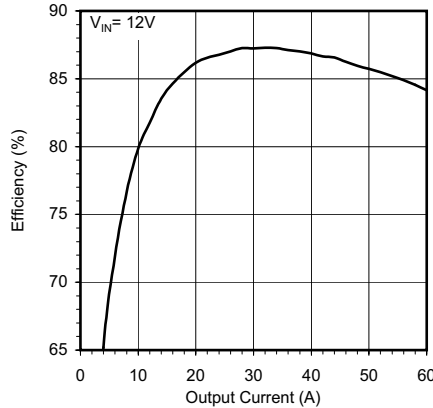
**Overload Hiccup ( $V_{OUT}$ )**



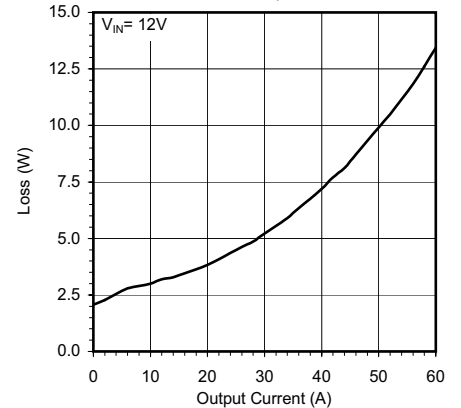
**Current Share  
2-Phase, 1.2V**



**Efficiency @ Fsw= 500kHz  
2-Phase, 1.2V**



**Loss @ Fsw= 500kHz  
2-Phase, 1.2V**



**POWER MANAGEMENT**
**Pin Descriptions**

Pin	Pin Name	Pin Function
1	CS1+	The Non-inverting Input of Channel 1 Current-sense Amplifier/Comparator
2	CS1-	The Inverting Input of Channel 1 Current-sense Amplifier/Comparator. Normally tied to the output of the converter.
3	ROSC	An external resistor connected from this pin to AGND sets the oscillator frequency.
4	IN1-	Inverting Input of Channel 1 Error Amplifier. Tie an external resistive divider between output 1 and ground for output voltage sensing.
5	COMP1	The Channel 1 Error Amplifier Output. This pin is used for loop compensation.
6	SYNC	Edge-triggered Synchronization Input. When not synchronized, tie this pin to a voltage above 1.5V or ground. An external clock (frequency > frequency set with ROSC) at this pin synchronizes the controllers.
7	AGND	Analog Signal Ground.
8	REF	The Non-inverting Input of Channel 1 Error Amplifier.
9	REFOUT	Buffered 0.5V internal reference.
10	REFIN	An external reference voltage is applied to this pin. This is also the non-inverting input of Channel 2 Error amplifier.
11	COMP2	The Channel 2 Error Amplifier Output. This pin is used for loop compensation.
12	IN2-	The Inverting Input of Channel 2 Error Amplifier. Tie an external resistive divider between output 2 and ground for output voltage sensing. Tie to AVCC for two-phase single output applications.
13	CS2-	The Inverting Input of Channel 2 Current-sense Amplifier/Comparator. Normally tied to the output of the converter.
14	CS2+	The Non-inverting Input of Channel 2 Current-sense Amplifier/Comparator.
15	SS2/EN2	An external capacitor tied to this pin sets (1) the soft-start time (2) output overload shutdown time for Channel 2. Pulling this pin below 0.6V tri-states GHD2 and forces GDL2 low. Leave open for two-phase single output applications.
16	AVCC	Power Supply Voltage for the Analog Portion of the Controllers.
20	GDH2	PWM Output 2.
21	GDL2	Logic Enable Signal for Channel 2.
24	GDL1	Logic Enable Signal for Channel 1.
25	GDH1	PWM Output 1.
28	SS1/EN1	An external capacitor tied to this pin sets (1) the soft-start time (2) output overload shutdown time for Channel 1. Pulling this pin below 0.6V tri-states GDH1 and forces GDL1 low.
17,18,19 22,23,26,27	NC	No Connection.

POWER MANAGEMENT

Block Diagram

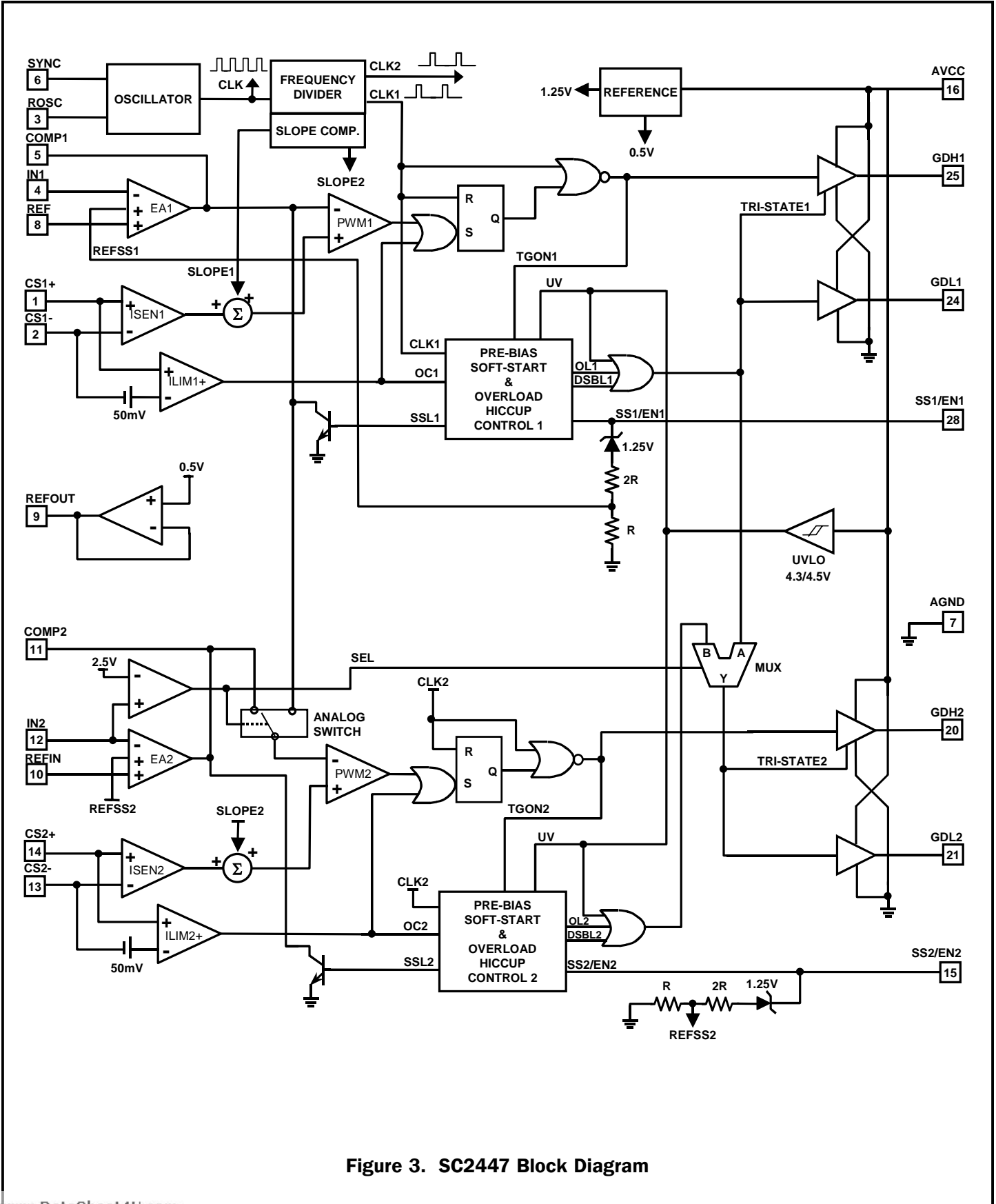
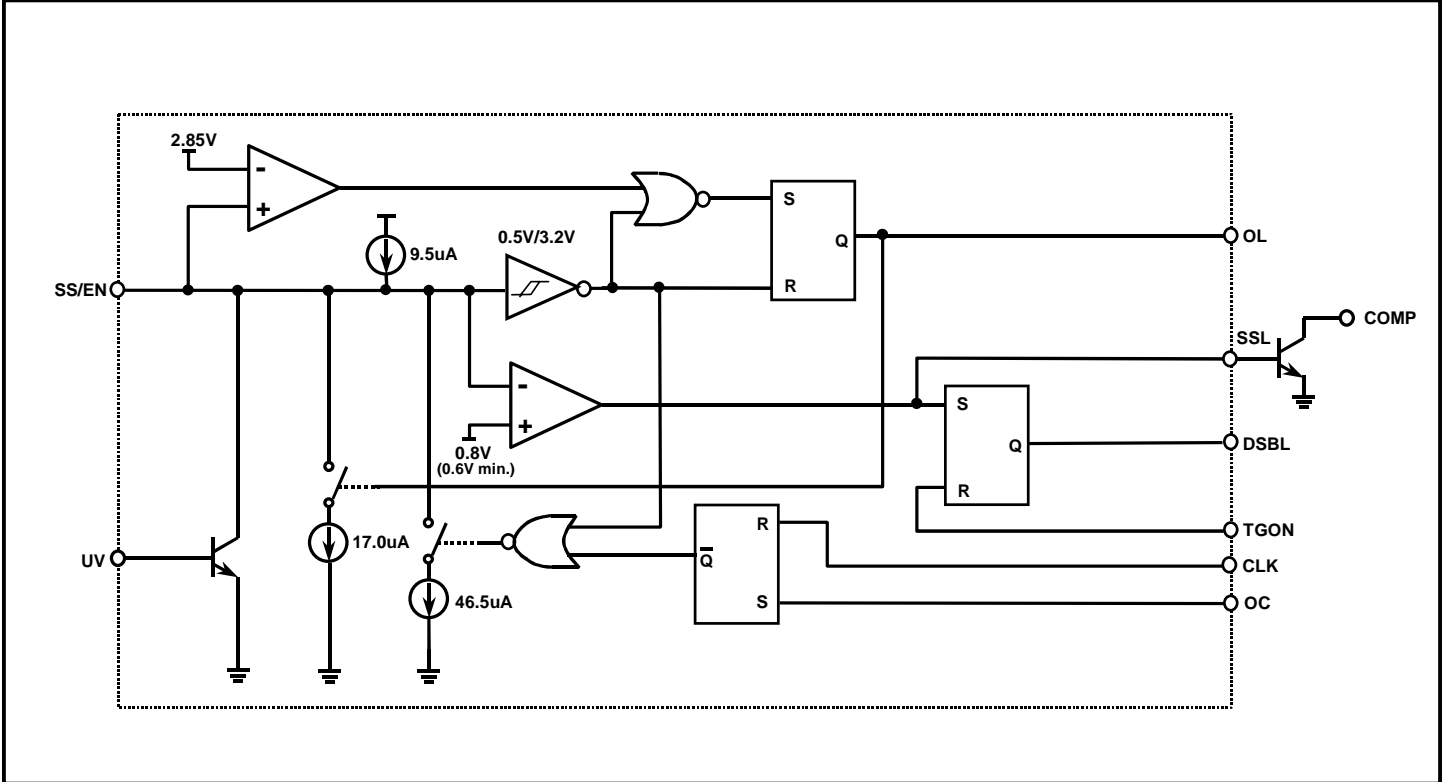


Figure 3. SC2447 Block Diagram

**POWER MANAGEMENT**

**Block Diagram**



**Figure 4. Soft-Start and Overload Hiccup Control Circuit**

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Timing Chart

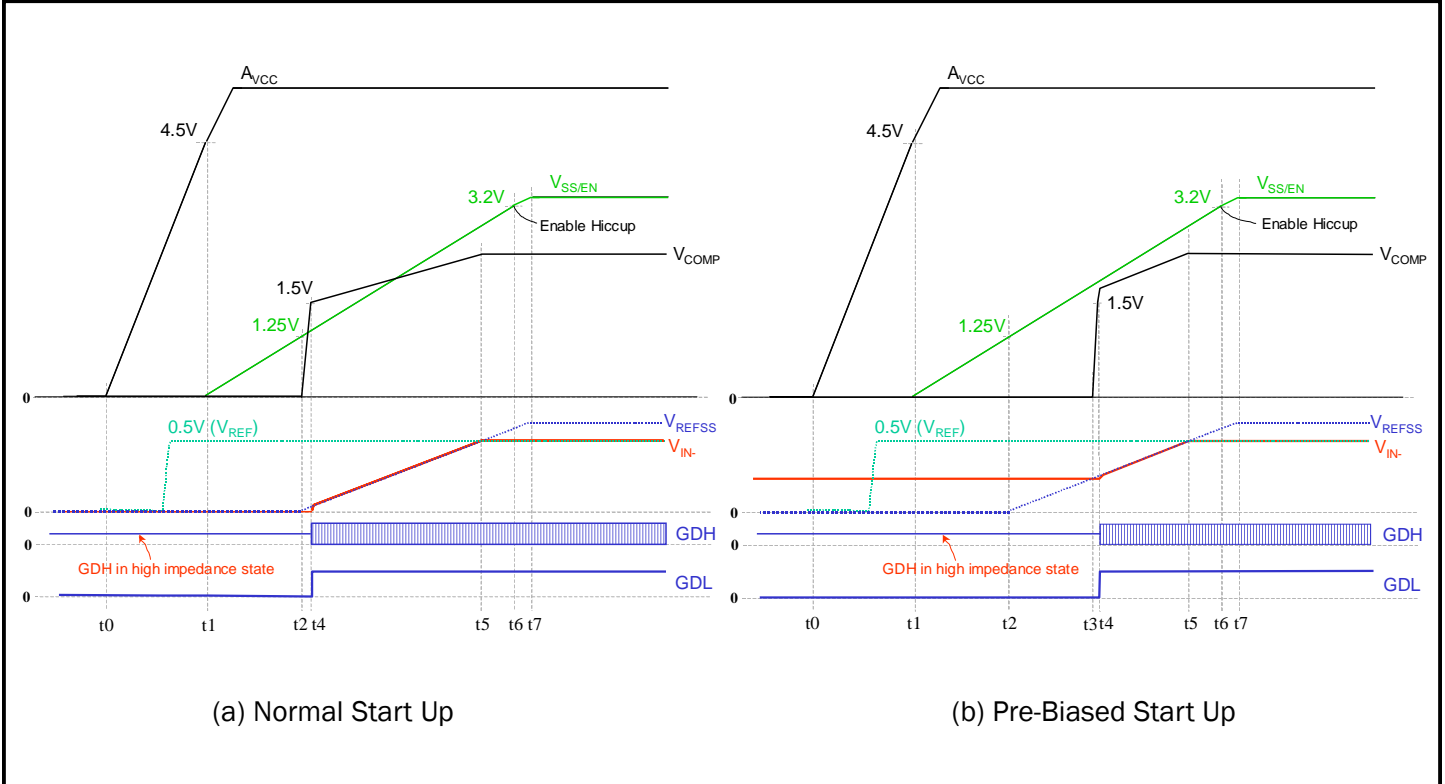


Figure 5. SC2447 Start-up Timing Diagram

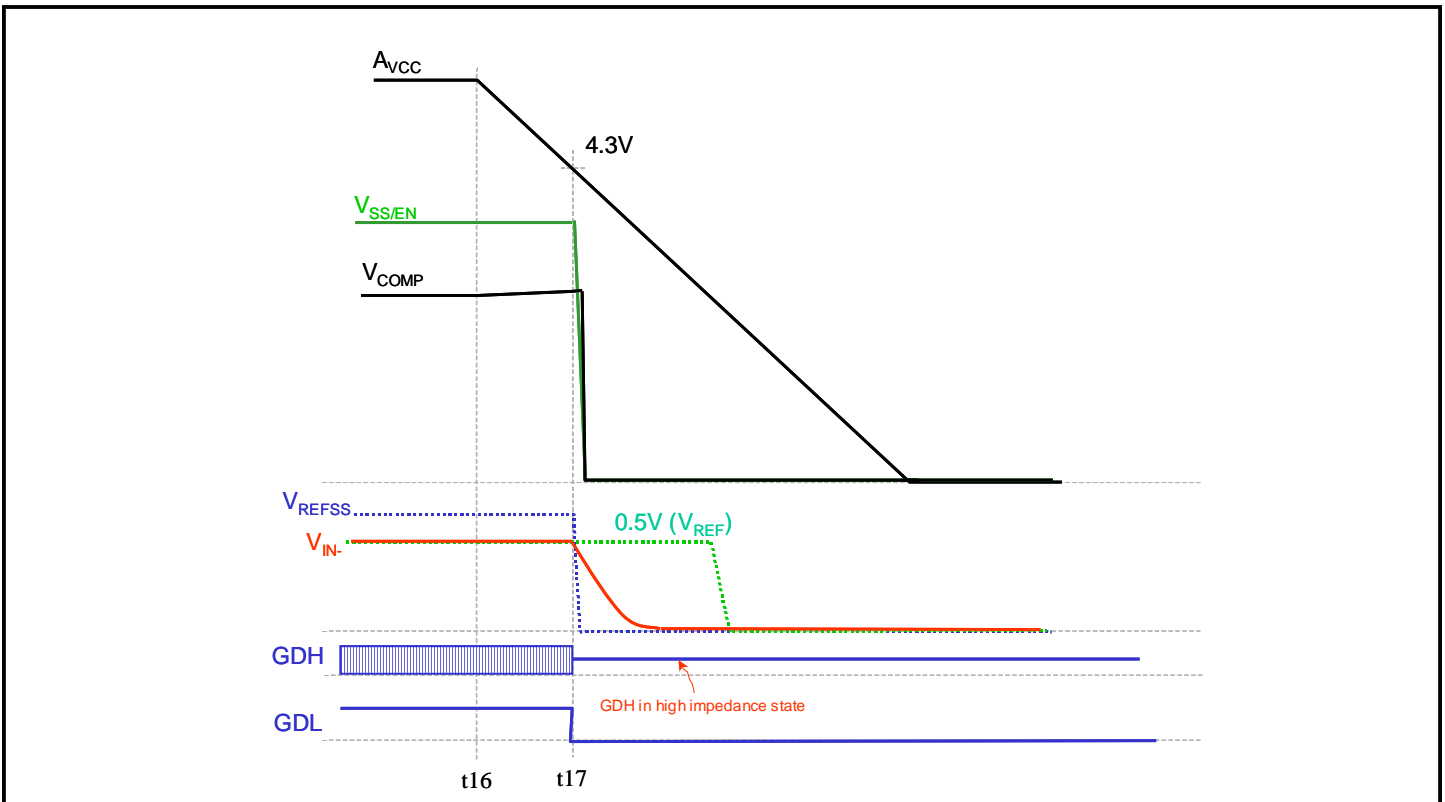
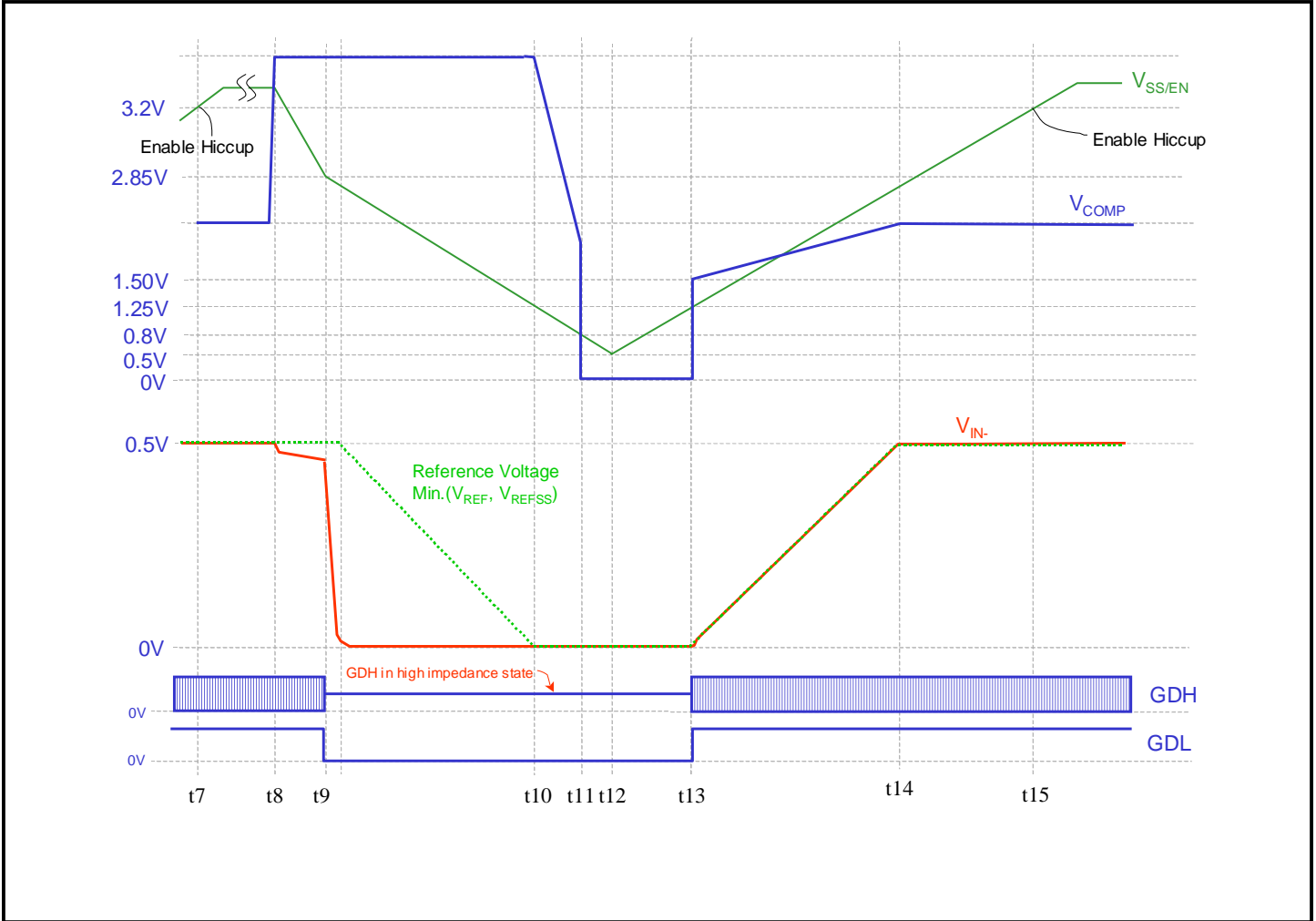


Figure 6. SC2447 UVLO Shutdown Timing Diagram

**POWER MANAGEMENT**

**Timing Chart**



**Figure 7. SC2447 Overload Hiccup Operation Timing Diagram**

**POWER MANAGEMENT**
**Application Information**

The SC2447 consists of two current-mode synchronous buck controllers with many integrated functions. The SC2447 can be used to generate:

- 1) two independent outputs from a common input or two different inputs or,
- 2) dual-phase output with current sharing,
- 3) current sourcing/sinking from common or separate inputs as in DDR (I and II) memory application.

**Step-Down Converter**

Starting from the following step-down converter specifications,

Input voltage range:  $V_{in} \in [V_{in,min}, V_{in,max}]$

Input voltage ripple (peak-to-peak):  $\Delta V_{in}$

Output voltage:  $V_o$

Output voltage accuracy:  $\epsilon$

Output voltage ripple (peak-to-peak):  $\Delta V_o$

Nominal output (load) current:  $I_o$

Maximum output current limit:  $I_{o,max}$

Output (load) current transient slew rate:  $di_o$  (A/s)

Circuit efficiency:  $\eta$

Selection criteria and design procedures for the following are described.

- 1) output inductor ( $L$ ) type and value
- 2) output capacitor ( $C_o$ ) type and value
- 3) input capacitor ( $C_{in}$ ) type and value
- 4) power MOSFETs
- 5) current sensing and limiting circuit
- 6) voltage sensing circuit
- 7) loop compensation network

**Operating Frequency ( $f_s$ )**

The switching frequency in the SC2447 is user-programmable. The advantages of using constant frequency operation are simple passive component selection and ease of feedback compensation. Before setting the operating frequency, the following trade-offs should be considered:

- 1) Passive component size
- 2) Efficiency
- 3) EMI condition
- 4) Minimum switch on time
- 5) Maximum duty ratio

For a given output power, the size of the passive components are inversely proportional to the switching frequency, whereas MOSFET/Diode switching losses are proportional to the operating frequency. Other issues such as heat dissipation, packaging and the cost issues are also considered. The frequency bands for signal transmission should be avoided because of EM interference.

**Minimum Switch On Time Consideration**

In the SC2447, the falling edge of the clock turns on the top MOSFET. The inductor current and the sensed voltage ramp up. After the sensed voltage crosses a threshold determined by the error amplifier output, the top MOSFET is turned off. The propagation delay time from the turn-on of the controlling FET to its turn-off is the minimum switch on time. This propagation delay time consists of the propagation delay time ( $T_{DLPWM}$ ) from the current sense inputs to the PWM output and the propagation delay time ( $T_{DLTG}$ ) from the trailing edge of the PWM input to the trailing edge of the phase voltage.

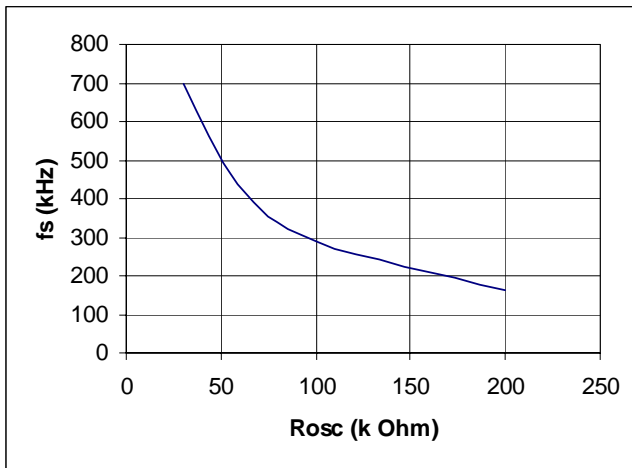
The SC2447 has a typical propagation delay time from the current sense inputs to the PWM output of about 85ns at room temperature. The shortest on interval ( $T_{MINON}$ ) of the controlling FET is then  $85ns + T_{DLTG}$ . Assuming that  $T_{DLTG}$  is 45ns, the controller either does not turn on the top MOSFET at all or turns it on for at least 130ns.  $T_{DLTG}$  can be found in the MOSFET driver datasheet.

For a synchronous step-down converter, the operating duty cycle is  $V_o/V_{IN}$ . The required on time for the top MOSFET is  $V_o/(V_{IN} * f_s)$ . If the frequency is set such that the required pulse width is less than 130ns, assuming  $T_{DLTG}$  is 45ns, then the converter will start skipping cycles. Due to minimum on-time limitation, simultaneously operating at very high switching frequency and very short duty cycle is not practical. If the voltage conversion ratio  $V_o/V_{IN}$  and hence the required duty cycle is higher, the switching frequency can be increased to reduce the size of passive components.

There will not be enough modulating headroom if the on time is made equal to the minimum on time ( $T_{MINON}$ ). For ease of control, set the switching frequency so that the pulse width is at least 1.5 times the minimum on time.

**POWER MANAGEMENT**
**Application Information (Cont.)**
**Setting the Switching Frequency**

The switching frequency is set with an external resistor connected from Pin 3 to the ground. The set frequency is inversely proportional to the resistor value (Figure 8).



**Figure 8. Free Running Frequency vs.  $R_{osc}$**

**Inductor (L) and Ripple Current**

Both step-down controllers in the SC2447 operate in synchronous continuous-conduction mode (CCM) regardless of the output load. The output inductor selection/design is based on the output DC and transient requirements. Both output current and voltage ripples are reduced with larger inductors but it takes longer to change the inductor current during load transients. Conversely, smaller inductors results in lower DC copper losses but the AC core losses (flux swing) and the winding AC resistance losses are higher. A compromise is to choose the inductance such that peak-to-peak inductor ripple-current is 20% to 30% of the rated output load current.

Assuming that the inductor current ripple (peak-to-peak) value is  $\delta \cdot I_o$ , the inductance value will then be

$$L = \frac{V_o(1-D)}{\delta I_o f_s}$$

The peak current in the inductor becomes  $(1+\delta/2) \cdot I_o$  and the RMS current is

$$I_{L,rms} = I_o \sqrt{1 + \frac{\delta^2}{12}}$$

Consider the following when choosing inductors:

a) Inductor core material: For high efficiency applications above 350kHz, ferrite, Kool-Mu and polypermalloy materials should be used. Low-cost powdered iron cores can be used for cost sensitive-applications below 350kHz but with attendant higher core losses.

b) Select inductance value: Sometimes the calculated inductance value is not available off-the-shelf. The designer can choose the next larger standard inductance value. The inductance varies with temperature and DC current. It is a good engineering practice to re-evaluate the resulting current ripple at the rated DC output current.

c) Current rating: The saturation current of the inductor should be at least 1.5 times of the peak inductor current under all conditions.

**Output Capacitor ( $C_o$ ) and  $V_{out}$  Ripple**

The output capacitor filters the inductor current in the steady state and serves as a reservoir during load transient. The output capacitor can be modeled as an ideal capacitor in series with its parasitic ESR ( $R_{esr}$ ) and ESL ( $L_{esl}$ ) (Figure 9).



**Figure 9. An Equivalent Circuit of  $C_o$**

If the current through the branch is  $i_b(t)$ , the voltage across the terminals will then be

$$v_o(t) = V_o + \frac{1}{C_o} \int_0^t i_b(t) dt + L_{esl} \frac{di_b(t)}{dt} + R_{esr} i_b(t)$$

This basic equation illustrates the effect of ESR, ESL and  $C_o$  on the output voltage.

The first term is the DC voltage across  $C_o$  at time  $t=0$ . The second term is the voltage variation caused by the



**POWER MANAGEMENT**
**Application Information (Cont.)**

charge balance between the load and the converter output. The third term is voltage ripple due to ESL and the fourth term is the voltage ripple due to ESR. The total output voltage ripple is then the vector sum of the last three terms.

Since the inductor current waveform is a triangular with peak-to-peak value  $\delta I_o$ , the ripple-voltage caused by inductor current ripple is

$$\Delta V_C \approx \frac{\delta I_o}{8C_o f_s}$$

the ripple-voltage due to ESL is

$$\Delta V_{ESL} = L_{esl} f_s \frac{\delta I_o}{D}$$

and the ESR ripple-voltage is

$$\Delta V_{ESR} = R_{esr} \delta I_o$$

Aluminum capacitors (e.g. electrolytic, solid OS-CON, POSCAP, tantalum) have high capacitances and low ESLs. The ESR has the dominant effect on the output ripple voltage. It is therefore very important to minimize the ESR.

When determining the ESR value, both the steady state ripple-voltage and the dynamic load transient need to be considered. To keep the steady state output ripple-voltage  $< \Delta V_o$ , the ESR should satisfy

$$R_{esr1} < \frac{\Delta V_o}{\delta I_o}$$

To limit the dynamic output voltage overshoot/undershoot to within  $\alpha$  (say 3%) of the steady state output voltage) from no load to full load, the ESR value should satisfy

$$R_{esr2} < \frac{\alpha V_o}{I_o}$$

Then, the required ESR value of the output capacitors should be

$$R_{esr} = \min\{R_{esr1}, R_{esr2}\}$$

The voltage rating of aluminum capacitors should be at least  $1.5V_o$ . The RMS current ripple rating should also be greater than

$$\frac{\delta I_o}{2\sqrt{3}}$$

Usually it is necessary to have several capacitors of the same type in parallel to satisfy the ESR requirement. The voltage ripple cause by the capacitor charge/discharge should be an order of magnitude smaller than the voltage ripple caused by the ESR. To guarantee this, the capacitance should satisfy

$$C_o > \frac{10}{2\pi f_s R_{esr}}$$

In many applications, several low ESR ceramic capacitors are added in parallel with the aluminum capacitors in order to further reduce ESR and improve high frequency decoupling. Because the values of capacitance and ESR are usually different in ceramic and aluminum capacitors, the following remarks are made to clarify some practical issues.

**Remark 1:** High frequency ceramic capacitors may not carry most of the ripple current. It also depends on the capacitor value. Only when the capacitor value is set properly, the effect of ceramic capacitor low ESR starts to be significant.

For example, if a  $10\mu\text{F}$ ,  $4\text{m}\Omega$  ceramic capacitor is connected in parallel with  $2 \times 1500\mu\text{F}$ ,  $90\text{m}\Omega$  electrolytic capacitors, the ripple current in the ceramic capacitor is only about 42% of the current in the electrolytic capacitors at the ripple frequency. If a  $100\mu\text{F}$ ,  $2\text{m}\Omega$  ceramic capacitor is used, the ripple current in the ceramic capacitor will be about 4.2 times of that in the electrolytic capacitors. When two  $100\mu\text{F}$ ,  $2\text{m}\Omega$  ceramic capacitors are used, the current ratio increases to 8.3. In this case most of the ripple current flows in the ceramic decoupling capacitor. The ESR of the ceramic capacitors will then determine the output ripple-voltage.

**Remark 2:** The total equivalent capacitance of the filter bank is not simply the sum of all the paralleled capacitors. The total equivalent ESR is not simply the parallel combination of all the individual ESRs either. Instead

**POWER MANAGEMENT**

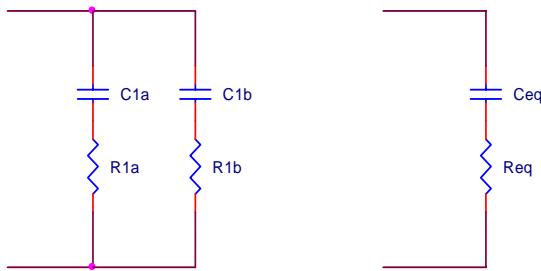
**Application Information (Cont.)**

they should be calculated using the following formulae.

$$C_{eq}(\omega) := \frac{(R_{1a} + R_{1b})^2 \omega^2 C_{1a}^2 C_{1b}^2 + (C_{1a} + C_{1b})^2}{(R_{1a}^2 C_{1a} + R_{1b}^2 C_{1b}) \omega^2 C_{1a} C_{1b} + (C_{1a} + C_{1b})}$$

$$R_{eq}(\omega) := \frac{R_{1a} R_{1b} (R_{1a} + R_{1b}) \omega^2 C_{1a}^2 C_{1b}^2 + (R_{1b} C_{1b}^2 + R_{1a} C_{1a}^2)}{(R_{1a} + R_{1b})^2 \omega^2 C_{1a}^2 C_{1b}^2 + (C_{1a} + C_{1b})^2}$$

where  $R_{1a}$  and  $C_{1a}$  are the ESR and capacitance of electrolytic capacitors, and  $R_{1b}$  and  $C_{1b}$  are the ESR and capacitance of the ceramic capacitors respectively. (Figure 10)



**Figure 10. Equivalent RC Branch**

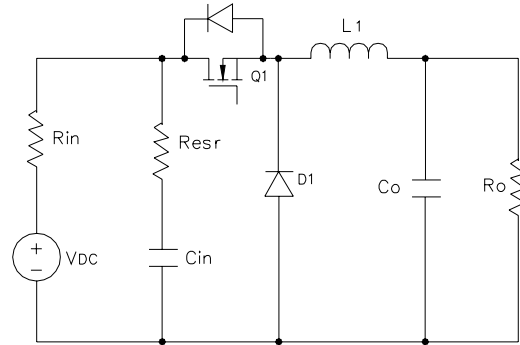
$R_{eq}$  and  $C_{eq}$  are both functions of frequency. For rigorous design, the equivalent ESR should be evaluated at the ripple frequency for voltage ripple calculation when both ceramic and electrolytic capacitors are used. If  $R_{1a} = R_{1b} = R_1$  and  $C_{1a} = C_{1b} = C_1$ , then  $R_{eq}$  and  $C_{eq}$  will be frequency-independent and

$$R_{eq} = 1/2 R_1 \text{ and } C_{eq} = 2C_1.$$

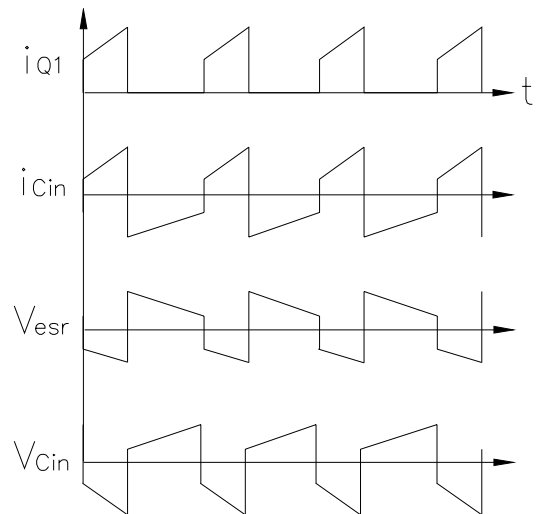
**Input Capacitor ( $C_{in}$ )**

The input supply to the converter usually comes from a pre-regulator. Since the input supply is not ideal, input capacitors are needed to filter the current pulses at the switching frequency. A simple buck converter is shown in Figure 11.

In Figure 11 the DC input power supply has an internal impedance  $R_{in}$  and the input capacitor  $C_{in}$  has an ESR of  $R_{esr}$ . The MOSFET and the input capacitor current waveforms, the ESR voltage ripple and the input voltage ripple are shown in Figure 12.



**Figure 11. A Simple Model for the Converter Input**



**Figure 12. Typical Waveforms at Converter Input**

It can be seen that high di/dt pulse current flows in the input capacitor. Capacitors with low ESL should be used. It is also important to place the input capacitor close to the MOSFETs on the PC board to reduce trace inductance around the pulse current loop.

The RMS value of the capacitor current is approximately

$$I_{Cin} = I_o \sqrt{D \left[ \left(1 + \frac{\delta^2}{12}\right) \left(1 - \frac{D}{\eta}\right)^2 + \frac{D}{\eta^2} (1 - D) \right]}$$

The power dissipated in the input capacitor is then

$$P_{Cin} = I_{Cin}^2 R_{esr}$$

**POWER MANAGEMENT**
**Application Information (Cont.)**

For reliable operation, the maximum power dissipation in the capacitors should not result in more than 10°C of temperature rise. Many manufacturers specify the maximum allowable ripple current (ARMS), rating of the capacitor at a given ripple frequency and ambient temperature. The input capacitance should be large enough to handle the ripple current. For higher power applications, multiple capacitors are placed in parallel to increase the ripple current handling capability.

Sometimes meeting tight input voltage ripple specifications may require the use of larger input capacitance. At full load, the peak-to-peak input voltage ripple due to the ESR is

$$\Delta v_{ESR} = R_{esr} \left(1 + \frac{\delta}{2}\right) I_o.$$

The peak-to-peak input voltage ripple due to the capacitor is

$$\Delta v_C \approx \frac{DI_o}{C_{in} f_s},$$

From these two expressions,  $C_{IN}$  can be found to meet the input voltage ripple specification. In a multi-phase converter, interleaved switching reduces ripple. The two step-down channels of the SC2447 operate at 180 degrees from each other. If both step-down channels in the SC2447 are connected in parallel, both the input and the output RMS currents will be reduced.

Ripple cancellation effect of interleaving allows the use of smaller input capacitors. When converter outputs are connected in parallel and interleaved, a smaller inductor and capacitor can be used for each channel. The total output ripple-voltage remains unchanged. The use of a smaller inductor helps speed up the output load transient.

When two channels with a common input are interleaved, the combined input current waveform depends on the duty ratios and the output currents of both channels. Assuming that the output current ripple is small, the following formula can be used to estimate the RMS ripple current in the input capacitor.

Let the duty ratio and output current of Channel 1 and Channel 2 be  $D_1$ ,  $D_2$  and  $I_{o1}$ ,  $I_{o2}$ , respectively.

If  $D_1 < 0.5$  and  $D_2 < 0.5$ , then

$$I_{Cin} \approx \sqrt{D_1 I_{o1}^2 + D_2 I_{o2}^2}.$$

**Choosing Power MOSFETs**

Power MOSFETs with integrated gate drivers such as PIP212, R2J20601NP, PIP202, PIP201 and IP2001, IP2002 are suitable for SC2447 application.

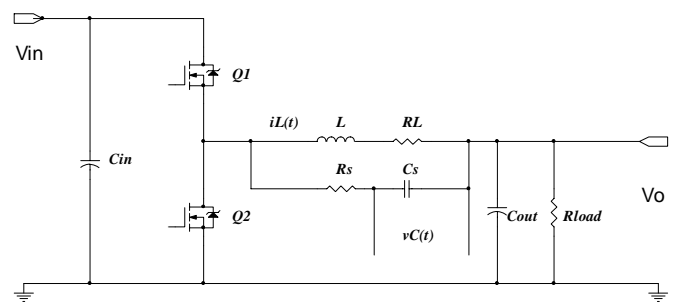
**Current Sensing**

Inductor current sensing is required for the current-mode control. Although the inductor current can be sensed with a precision resistor in series with the inductor, the lossless inductive current sense technique can be used in the SC2447. This technique has the advantages of,

- 1) lossless current sensing
- 2) lower cost compared to resistive sensing
- 3) more accurate compared to  $R_{DS(ON)}$  sensing

The basic arrangement of the inductive current sense is shown in Figure 13.

$R_L$  is the equivalent series resistance of the output inductor.  $R_s$  and  $C_s$  form a RC network for inductor current sensing.



**Figure 13. The Basic Structure of Inductive Current Sense**

In steady state, the DC voltage across  $R_L$  is

$$V_{CS} = R_L I_o.$$

Notice that the DC value of  $V_{CS}$  is independent of the values of  $L$ ,  $R_s$  and  $C_s$ . This means that, if only the average load current information is needed (such as in

**POWER MANAGEMENT**
**Application Information (Cont.)**

average current mode control), this current sensing method is sufficient without time constant matching requirement.

In the current mode control as implemented in SC2447, voltage ripple on  $C_s$  is required for PWM operation. In fact, the  $V_{cs}$  AC peak-to-peak voltage ripple (denoted as  $\Delta V_{cs}$ ) directly affects the signal-to-noise ratio of the PWM operation. In general, smaller  $\Delta V_{cs}$  leads to lower signal-to-noise ratio and more noise sensitive operation. Larger  $\Delta V_{cs}$  leads to more circuit (power stage) parameter sensitive operation. A good engineering compromise is:

$$\Delta V_{cs} \sim R_L \delta I_o$$

It is necessary to match the following time constants to equalize the ripple.

$$\frac{L}{R_L} \approx R_s C_s$$

For example,  $L = 1\mu\text{H}$  and  $R_L = 1.8\text{m}\Omega$ , the time constant  $R_s C_s$  should be set to  $555.6\mu\text{s}$ . If one selects  $C_s = 33\text{nF}$ , then  $R_s = 16.9\text{ k}\Omega$ .

**Scaling the Current Limit**

Over-current is handled differently in the SC2447 depending on the direction of the inductor current. If the differential sense voltage between CS+ and CS- exceeds  $+50\text{mV}$ , the PWM signal (GDH) will go low. The MOSFET driver will turn off the top MOSFET and turn on the bottom MOSFET, to limit the inductor current. This  $+50\text{mV}$  is the cycle-by-cycle peak current limit when the load is drawing current from the converter. There is no cycle-by-cycle current limit when the inductor current flows in the reverse direction.

In the circuit of Figure 13, the equivalent inductor current limit is set according to

$$I_{LMcp} = \frac{50\text{mV}}{R_L}$$

when the load is sourcing current from the converter. If  $R_L = 1.8\text{m}\Omega$ , then  $I_{LMcp} = 27.8\text{A}$ . The circuit in Figure 14 allows the user to scale the equivalent current limit with the same  $R_L$ .

$C_s$  in the current sensing network is usually in the range

of  $22\text{nF} \sim 330\text{nF}$ .

a) When the required current limit  $I_{LM}$  is higher than  $I_{LMcp}$ ,  $R_{s3}$  is not needed and solve the following three equations for  $R_s$ ,  $R_{s1}$ , and  $R_{s2}$ :

$$(R_s // R_{s1}) C_s = \frac{L}{R_L}$$

$$I_{LM} R_L \frac{R_{s1}}{R_s + R_{s1}} = 50\text{mV}$$

and  $R_{s2} = R_s // R_{s1}$ .

Note that  $R_{s2}$  is made equal to  $R_s // R_{s1}$  to reduce effect of the bias current of the current amplifier in SC2447.

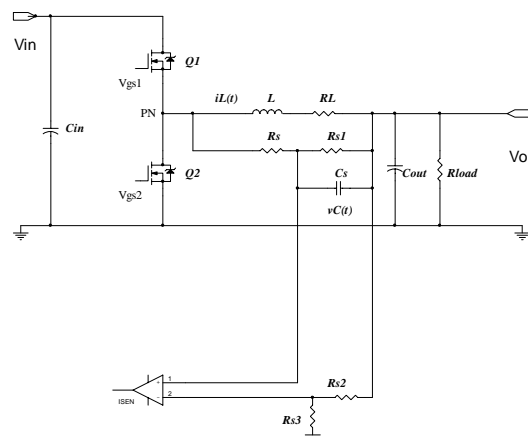
b) When the required current limit  $I_{LM}$  is less than  $I_{LMcp}$ , remove  $R_{s1}$  and solve the following two equations for  $R_s$  and  $R_{s3}$ :

$$R_s C_s = \frac{L}{R_L}$$

$$I_{LM} R_L + \frac{R_s}{R_{s3}} V_o = 50\text{mV}$$

$R_{s2}$  is then calculated from

$$R_{s2} = \frac{R_{s3} R_s}{R_{s3} - R_s}$$



**Figure 14. Scaling the Equivalent Current Limit**

**Application Information (Cont.)**
**Overload Protection and Hiccup**

During start-up, the capacitor from the SS/EN pin to ground functions as a soft-start capacitor. After the converter starts and enters regulation, the same capacitor operates as an overload shutoff timing capacitor. There is an internal net 9.5μA current source charging the soft start capacitor  $C_{32}(C_{33})$ , connected to the SS/EN pin. The soft-start voltage  $V_{SS/EN}$  will reach its final value if no current limit occurs. As the load current increases, the cycle-by-cycle current-limit comparator will first limit the inductor current. If  $V_{SS/EN}$  is higher than 3.2V, an internal net 37μA current source will discharge the soft-start capacitor  $C_{32}(C_{33})$  during the off time after tripping the over-current comparator. If  $V_{SS/EN}$  falls to 2.85V, the controller will shut off both the top and the bottom MOSFETs by pulling down the GDL and tri-stating the GDH output (PWM). An internal net 7.5μA current source discharges  $C_{32}(C_{33})$ .

When the capacitor is discharged below 0.5V, the overload hiccup latch is reset, the 9.5μA current source recharges the SS/EN capacitor and converter restarts. The overload hiccup function is enabled when the soft start capacitor voltage exceeds 3.2V. The converter will repeatedly start and shut off until it is no longer overloaded when the soft-start voltage exceeds 3.2V. This hiccup mode of overload protection is a form of foldback current limiting. The following calculations estimate the average inductor current when the converter output is shorted to the ground:

a) The time taken to discharge the capacitor from 3.2V to 2.85V is

$$t_{ssf1} = C_{32} \frac{(3.2 - 2.85)V}{37\mu A}$$

If  $C_{32} = 0.1\mu F$ ,  $t_{ssf1}$  is calculated as 0.945ms.

b) The time taken to discharge the capacitor from 2.85V to 0.5V is

$$t_{ssf2} = C_{32} \frac{(2.85 - 0.5)V}{7.5\mu A}$$

If  $C_{32} = 0.1\mu F$ ,  $t_{ssf2}$  is calculated as 31.3ms.

c) The soft start time from 0.5V to 3.2V is

$$t_{ssr} = C_{32} \frac{(3.2 - 0.5)V}{9.5\mu A}$$

When  $C_{32} = 0.1\mu F$ ,  $t_{ssr}$  is calculated as 28.4ms. Note that during soft start, the converter only starts switching when the voltage at SS/EN exceeds 1.25V.

d) The effective start-up time is

$$t_{sso} = C_{32} \frac{(3.2 - 1.25)V}{9.5\mu A}$$

The average inductor current is then

$$I_{Leff} = I_{LMcp} \frac{t_{sso}}{t_{ssf1} + t_{ssf2} + t_{ssr}}$$

$I_{Leff} \approx 0.34 I_{LMcp}$  and is independent of the soft start capacitor value. The converter will not overheat in hiccup.

**Setting the Output Voltage**

The non-inverting inputs of channel 1 and channel 2 error amplifiers are brought out as device pins (Pin 10 and Pin 8). These pins can be tied to the precision 0.5V reference output (Pin 9) of the SC2447. A simple voltage divider ( $R_{o1}$  at top and  $R_{o2}$  at bottom) sets the converter output voltage. The voltage feedback gain  $h=0.5/V_o$  is related to the divider resistors as follows:

$$R_{o2} = \frac{h}{1-h} R_{o1}$$

Once either  $R_{o1}$  or  $R_{o2}$  is chosen, the other can be calculated for the desired output voltage  $V_o$ . Since the number of standard resistance values is limited, the calculated resistance may not be available as a standard value resistor. As a result, there will be a set error in the converter output voltage. This non-random error is caused by the feedback voltage divider ratio. It cannot be corrected by the feedback loop.

The following table lists a few standard resistor combinations for realizing some commonly used output voltages.

$V_o$ (V)	<b>0.6</b>	0.9	<b>1.2</b>	<b>1.5</b>	1.8	2.5	3.3
(1-h)/h	<b>0.2</b>	0.8	<b>1.4</b>	<b>2</b>	2.6	4	5.6
$R_{o1}$ (Ohm)	<b>200</b>	806	<b>1.4K</b>	<b>2.0K</b>	2.61K	4.02K	5.62K
$R_{o2}$ (Ohm)	<b>1K</b>	1K	<b>1K</b>	<b>1K</b>	1K	1K	1K

**POWER MANAGEMENT**
**Application Information (Cont.)**

Only the voltages in boldface can be precisely set with standard 1% resistors.

From this table, one may also observe that when the value

$$\frac{1-h}{h} = \frac{V_o - 0.5}{0.5}$$

and its multiples fall into the standard resistor value chart (1%, 5% or so), it is possible to use standard value resistors to set up the exact and required output voltage value.

The input bias current of the error amplifier also causes an error in setting the output voltage. The maximum inverting input bias current of the error amplifiers is -380nA. Assuming the non-inverting input is tied to the 0.5V reference output, the percentage error in the second output voltage will be  $-100\% \cdot (0.38\mu\text{A}) \cdot$

$R_{o1}R_{o2} / [0.5 \cdot (R_{o1} + R_{o2})]$ . To keep this error below 0.2%,  $R_{o2} < 2.6\text{k}\Omega$ .

**Loop Compensation**

SC2447 uses current-mode control for both step-down channels. Current-mode control is a dual-loop control system in which the inductor peak current is loosely controlled by the inner current-loop. The higher gain outer loop regulates the output voltage. Since the current loop makes the inductor appear as a current source, the complex high-Q poles of the output LC network are split into a dominant pole determined by the output capacitor and the load resistance and a high frequency pole. This pole-splitting property of current-mode control greatly simplifies loop compensation.

The inner current-loop is unstable (sub-harmonic oscillation) unless the inductor current up-slope is steeper than the inductor current down-slope. For stable operation above 50% duty-cycle, a compensation ramp is added to the sensed-current. In the SC2447 the compensation ramp is approximately

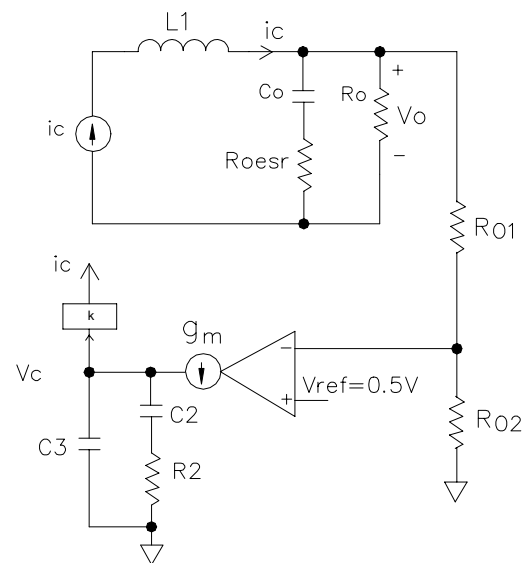
$$V_{ramp} = D * 0.4V.$$

The slope of the compensation ramp is then

$$S_e = 0.4 * f_s.$$

The slope of the internal compensation ramp is well above the minimal slope requirement for current loop stability and is sufficient for all the applications.

With the inner current loop stable, the output voltage is then regulated with the outer voltage feedback loop. A simplified equivalent circuit model of the synchronous Buck converter with current mode control is shown in Figure 15.



**Figure 15. A Simple Model of Synchronous Buck Converter with Current Mode Control**

The transconductance error amplifier (in the SC2447) has a gain  $g_m$  of  $170\mu\text{A}/\text{V}$ . The target of the compensation design is to select the compensation network consisting of  $C_2$ ,  $C_3$  and  $R_2$ , along with the feedback resistors  $R_{o1}$ ,  $R_{o2}$  and the current sensing gain, such that the converter output voltage is regulated with satisfactory dynamic performance.

**POWER MANAGEMENT****Application Information (Cont.)****PC Board Layout Issues**

Circuit board layout is very important for the proper operation of high frequency switching power converters. A power ground plane is required to reduce ground bounces. The followings are suggested for proper layout.

**Power Stage**

1) Separate the power ground from the signal ground. In the SC2447, the power ground PGND should be tied to the source terminal of lower MOSFETs. The signal ground AGND should be tied to the negative terminal of the output capacitor.

2) Minimize the size of high pulse current loop. Place the top MOSFET, bottom MOSFET and the input capacitors close to each other with short and wide traces. In addition to the aluminum energy storage capacitors, add multi-layer ceramic (MLC) capacitors from the input to the power ground to improve high frequency bypass.

**Control Section**

1) The frequency-setting resistor  $R_{osc}$  should be placed close to Pin 3. Trace length from this resistor to the analog ground should be minimized.

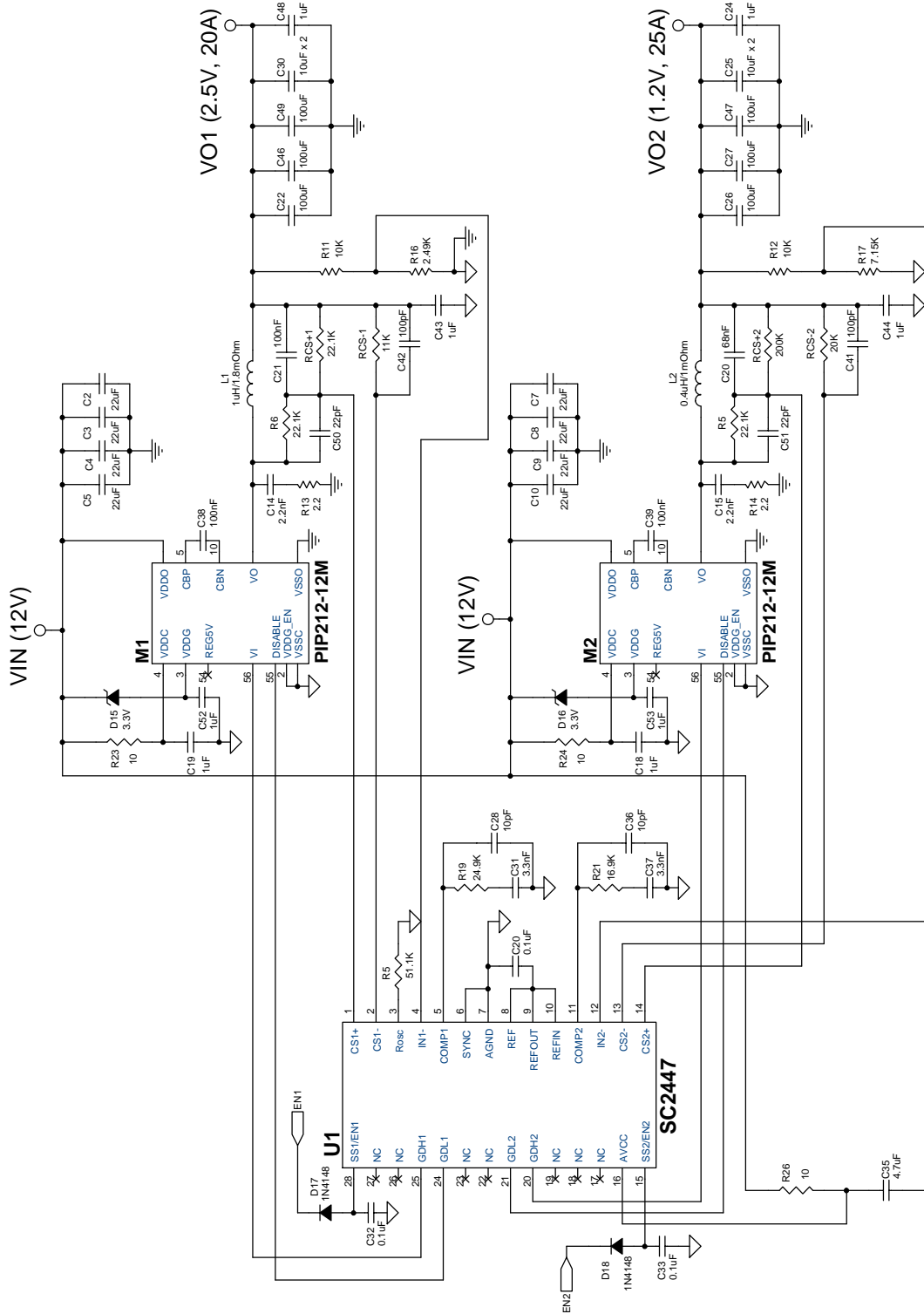
2) Solder the bias decoupling capacitor right across the AVCC and analog ground AGND.

3) Place the current sensing network away from the power circuit and close to the corresponding CS+ and CS- pins. Use X7R ceramic capacitor for the sensing capacitor because of its temperature stability.

4) Use an isolated local ground plane for the controller and tie it to the negative side of output capacitor bank.

POWER MANAGEMENT

Typical Application Schematic



$V_{IN} = 12V$   
 $V_{OUT} = 2.5V/20A, 1.2V/25A$   
 Switching Frequency = 500kHz  
 M1, M2: Philips PIP212-12M  
 L1, L2: Delta SPL146 Type Power Inductor  
 Input Capacitors: Murata GRM31CR61C226K (22uF/16V)  
 Output Capacitors: TDK C3225X6R0J107K (100uF/6.3V)  
 Murata GRM31CR60J106K (10uF/6.3V)

Figure 16. SC2447/PIP212 Two Outputs Application



### Typical Application Schematic

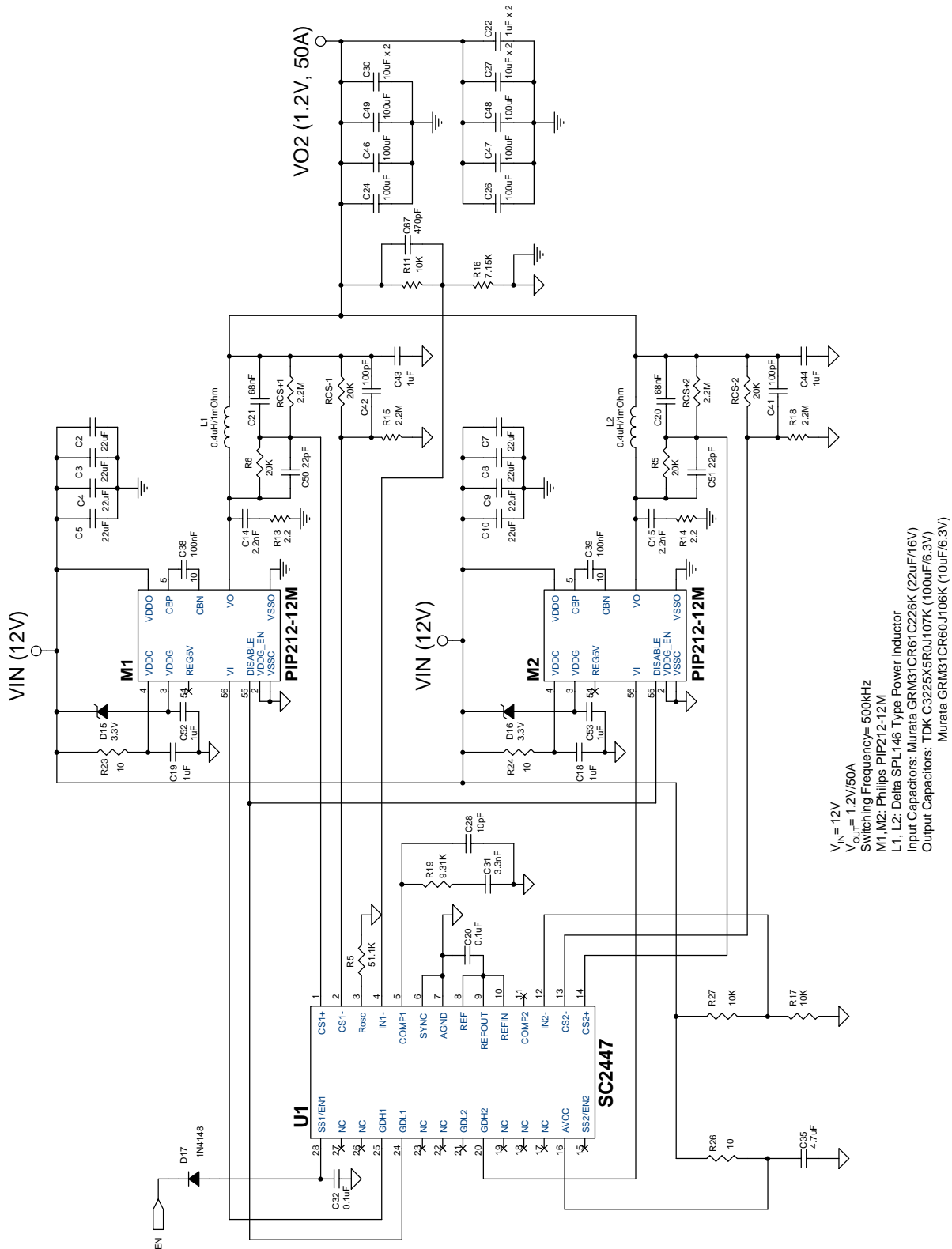
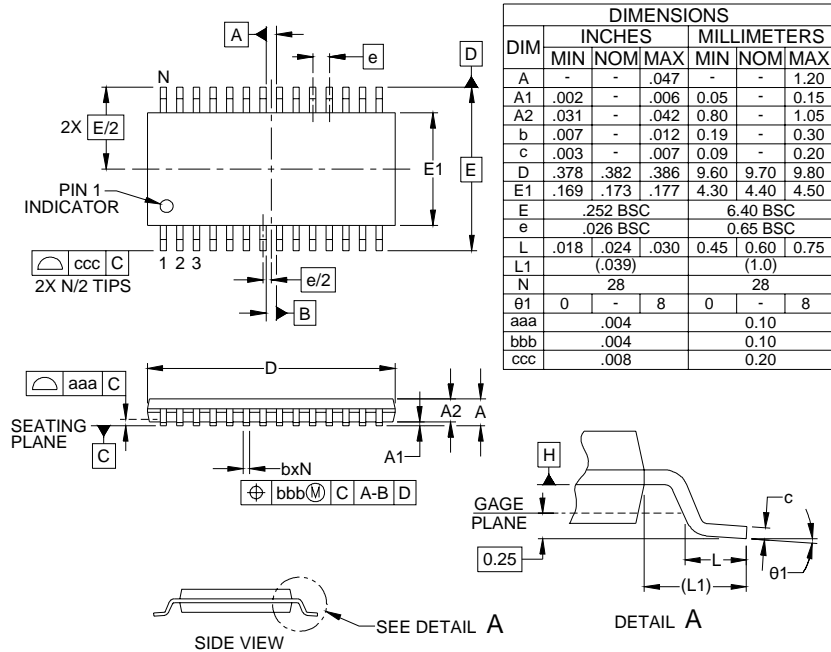


Figure 17. SC2447/PIP212 Dual-Phase Single Output Application

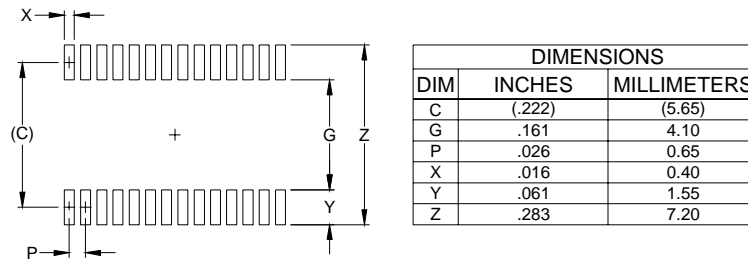
**POWER MANAGEMENT**

**Outline Drawing - TSSOP-28**



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS [-A-] AND [-B-] TO BE DETERMINED AT DATUM PLANE [-H-]
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MO-153, VARIATION AE.

**Land Pattern - TSSOP-28**



- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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