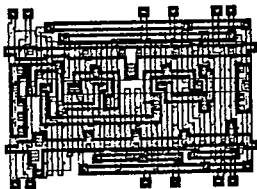


These data sheets are provided for technical guidance only. The final device performance may vary depending upon the final device design and configuration.

CMOS Standard Cells



92CS-36264

Features:

- CMOS standard cell approach
- Low-power silicon-gate CMOS technology
- Supply voltage - 5 volts
- Implements user-defined logic
- Supported by MIMIC simulation system
- Wide range of packaging capabilities
- Military temperature range
- Double-level metal
- LSTTL and CMOS compatibility

SC2500 is a GE/RCA computer-automated design approach to LSI. It is based on a group of circuit building blocks (standard cells) that can be automatically chosen, placed, and interconnected by a computer program. The standard cells are fabricated utilizing a three (3) micron coplanar oxide-isolated CMOS technology.

Standard cells are comprised of logic gates such as NAND, NOR, Exclusive-OR, transmission gates, tri-state functions, flip-flops, latches, and various input/output cells.

SC2500 provides critical path options. The placement and routing algorithms have capabilities for:

- critical placement weighting options
- critical path wire-first options which can be employed to give preference to critical timing paths.

MAXIMUM RATINGS, Absolute-Maximum Values: (Voltages referenced to V_{SS} Terminal)

| | | |
|---|-------|---------------------------------------|
| DC SUPPLY-VOLTAGE (V_{DD}) | | -0.5 to +7 V |
| RECOMMENDED DC OPERATING VOLTAGE RANGE (V_{DD}) | | 3 to 6 V |
| DC INPUT VOLTAGE RANGE, ALL INPUTS (V_{IN}) | | -0.5 to $V_{DD} + 0.5$ V |
| DC OUTPUT VOLTAGE RANGE, ALL OUTPUTS (V_{OUT}) | | -0.5 to $V_{DD} + 0.5$ V |
| DC INPUT CURRENT, ANY ONE INPUT | | ± 1 mA |
| POWER DISSIPATION PER PACKAGE (P_D): | | |
| For External Temperature Range -55 to +125°C | | |
| For $T_A = -55$ to +100°C (PACKAGE TYPE D) | | 500 mW |
| For $T_A = +100$ to +125°C (PACKAGE TYPE D) | | Derate Linearly at 12 mW/°C to 200 mW |
| POWER DISSIPATION PER OUTPUT | | 100 mW |
| OPERATING-TEMPERATURE RANGE (T_A): | | |
| PACKAGE TYPE D (CERAMIC) | | -55 to +125°C |
| STORAGE TEMPERATURE RANGE (T_{stg}) | | -65 to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | | |
| At distance 1/16 \pm 1/32 in. (1.59 \pm 0.79 mm) from case for 10 s maximum | | 265°C |

SC2500 Family

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | TEST CONDITIONS | V _{DD} (V) | LIMITS | | | | | UNITS | |
|------------------------------------|------------------------|--|--------|------|-------------------|------------|------|-------|---------|
| | | | +25°C | | | -55/+125°C | | | |
| | | | Min. | Typ. | Max. | Min. | Max. | | |
| Quiescent Device Current | I _{DD} | V _{IN} = V _{DD} or V _{SS} | 5 | — | 10 ⁻⁴ | 0.05 | — | 0.2 | μA/cell |
| Low-Level Input Voltage | V _{IL} | | 5 | — | — | 1.0 | — | 1.0 | V |
| High-Level Input Voltage | V _{IH} | | 5 | 4.0 | — | — | 4.0 | — | V |
| Low-Level Output Voltage | V _{OL} | I _{OUT} ≤ 1 μA | 5 | — | — | 0.05 | — | 0.05 | V |
| High-Level Output Voltage | V _{OH} | I _{OUT} ≤ 1 μA | 5 | 4.95 | — | — | 4.95 | — | V |
| Output Low Drive (Sink) Current | I _{OL} | | | | | | | | |
| Inv. Output Buffer (8550) | | V _O = 0.4 V | 5 | — | 1.75 | — | 0.83 | — | mA |
| Non-Inv. Output Buffer (8600) | V _O = 0.4 V | 5 | — | 3.75 | — | 1.75 | — | mA | |
| Output High Drive (Source) Current | I _{OIH} | | | | | | | | |
| Inv. Output Buffer (8550) | | V _O = 4.6 V | 5 | — | 1.25 | — | 0.59 | — | mA |
| Non-Inv. Output Buffer (8600) | V _O = 4.6 V | 5 | — | 2.75 | — | 1.30 | — | mA | |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} or V _{SS} | 5 | — | ±10 ⁻⁴ | ±0.1 | — | ±1 | μA |
| 3-State Output Leakage Current | I _{OUT} | V _{IN} = V _{DD} or V _{SS} | 5 | — | ±10 ⁻⁴ | ±0.5 | — | ±10 | μA |
| Input Capacitance | C _{IN} | | — | — | 5 | — | — | — | pF |

DYNAMIC ELECTRICAL CHARACTERISTICS

5-Volt Operation

| Number | Gate Description | Propagation Delay t _{PD} (ns) | | | |
|--------|-----------------------------|--|-------|-----------------------------|-------|
| | | Typical 25°C | | Typical 125°C | |
| | | Fanout | | Fanout | |
| | Internal Gates | 1 | 4 | 1 | 4 |
| 1120 | Two-Input NOR | 2.0 | 4.0 | 2.8 | 5.6 |
| 1220 | Two-Input NAND | 1.75 | 3.0 | 2.45 | 4.2 |
| 1240 | Four-Input NAND | 2.25 | 4.25 | 3.15 | 5.95 |
| 1410 | S-R NAND Flip-Flop | 3.0 | 4.0 | 4.2 | 5.6 |
| | Peripheral Devices | Capacitive Load (pF) | | Capacitive Load (pF) | |
| | | 15 pF | 50 pF | 15 pF | 50 pF |
| 8550 | Inverting Output Buffer | 19 | 27 | 14 | 22.4 |
| 8600 | Non-Inverting Output Buffer | 13 | 17 | 7 | 11.2 |

Cell Library

The following is a listing of the cells which are currently available in the cell library. The cells are listed by their logical functions. Additional cells are currently being designed

to enhance the library. Bulletins will periodically be published listing the new cells with their logical functions.

T-42-41

SC2500 CELL LIBRARY
LISTING BY LOGIC FUNCTION

| FUNCTION | CELL # | MIMIC PIN ORDER |
|-------------------------------------|--------|--|
| LOGIC GATES | | |
| 2-Input NOR | 1120 | I — A, B O — NOR |
| 3-Input NOR | 1130 | I — A, B, C O — NOR |
| 4-Input NOR | 1140 | I — A, B, C, D O — NOR |
| 2-Input NAND | 1220 | I — A, B O — NAND |
| 3-Input NAND | 1230 | I — A, B, C O — NAND |
| 4-Input NAND | 1240 | I — A, B, C, D O — NAND |
| 2-Input Decode Gate | 1610 | I — A, B O — NOR of A, NB |
| 2-Input AND Gate | 1620 | I — A, B O — AND |
| 3-Input AND Gate | 1630 | I — A, B, C O — AND |
| 4-Input AND Gate | 1640 | I — A, B, C, D O — AND |
| 2-Input NAND/AND Gate | 1660 | I — A, B O — NAND, AND |
| 3-Input NAND/AND Gate | 1670 | I — A, B, C O — NAND, AND |
| 4-Input NAND/AND Gate | 1680 | I — A, B, C, D O — NAND, AND |
| 2-Input OR Gate | 1720 | I — A, B O — OR |
| 3-Input OR Gate | 1730 | I — A, B, C O — OR |
| 4-Input OR Gate | 1740 | I — A, B, C, D O — OR |
| 2-Input NOR/OR Gate | 1760 | I — A, B O — NOR, OR |
| 3-Input NOR/OR Gate | 1770 | I — A, B, C O — NOR, OR |
| 4-Input NOR/OR Gate | 1780 | I — A, B, C, D O — NOR, OR |
| 3,3 AND/NOR Gate (AND-OR-Invert) | 1840 | I — A, B, C — D, E, F O — Q |
| 2, 2 AND/NOR Gate (AND-OR-Invert) | 1870 | I — A, B — C, D O — Q |
| Exclusive OR (EXOR) | 2310 | I — A, B O — EXOR |
| 2, 2 AND/NOR Gate (AND-OR-Invert) | 3870 | I — A, B — C, D O — Q |
| 8 Bit Magnitude Comparator & Enable | 4000 | I — A0, B0, A1, B1, A2, B2, A3, B3, A4, B4, A5, B5, A6, B6, A7, B7, Enab. O — Q |
| Exclusive OR (EXOR) | 4310 | I — A, B O — EXOR |

| FUNCTION | CELL # | MIMIC PIN ORDER |
|---|--------|--|
| BUFFERS/INVERTERS | | |
| Non-Inverting Buffer | 1300 | I — A O — Q |
| Inverting Buffer | 1310 | I — A O — NA |
| Low-Impedance Inverter | 1500 | I — A O — NA |
| Double Buffer Inverter | 1520 | I — A O — NA |
| High-Impedance Inverter | 1540 | I — A O — NA |
| SWITCHES | | |
| Transmission Gate | 1320 | I — CONTROL B — BUSS-A, BUSS-B |
| Single Clock Multiplexer (Trans. Gate) | 1330 | I — CONTROL B — BUSS-A, BUSS-B, COMMON BUSS |
| Inverting Tri-State | 1360 | I — DATA, CONTROL O — Q |
| Non-Inverting Tri-State | 1380 | I — DATA, CONTROL O — Q |
| Functional Jammer | 1570 | I — DATA, CLOCK O — S, R |
| Tri-State Driver | 1580 | I — DATA, CONTROL O — QN, QP |
| FLIP-FLOPS/LATCHES | | |
| RS NAND Flip-Flop | 1410 | I — NSET, NRESET O — Q, NQ |
| RS NOR Flip-Flop | 1420 | I — SET, RESET O — Q, NQ |
| R1-S1, S2 NAND Flip-Flop | 1450 | I — NSET1, NSET2, NRESET O — Q, NQ |
| R1-S1, S2 NOR Flip-Flop | 1460 | I — SET1, SET2, RESET O — Q, NQ |
| D-Type M/S Flip-Flop (Negative-Edge Clock) | 2120 | I — DATA, CLOCK O — Q, NQ |
| D-Type M/S Flip-Flop (Positive-Edge Clock) | 2130 | I — DATA, CLOCK O — Q, NQ |
| D-Type M/S Flip-Flop (Negative-Edge Clock) w/Set Overrides Reset | 2140 | I — DATA, CLOCK, SET, RESET O — Q, NQ |
| D-Type M/S Flip-Flop (Positive-Edge Clock, Zero Active Set) w/Set Overrides Reset | 2150 | I — DATA, CLOCK, SET, RESET O — Q, NQ |
| D-Type M/S Flip-Flop (Negative-Edge Clock, Zero Active Set) w/Reset Overrides Set | 2160 | I — DATA, CLOCK, SET, RESET O — Q, NQ |

SC2500 Family

1-42-41

| FUNCTION | CELL # | MIMIC PIN ORDER |
|---|--------|--|
| FLIP-FLOPS/LATCHES | | |
| D-Type M/S Flip-Flop (Positive-Edge Clock, Zero Active Set) w/Reset Overrides Set | 2170 | I — DATA, CLOCK, SET, RESET O — Q, NQ |
| D-Type M/S Flip-Flop (Positive-Edge Clock) | 2820 | I — DATA, CLOCK O — Q, NQ |
| D-Latch (Negative-Edge Clock) | 2830 | I — DATA, CLOCK O — Q, NQ |
| D-Type M/S Flip-Flop (Negative-Edge Clock) | 2920 | I — DATA, CLOCK O — Q, NQ |
| D-Latch (Positive-Edge Clock) | 2930 | I — DATA, CLOCK O — Q, NQ |
| D-Type Flip-Flop (Positive-Edge Clock) w/Reset | 4080 | I — DATA, CLOCK, RESET O — Q, NQ |
| D-Type Flip-Flop (Negative-Edge Clock) w/Reset | 4090 | I — DATA, CLOCK, RESET O — Q, NQ |
| Jammable D-Type Flip-Flop (Positive-Edge Clock) | 4110 | I — DATA, CLOCK, JAM DATA, JAM ENABLE O — Q, NQ |
| Jammable D-Type Flip-Flop (Negative-Edge Clock) | 4120 | I — DATA, CLOCK, JAM DATA, JAM ENABLE O — Q, NQ |

| FUNCTION | CELL # | MIMIC PIN ORDER |
|--|--------|--|
| INPUT/OUTPUT | | |
| Inverting Input Pad | 8530 | I — PADIN O — NPADIN |
| Inverting Input Pad | 8540 | I — PADIN O — NPADIN |
| Inverting Output Driver | 8550 | I — A O — PADOUT |
| Bi-Directional Tri-State Pad (TTL Input) | 8590 | I — DATA, ENABLE, PADIN O — DATA-IN, PADOUT |
| Non-Inverting Output Pad | 8600 | I — DATA O — PADOUT |
| Schmitt-Trigger — Inverting Input | 8630 | I — PADIN O — NPADIN |
| High-Frequency Oscillator | 8720 | I — PADIN O — NPADIN, OSCOUT |
| Low-Frequency Oscillator | 8730 | I — PADIN, DISABLE O — NPADIN, OSCOUT |
| TTL Non-Inverting Input Pad | 8920 | I — PADIN O — PADOUT |
| Bond Pad With Protection Only | 8960 | B — BONDPAD, CIRCUIT |
| Input Series Transmission Gate | 8980 | I — ENABLE O — PADIN, OUT |
| SPECIAL FUNCTIONS | | |
| <ul style="list-style-type: none"> • Static RAM • ROM • PLA • Expandable Bit-Slice Processor | | |