

High Performance Multi-Mode PWM Controller

Features

- UVLO 7.5V/17.5V
- Multi-Mode Operation
- Current Mode Control
- Low Operation Current
- Max. Operation Frequency:65KHz
- Extra Low Standby(<75mW)
- Built-in Jittering Frequency
- Internal Leading Edge Blanking
- Audio Noise Free Operation
- VDD Under Voltage Lockout With Hysteresis
- Cycle-by-Cycle Over Current Protection
- Internal Over Load Protection (OLP)
- External or Internal Over Temperature Protection (OTP)
- Output Over Voltage Protection(Output OVP)
- Internal VDD Over Voltage Protection (OVP)
- Output Short Protection (OSP)

Applications

Offline AC/DC flyback converter for

- AC/DC Adapter
- Set-Top Box Power Supplies
- Auxiliary Power Supply
- Open-frame SMPS

Typical Application

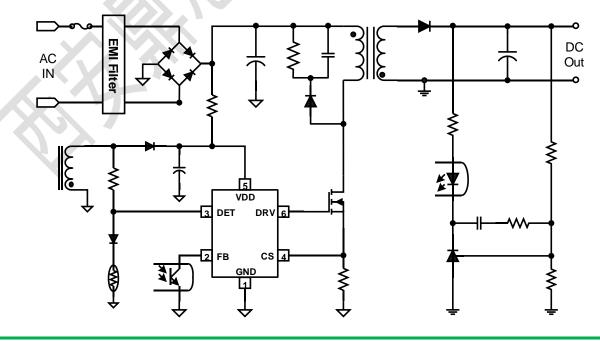
Description

SC2585A is a high performance AC/DC power supply controller which use advanced control technology to build peak current mode PWM flyback power supplies. When the load is pretty light, the device operates in 'burst mode' to minimize the standby power loss. The device operates in green mode and quasi-resonant mode at low and medium loading. At full loading, the device operates in fixed frequency mode. As a result, these different operating mode keeps high efficiency in the whole loading range.

SC2585A

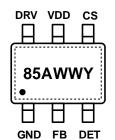
The ultra-low operating current at light load ensures that the SC2585A is ideal for applications targeting the newest regulatory standards for average efficiency and standby power.

The SC2585A is designed especially for low power purpose, furitful protection such as autorecovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD under voltage lockout (UVLO), over temperature protection (OTP), and over voltage protection (OVP). Achieved excellent EMI performance by internal frequency jitter technique.



Pin Configuration

SOT23-6 (TOP VIEW)

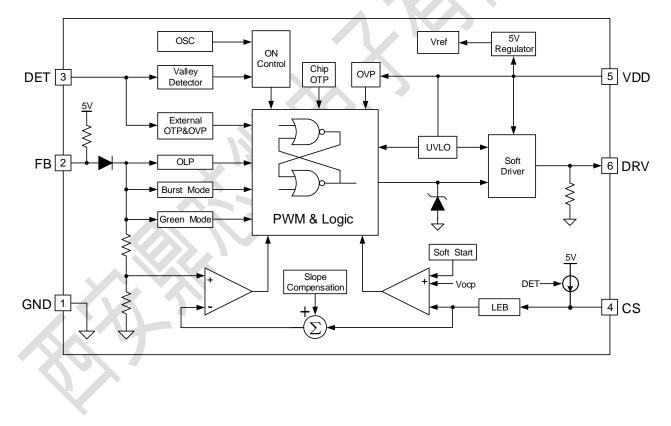


A: Version Code WW: Week Code(01-52) Y: Year Code

Ordering Information

| Part number | Pac | kage | TOP MARK | Shipping |
|-------------|---------|---------|----------|-------------|
| SC2585A | SOT23-6 | Pb-free | 85AWWY | Tape & Reel |

Block Diagram



Pin Descriptions

| Name | Pin | Description | |
|------|-----|--|--|
| GND | 1 | Ground | |
| FB | 2 | Feedback input pin | |
| DET | 3 | External protection functions detect pin | |
| CS | 4 | Current sense input | |
| VDD | 5 | Power Supply | |
| DRV | 6 | Driver output to drive the external power MOSFET | |

Absolute Maximum Ratings

| Symbol | Parameter | Min. | Max. | Unit |
|------------------|---|------|------|--------------|
| V_{DD} | DC Supply Voltage | | 30 | V |
| I _{DD} | VDD DC Clamp Current | | 10 | mA |
| V _{FB} | FB Input Voltage | -0.3 | 5.5 | V |
| V _{CS} | CS Input Voltage | -0.3 | 5.5 | V |
| V _{DET} | DET Input Voltage | -0.3 | 5.5 | V |
| R _{JA} | SOT23-6 Thermal Resistance (Junction-to-Air) | | 200 | °C /W |
| TJ | Operating Junction Temperature | -20 | 150 | °C |
| T _{STG} | Storage Temperature Range | -55 | 160 | °C |
| TL | Lead Temperature (Wave Soldering or IR,10Seconds) | | 260 | °C |
| ESD | Human Body Model, JEDEC: JESD22-A114 | | 3 | KV |
| ESD | Machine Model, JEDEC:JESD22-A115 | | 250 | V |

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device's reliability.

Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Unit |
|--------------------|---|------|------|------|
| V _{DD} | DC Supply Voltage | 10 | 26 | V |
| TA | Operating Ambient Temperature | -20 | 85 | °C |
| C _{VDD} | VDD Capacitor | 4.7 | 10 | uF |
| R _{ST_DC} | Start-up resistor Value (DC Side, Filter Capacitor) | 2000 | 4000 | KΩ |

Electrical Characteristics(T_A = 25°C, V_{DD}=18V, unless otherwise noted)

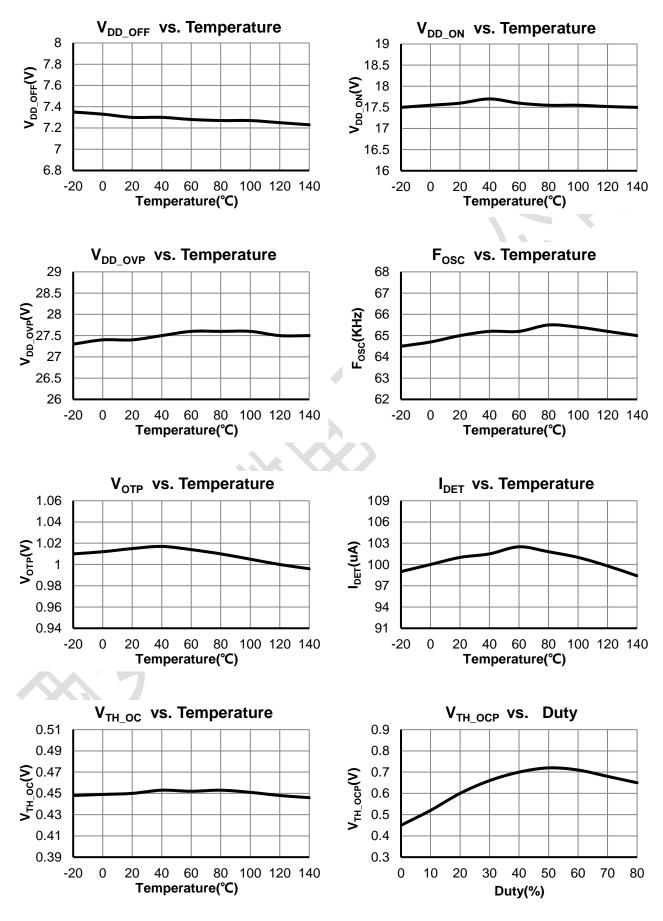
| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Unit | |
|--|---|---|----------|------|------|------|--|
| VDD Section | | | | | | | |
| V _{DD_ON} | Threshold voltage to startup | VDD Rising | 16.5 | 17.7 | 18.5 | V | |
| | Threshold voltage to cease | | <u> </u> | 7 0 | | | |
| V_{DD_OFF} | switching in normal mode | VDD Falling | 6.8 | 7.3 | 7.8 | V | |
| I _{DD_ST} | Startup current | $VDD=V_{DD_ON}-1V$ | | 2 | 5 | uA | |
| IDD_OP | Operation current | V _{FB} =3V | | 2.5 | 3.0 | mA | |
| I _{DD_standby} | Standby current | V _{CS} =0V,V _{FB} =0.5V | | 0.5 | 0.7 | mA | |
| V _{Pull-up} | Pull-up PMOS active | | | 10 | | V | |
| V_{DD_OVP} | Over voltage protection voltage | | 26.5 | 27.5 | 28.5 | V | |
| Feedback In | nput Section | | | | | | |
| V_{FB_Open} | Open loop voltage | | | 5.1 | | V | |
| V_{Ref}_{Green} | Threshold voltage enter green mode | | | 2.1 | | V | |
| $V_{\text{Ref}_\text{Burst}_\text{H}}$ | Threshold voltage exit Burst mode | | | 1.3 | | V | |
| V _{Ref_Burst_L} | Threshold voltage enter Burst mode | X | - | 1.2 | | V | |
| I _{FB_Short} | Short circuit current | Short FB pin to GND | | 0.21 | | mA | |
| Av | PWM input gain ΔVFB/ ΔVCS | | | 3.5 | | V/V | |
| D _{MAX} | Maximum duty cycle | V _{FB} =3V,V _{CS} =0.3V | 77 | 80 | 83 | % | |
| V _{TH_PL} | Power limiting FB threshold voltage | | | 4.6 | | V | |
| T _{D_PL} | Power limiting debounce time | l III | | 60 | | mS | |
| Z _{FB_IN} | Input impedance | | | 32 | | KΩ | |
| Current Ser | nse section | | | | | | |
| T _{SS} | Soft start time | | | 2.5 | | ms | |
| T _{LEB} | Leading edge blanking time | | | 330 | | ns | |
| T _{D_OC} | Delay of over current detection | | | 120 | | ns | |
| M | Current limiting threshold | | 0.42 | 0.45 | 0.47 | V | |
| V _{TH_OC} | voltage with zero duty cycle | | 0.43 | 0.45 | 0.47 | V | |
| VOCP_Clamp | Peak current limitation | | | 0.70 | | V | |
| Oscillator s | ection | | | | | | |
| f _{osc} | Normal oscillation frequency | V_{FB} =3V, V_{CS} =0V | 60 | 65 | 70 | KHz | |
| f _{JR} | Frequency jitter range | | | +/-6 | | % | |
| f _{Jitter} | Jitter frequency | | | 32 | | Hz | |
| f _{DT} | Frequency variation vs. temperature deviation | | | 5 | | % | |
| f _{DV} | Frequency variation vs. V _{DD} deviation | | | 1 | | % | |
| f _{Burst} | Burst mode switch frequency | | | 22 | | KHz | |

SC2585A

Safety-Chip

| SymbolParameterConditionsMin.Typ.Max.UnitDriver section V_{DD} V_{DD | | | | | | J | - | | |
|--|--|--------------------------|--|------|------|------|-------|--|--|
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | Symbol | Parameter | Conditions | Min. | Тур. | Max. | Unit | | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | Driver section | | | | | | | | |
| V_{DRV_Clamp} DRV clamp voltage11.0V T_R DRV rising time $C_L=1000pF$ 150nS T_F DRV falling time $C_L=1000pF$ 60nSExternal Protection Detect (DET) section I_{DET} Output current for external OTP detection90100110uA V_{OTP} Threshold voltage for external OTP0.951.001.05V I_{Output_OVP} Current threshold for adjustable output OVP175185195uA $T_{DOutput_OVP}$ Output OVP debounce time10cycle T_{OTP_EN} OTP enter150°C | V_{DRV_L} | DRV low level | V _{DD} =14V, I _O =10mA | | | 1 | V | | |
| T_R DRV rising time $C_L=1000pF$ 150nS T_F DRV falling time $C_L=1000pF$ 60nSExternal Protection Detect (DET) section I_{DET} Output current for external OTP detection90100110uA V_{OTP} Threshold voltage for external OTP0.951.001.05V I_{output_OVP} Current threshold for adjustable output OVP175185195uA $T_{DOutput_OVP}$ Output OVP debounce time010cycleChip OTP T_{OTP_EN} OTP enter OTP enter I_{50} $^{\circ}$ C | $V_{\text{DRV}_{H}}$ | DRV high level | V _{DD} =14V, I _O =10mA | 6 | | | V | | |
| TFDRV falling time $C_L=1000pF$ 60nSExternal Protection Detect (DET) section I_{DET} Output current for external OTP detection90100110uA V_{OTP} Threshold voltage for external OTP0.951.001.05V I_{Output_OVP} Current threshold for adjustable output OVP175185195uA $T_{DOutput_OVP}$ Output OVP debounce time010cycleChip OTP T_{OTP_EN} OTP enter150°C | V_{DRV_Clamp} | DRV clamp voltage | | | 11.0 | | V | | |
| External Protection Detect (DET) sectionIDETOutput current for external OTP detection90100110uAVOTPThreshold voltage for external OTP0.951.001.05VIOUTPUT_OVPCurrent threshold for adjustable output OVP175185195uATDOutput_OVPOutput OVP debounce time10cycleChip OTPTOTP_ENOTP enter150°C | T _R | DRV rising time | C _L =1000pF | | 150 | | nS | | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | T _F | DRV falling time | C _L =1000pF | | 60 | | nS | | |
| IDETOTP detection90100110uAVOTPThreshold voltage for external OTP0.951.001.05VIoutput_OVPCurrent threshold for adjustable output OVP175185195uATDOutput_OVPOutput OVP debounce time1010cycleChip OTPTOTP_ENOTP enter150°C | External Protection Detect (DET) section | | | | | | | | |
| VOTPOTP0.951.001.05VIOUTPUT_OVPCurrent threshold for adjustable output OVP175185195uATDOutput_OVPOutput OVP debounce time1010cycleChip OTPTOTP_ENOTP enter150°C | I _{DET} | | | 90 | 100 | 110 | uA | | |
| Ioutput_OVP adjustable output OVP 175 185 195 uA T_DOutput_OVP Output OVP debounce time 10 cycle Chip OTP T_OTP_EN OTP enter 150 °C | Votp | | | 0.95 | 1.00 | 1.05 | V | | |
| Chip OTP TOTP_EN OTP enter 150 ℃ | I _{Output_OVP} | | | 175 | 185 | 195 | uA | | |
| T _{OTP_EN} OTP enter 150 °C | T _{DOutput_OVP} | Output OVP debounce time | | Z | 10 | | cycle | | |
| | Chip OTP | | | | | | | | |
| T _{OTP_EX} OTP exit 120 °C | T _{OTP_EN} | OTP enter | | | 150 | | °C | | |
| | T _{OTP_EX} | OTP exit | | | 120 | | °C | | |

Typical Performance Characteristics(T_A = 25°C, V_{DD}=18V, unless otherwise noted)



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Functional Description

SC2585A is a high performance current mode PWM controller, which optimized for low standby power and cost effective offline flyback converter applications. The "burst mode" control decrease the standby power consumption and improve the efficiency, to helps the design easier to meet the international power conservation requirements.

UVLO Control

The startup current of SC2585A is designed to be ultra-low so that VDD can be quickly charged up to V_{DD_ON} and without any larger bleeding. A high value startup resistor should be used to minimize the power loss.

Start up Circuit

SC2585A offers 2.5ms soft start time, which used to soften the electrical stress during the power supply startup period. So long as VDD reaches V_{DD_ON} , the voltage of CS peak is gradually climbing from 50mV to the maximum level. Soft start take place in every restart up phase.

Quadruple Operation Mode

SC2585A applies quadruple mode for improving efficiency at light load operation.

(1). **PWM Mode:** For most of load, the device will run at traditional PWM current mode.

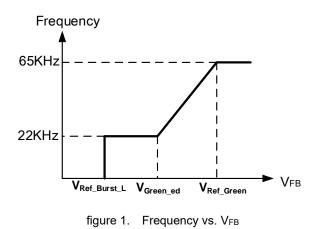
(2). Green Mode: The green mode is frequency reduction, which provide linear switching frequency reduction according to load conditions, as shown in figure 1. When the feedback voltage of FB pin is lower than V_{Ref_Green} , the switching frequency starts to decrease. When the feedback voltage of FB pin lower than V_{Green_ed} , the switching frequency is clamped at 22KHz. This frequency reduction mode function reduces power consumption under light load conditions, and easily meets even the strictest regulations.

(3). Burst Mode: During light load, switching loss will dominate the power efficiency. This mode is to cut switching loss. As shown in figure1, when the output load gets light, feedback signal drops and touched $V_{Ref_Burst_L}$, PWM signal will be blanked

and system ceases to switch. After Vout drops and feedback signal goes back to $V_{Ref_Burst_H}$, switching will be resumed.

(4). VDD Holdup Mode: Under light load or load transient moment, feedback signal will drop and touch V_{Ref Burst L}. Then PWM signal will be blanked and system stop to switch. VDD could drop down to turn off threshold voltage V_{DD OFF}. To avoid this, when VDD drops to a setting threshold, 9.0V, the hysteresis comparator will bypass PWM and burst mode loop and forces switching at a very low level to supply energy to VDD. VDD holdup mode is also improved to holdup VDD by less switching cycles. This mode is very useful in reducing start up resistor while still get start-up time in spec. It's not likely for VDD to touch UVLO turn off threshold during any light load condition. This will also makes bias winding design and transient design easier. Furthermore, VDD holdup mode is only designed to prevent VDD from tounching turn off threshold voltage under light load or load transient moment. Comparing with burst mode, the VDD holdup mode brings higher switching. Hence, it's recommended that the system should be designed to not to operate at this mode during light load or no load conditions.

To be noticed, in Green Mode and Burst Mode, the device is working in quasi-resonant mode(valley on), which inprove power efficiency.





Oscillator

To gurarantee precise frequency, it's trimmed to 5% tolerance. It also generates slop compensation saw–tooth, 80% maximum duty cycle pulse.it can typically operate at built-in 65KHz center frequency and features frequency jitting function.it's jitting depth is 6% with about 2.5ms envelope frequency at 65KHz.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in SC2585A current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Slope Compensation

internal slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. it greatly improves the system stability at CCM and prevents the sub-harmonic oscillation.

External Output OVP and External OTP

External Output OVP and OTP are detected as shown in the figure 2.

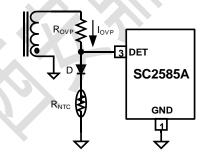


figure 2. DET pin function detect circuit

For Output OVP detection, if lovp is larger than 185uA (typical), OVP auto-recovery protection is triggered after 10 pwm cycles debounce. By selecting proper Rovp resistance, Output OVP level can be programmed.

$$I_{OVP} = \frac{(V_O + V_D) \times \frac{N_{AUX}}{N_S}}{R_{OVP}} > 185uA$$

Vo: Output voltage

 N_{S} : The secondary winding turns N_{AUX} : The auxiliary winding turns

For external OTP detection, there is an expression as below.

$$\Delta V_{OTP} = \frac{R_{NTC} \times R_{OVP}}{R_{NTC} + R_{OVP}} \times 100 uA$$

When ΔV_{OTP} <1.0V, external OTP auto-recovery protection is triggered after 50 PWM cycles debounce.

Gate Driver

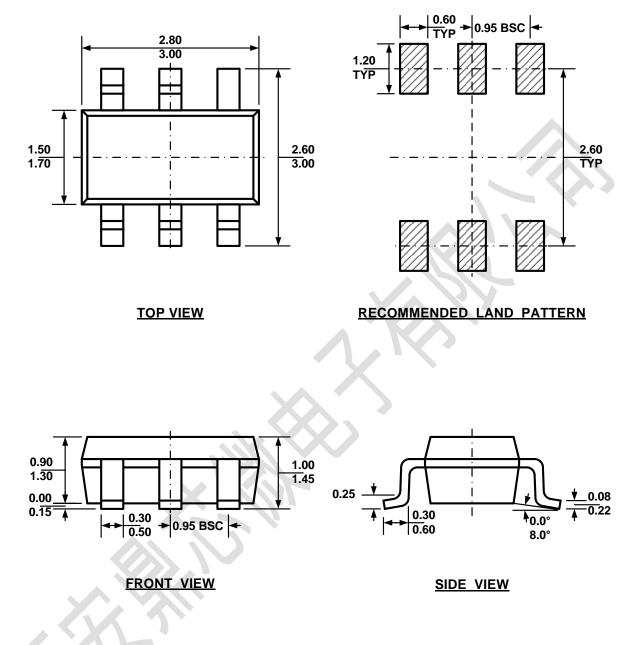
A totem pole gate driver is fine tuned to meet both EMI and efficiency requirement in low power application. An internal pull low circuit is activated after pretty low VDD to prevent external MOSFET from accidientally turing on during UVLO.

Protection

SC2585A provide fruitful protection functions that intend to peotect system from being damaged.which are auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP), VDD and output Over Voltage Protection (OVP).

Package Information

SOT23-6



Note:

- 1. All dimensions are in millimeters
- 2. Package length does not include mold flash protrusion or gate burr
- 3. Package WIDTH does not include mold flash protrusion
- 4. Drawing is not to scale
- 5. Pin 1 is lower left pin when reading top mark from left to right

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