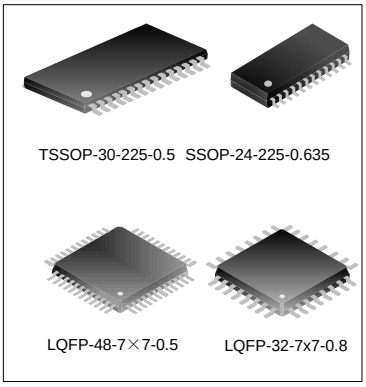
Cortex-M0 MCU WITH ENHANCED PWM AND ADC

DESCRIPTION

SC32F5632(64) is a high performance microcontroller which is designed intended for motor control and digital power applications. It uses Cortex-M0 core with maximum operating frequency 64MHz. and ADC sample rate up to 1Msps. A Co_ processor unit can meet a variety of multiplication, division, shift operation.

SC32F5632(64) supports single power, and intigrates high precision high speed and low speed oscillators, and supports a variety of low power mode. The integration of multi-channel enhanced PWM, analog comparator and multi-channel high speed operational amplifier, make it suitable for a variety of motor application and minimize the system cost.



APPLICATION

- PMSM controller
- BLDC controller
- Universal/private frequency converter
- AC-DC inverter
- Digital control power supply

FEATURES

ARM 32bit Cortex-M0

- Running at frequencies of up to 64 MHz
- Built-in Nested Vectored Interrupt Controller (NVIC)
- Serial Wire Debug(SWD)
- Supports single cycle 32bit*32bit multiplication operations
- Support 6 channel DMA controller
- Support MAC、DIV function

Memory

- Up to 64 KB on-chip flash programming memory, data retention >10 years.
- Up to 6 KB SRAM, with parity check

Development support

- Serial Wire Debug（SWD）
- Support MEMORY and peripheral protection

Power supply and Reset

- Operating voltage：2.0V~5.5V
- Built-in MVR,1.5V or 1.7V selectable; normal and low power mode selectable
- Built-in Power-On-Reset (POR)
- Built-in Low-Voltage-Reset (LVR) with 4 reset points optional :2.3V，2.7V，3.7V，4.1V
- Built-in Low-Voltage-Detect (LVD) with 8 levels optional: 2.4V，2.7V，3.0V，3.3V，3.6V，3.9V，4.2V，

4.5V

Clock generation unit

- Crystal oscillator with an operating range of 1MHz to 16 MHz
- 32KHz Internal RC (IRC) oscillator
- 16 MHz Internal RC (IRC) oscillator trimmed to 1% accuracy @-10~50℃
- PLL supports up to 96MHz

GPIO

- Up to 42 General Purpose I/O (GPIO) pins
- Programmable pull-up resistor, open-drain mode, programmable digital input glitch filter, and programmable input inverter.
- Programmable output drive on all GPIO pins.
- All GPIO pins can be used as edge and level sensitive interrupt sources.

Timer

- One 16-bit Timer0 with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- One 32-bit Timer6 with 2 independent timers
- 16-bit, motor control PWM timer with deadtime generation and emergency stop
- 2 watchdog timers (Independent and Window)
- SysTick timer 24-bit downcounter

Serial Communication interface

- 2-channel UART
- 1-channel SPI (12Mbit/s)

Analog Modules

- 2-channel rail to rail CMP0 and CMP10, input hysteresis optional
- Up to 3 channel general amplifier, both input and output are open
- 1-channel 12bit ADC, 16 channel inputs, maximum conversion rate is 1Msps

Operating Mode

- Normal operating mode
- IDLE mode
- STOP mode

Operating Temperature

- -40~105°C

Package Type

- LQFP-48
- TSSOP-30
- LQFP-32
- SSOP-24

ORDERING INFORMATION

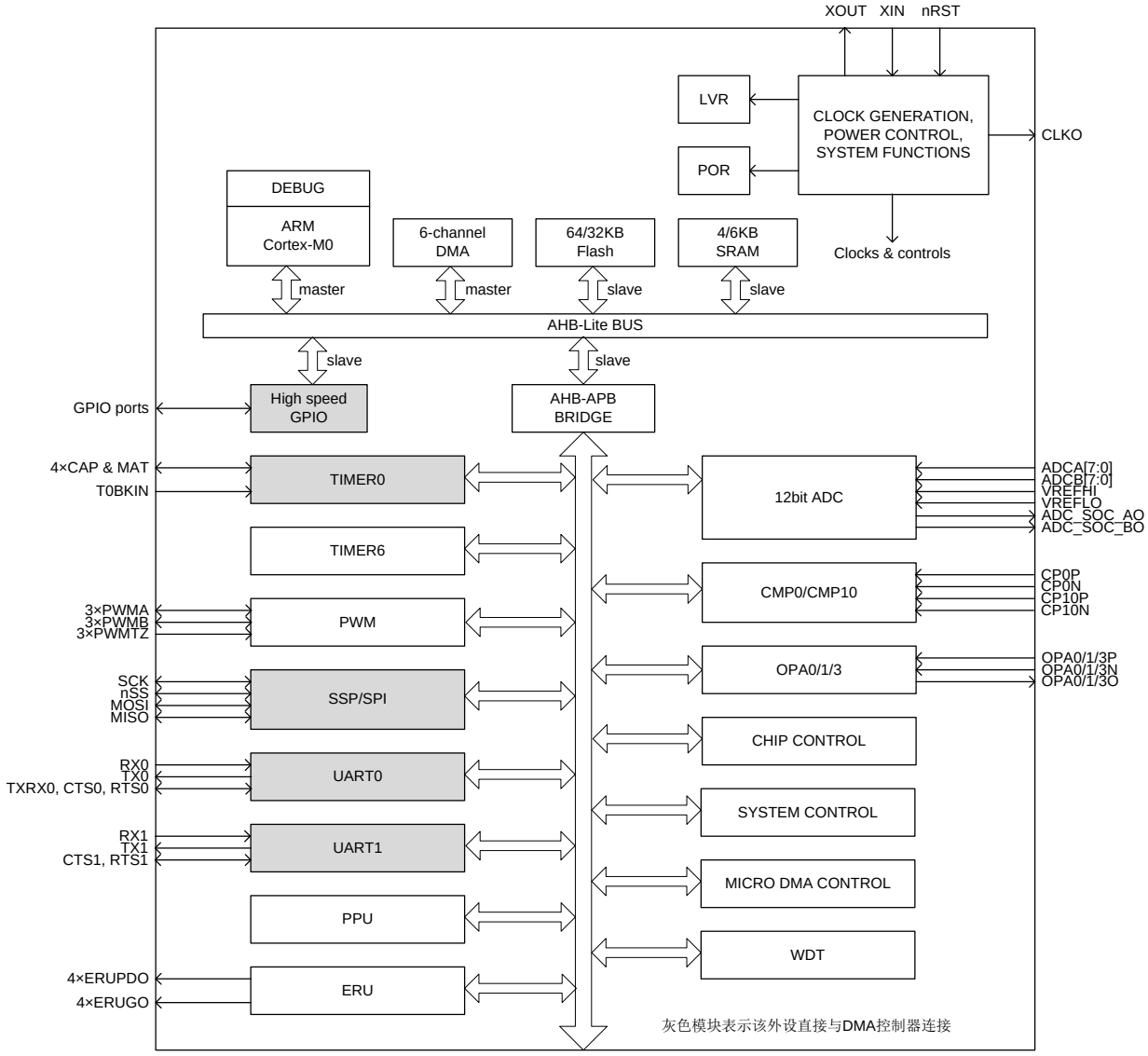
ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SC32F5632LL1G	LQFP-48-7x7-0.5	5632LL1G	Halogen free	Tray
SC32F5664LL1G	LQFP-48-7x7-0.5	5664LL1G	Halogen free	Tray
SC32F5632LF1G	LQFP-32-7x7-0.8	5632LF1G	Halogen free	Tray
SC32F5664LL1G	LQFP-32-7x7-0.8	5664LF1G	Halogen free	Tray
SC32F5632JV1G	TSSOP-30-225-0.5	5632JV1G	Halogen free	Tube
SC32F5632JV1GTR				Tape&Reel
SC32F5664JV1G	TSSOP-30-225-0.5	5664JV1G	Halogen free	Tube
SC32F5664JV1GTR				Tape&Reel
SC32F5632RE1G	SSOP-24-225-0.635	5632RE1G	Halogen free	Tube
SC32F5632RE1GTR				Tape&Reel

RESOURCE INFORMATION

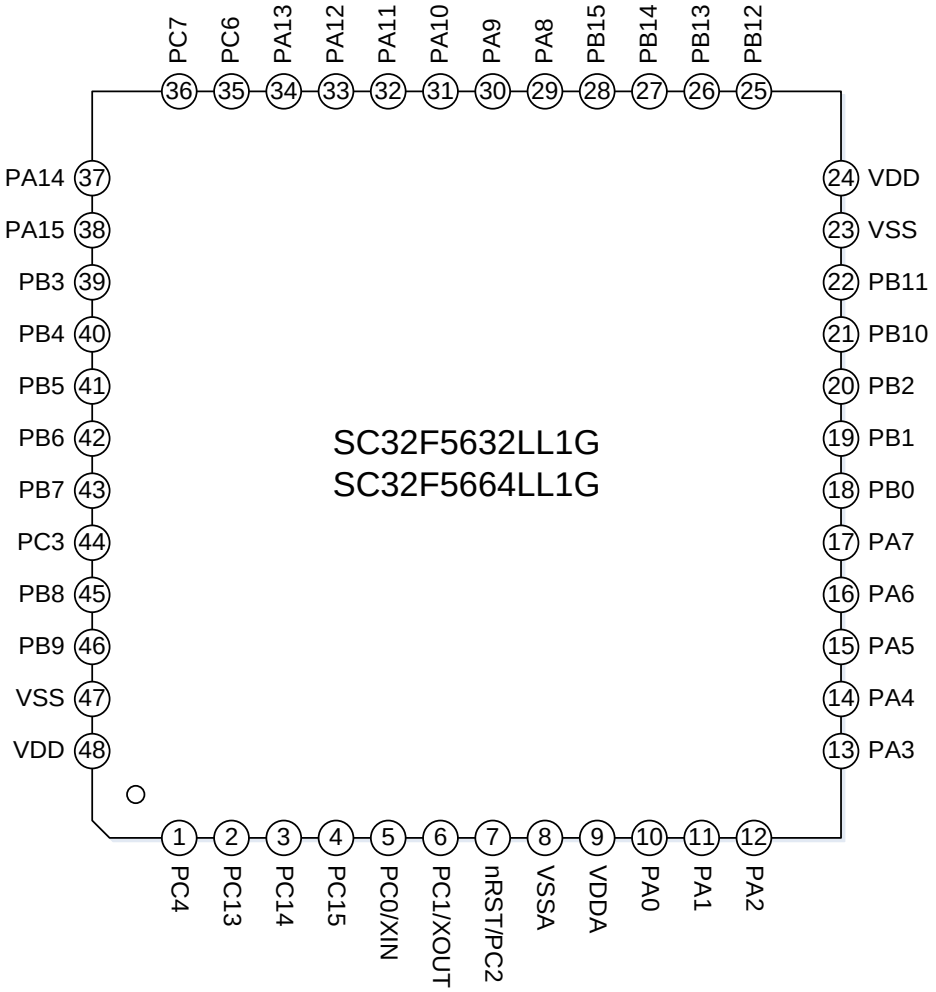
Feature	SC32F5632 RE1G	SC32F5632 JV1G	SC32F5632 LF1G	SC32F5632 LL1G	SC32F5664 JV1G	SC32F5664 LF1G	SC32F566 4LL1G
FLASH	32K Byte	32K Byte	32K Byte	32K Byte	64K Byte	64K Byte	32K Byte
RAM	4K Byte	4K Byte	4K Byte	4K Byte	6K Byte	6K Byte	4K Byte
I/O	22	26	26	42	26	26	42
T0	1	1	1	1	1	1	1
T6	2	2	2	2	2	2	2
PWM	3*2	3*2	3*2	3*2	3*2	3*2	3*2
ACMP	2	2	2	2	2	2	2
OPA	2	3	3	3	3	3	3
ADC	9ch	10ch	10ch	16ch	10ch	10ch	16ch
UART	2	2	2	2	2	2	2
SPI	--	1	1	1	1	1	1

BLOCK DIAGRAM

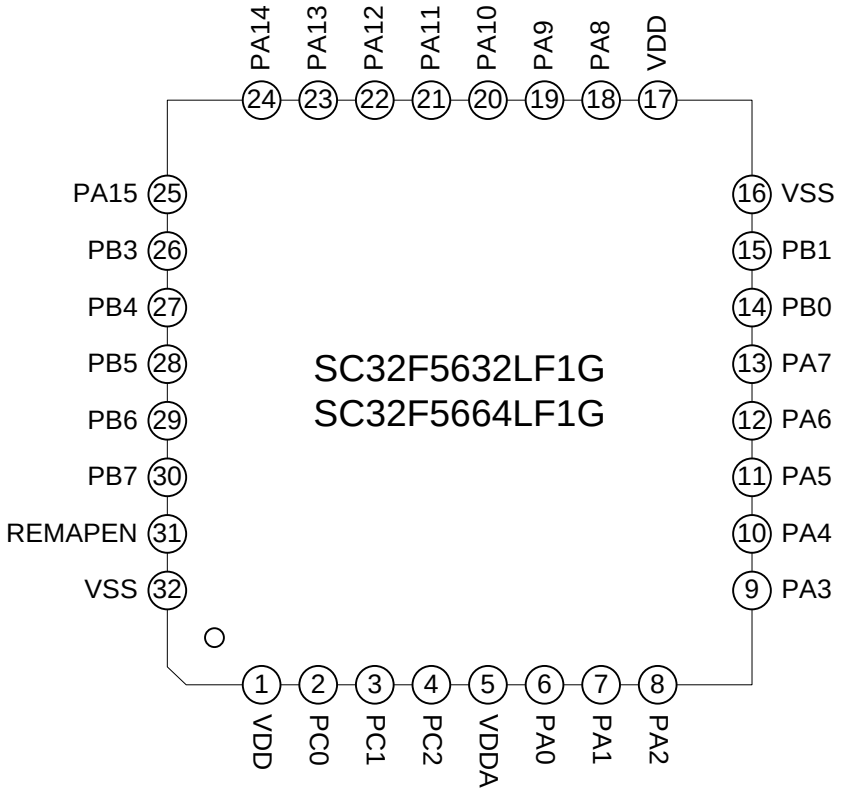


PIN CONFIGURATION

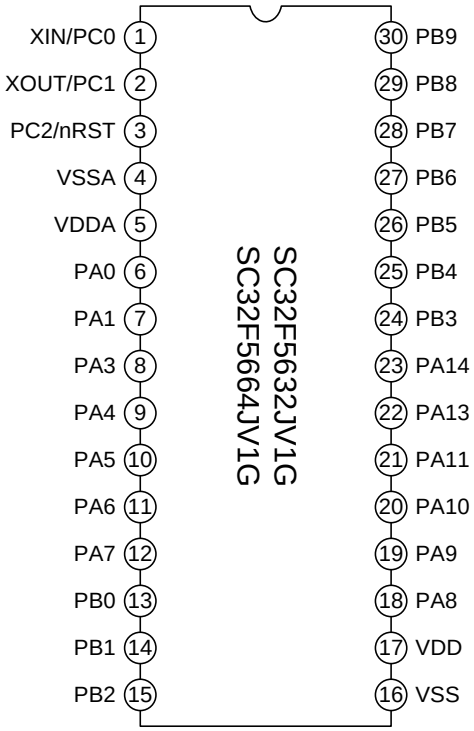
LQFP-48:SC32F5632/64LL1G



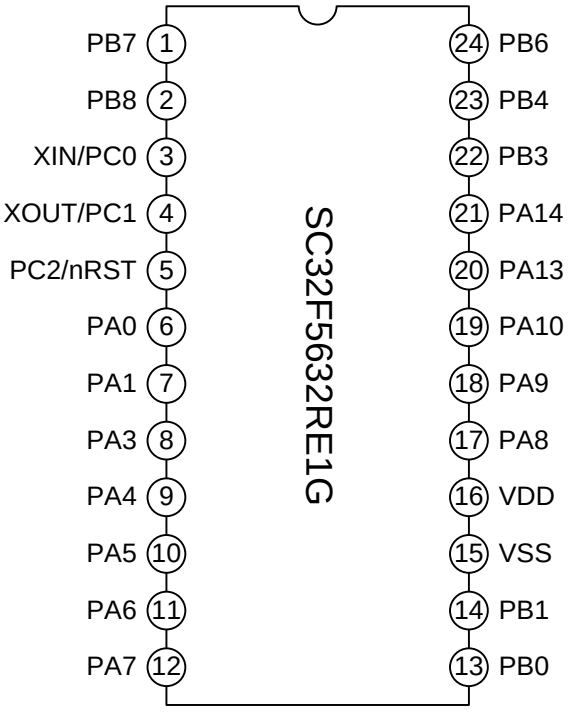
LQFP-32：SC32F5632/64LF1G



TSSOP-30：SC32F5632/64JV1G



SSOP-24：SC32F5632RE1G



PIN DESCRIPTION

PIN MULTIPLEX

-LL	-LF	-JV	-RE	Power	Digital								Analog		
					ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT0	ALT1	ALT2
1	--	--	--	--	PC4	PWM2B	PWM1B	--	--	T0ETR	ERU1PDO	ERU1GO	--	--	--
2	--	--	--	--	PC13	PWM0A	PWM1A	--	UART0RX	T0CH3	UART1_RX	--	ADCB7	--	--
3	--	--	--	--	PC14	PWM1A	PWM2B	--	UART0TX	T0CH3N	UART1TX	--	ADCA7	--	--
4	--	--	--	--	PC15	PWM2A	PWM2A	--	--	T0CH4	--	--	ADCA6	--	--

5	2	1	3	XIN	PC0	T0CH3	--	--	--	PWMTZ1	ERU0PDO	ERU0GO	--	--	--
6	3	2	4	XOUT	PC1	--	--	--	--	XCLKOUT	EXTSYNO	--	--	--	--
7	4	3	5	NRST	PC2	--	--	--	--	--	--	--	--	--	--
8	--	4	--	VSSA	--	--	--	--	--	--	--	--	--	--	--
9	5	5	--	VDDA	--	--	--	--	--	--	--	--	--	--	--
10	6	6	6	--	PA0	UART0CTS	UART1CTS	--	--	--	--	--	ADCA5	OPA0P	CP0P
11	7	7	7	--	PA1	UART0RTS	UART1RTS	--	--	--	--	--	ADCA4	OPA0N	CP0N
12	8	--	--	--	PA2	UART0TX	UART1TX	UART0TXRX	--	XCLKINA	--	--	ADCA3	OPA0O	--
13	9	8	8	--	PA3	UART0RX	UART1RX	T0CH2	--	--	--	--	ADCA2	OPA3P	--
	--	--	--	VDD	--	--	--	--	--	--	--	--	--	--	--
14	10	9	9	--	PA4	--	--	--	--	SPI0NSS	--	--	ADCA1	OPA3N	--
15	11	10	10	--	PA5	--	--	--	--	SPI0SCK	--	--	ADCA0	OPA3O	VREFHI
16	12	11	11	--	PA6	PWMTZ0	PWMTZ2	T0CH1	--	SPI0MISO	T0BKIN	--	ADCB0	--	VREFLO
17	13	12	12	--	PA7	PWM0B	--	T0CH2	--	SPI0MOS	T0CH1N	--	ADCB1	--	--

										I					
18	14	13	13	--	PB0	PWM0A	--	T0CH3	--	--	T0CH2N	--	ADCB2	--	--
19	15	14	14	--	PB1	PWM1B	--	T0CH4	--	--	T0CH3N	--	ADCB3	ELVI	--
20	--	15	--	--	PB2	--	--	--	--	XCLKOUT	--	--	ADCB4	--	--
21	--	--	--	--	PB10	--	--	--	--	--	ERU2PDO	ERU2GO	ADCB5	--	--
22	--	--	--	--	PB11	--	--	--	--	--	--	--	ADCB6	--	--
23	16	16	15	VSS	--	--	--	--	--	--	--	--	--	--	--
24	17	17	16	VDD	--	--	--	--	--	--	--	--	--	--	--
25	--	--	--	--	PB12	PWMTZ0	--	SPI0NSS	T0BKIN	--	--	--	--	--	--
26	--	--	--	--	PB13	PWM0B	PWM0B	SPI0SCK	T0CH1N	--	--	--	--	--	--
27	--	--	--	--	PB14	PWM1B	PWM0A	SPI0MISO	T0CH2N	--	T0CH1	--	--	--	--
28	--	--	--	--	PB15	PWM2B	PWM1B	SPI0MOSI	T0CH3N	--	T0CH1N	T0CH2	--	--	--
29	18	18	17	--	PA8	PWM0A	PWM1A	--	T0CH1	--	--	--	--	--	--
30	19	19	18	--	PA9	PWM1A	PWM2B	UART0TX	T0CH2	--	--	T0BKIN	--	--	--
31	20	20	19	--	PA10	PWM2A	PWM2A	UART0RX	T0CH3	--	--	--	--	--	--
32	21	21	--	--	PA11	--	PWMTZ0	UART0CTS	T0CH4	SPI0NSS	T0CH1	T0CH1	--	--	--
33	22	--	--	--	PA1	--	--	UAR	T0E	SPI0	UAR	T0C	--	--	--

					2			T0RTS	TR	SCK	T0RX	H1N			
34	23	22	20	--	PA13	SPDAT	IR_OUT	UART0RX	--	--	--	--	--	--	--
35	--	--	--	--	PC6	--	--	UART0TX	UART0TXRX	EXTSYNO	ERU3PDO	ERU3GO	--	--	--
36	--	--	--	--	PC7	--	--	--	--	--	--	--	--	--	--
37	24	23	21	--	PA14	SPCLK	--	UART0TX	UART1TX	--	--	--	--	--	--
38	25	--	--	--	PA15	--	SPI0NSS	UART0RX	UART1RX	EXTSYNI	ERU1PDO	ERU1GO	--	--	--
39	26	24	22	--	PB3	PWMTZ1	SPI0SCK	--	XCLKOUT	--	--	--	--	OPA1P	--
40	27	25	23	--	PB4	T0CH1	SPI0MISO	--	--	--	--	--	--	OPA1N	--
41	28	26	--	--	PB5	T0CH2	SPI0MOSI	--	--	--	--	--	--	OPA1O	--
42	29	27	24	--	PB6	T0CH3	--	UART1TX	--	T0CH1	--	--	--	--	CP10P
43	30	28	1	--	PB7	T0CH4	--	UART1RX	--	T0CH1N	--	--	--	--	CP10N
44	--	--	--	--	PC3	--	--	XCLKINB	EXTSYN	--	ERU0PD	ERU0GO	--	--	--

									O		O				
45	--	29	2	--	PB8	--	--	T0CH4	EXTSYNI	T0CH2	--	--	--	--	--
46	--	30	--	--	PB9	--	PWMTZ2	IR_OUT	--	T0CH2N	--	--	--	--	--
--	31	--	--	REMAPEN	--	--	--	--	--	--	--	--	--	--	--
47	32	--	--	VSS	--	--	--	--	--	--	--	--	--	--	--
48	1	--	--	VDD	--	--	--	--	--	--	--	--	--	--	--

PIN DESCRIPTION

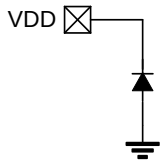
I/O	Pin Type	Function Description
PORT		
PA.0-PA.15	I/O	16-bit bidirectional I/O ports, bit operation available
PB.0-PB.15	I/O	16-bit bidirectional I/O ports, bit operation available
PC.0-PC.15	I/O	16-bit bidirectional I/O ports, bit operation available
SYSTEM		
NRST	I	External reset input, low voltage active
XIN	I	External oscillator input
XOUT	O	External oscillator output
XCLKOUT	O	Internal clock output
EXTSYNO	O	PWM synchronous pulse output
EXTSYNI	I	PWM synchronous pulse input
ELVI	I	External low voltage detect pin
REMAPEN	I	When REMAPEN connected to ground, MCU starting from EFLASH
TIMER		
T0CH1~T0CH4	I/O	Timer0 capture input and output (positive end)
T0CH1N~T0CH4N	I/O	Timer0 capture input and output (negative end)
T0BKIN	I	Timer0 brake input
IR_OUT	O	Carrier output
PWM		
PWM0A	O	PWM0 A channel output
PWM0B	O	PWM0 B channel output
PWM1A	O	PWM1 A channel output

I/O	Pin Type	Function Description
PWM1B	O	PWM1 B channel output
PWM2A	O	PWM2 A channel output
PWM2B	O	PWM2 B channel output
PWMTZ0~ PWMTZ2	I	PWM brake input(emergency brake)
COMMUNICATION INTERFACE		
SPI0NSS	I/O	SPI enable pin
SPI0SCK	I/O	SPI clock input
SPI0MISO	I/O	SPI master input/slave output
SPI0MOSI	I/O	SPI master output/slave input
SPI0IO	I/O	3 wire mode SPI data line
UART0CTS	I	UART0 send clear
UART0RTS	O	UART0 send request
UART0RXTX	I/O	UART0 half-duplex UART data line
UART0TX	O	UART0 data output
UART0RX	I	UART0 data input
UART1TX	O	UART1 data output
UART1RX	I	UART1 data input
Analog comparator		
CP0P	I	Comparator0 positive input
CP0N	I	Comparator0 negative input
CP10P	I	Comparator10 positive input
CP10N	I	Comparator10 negative input
Amplifier		
OPA0P	I	OPA0 positive input
OPA0N	I	OPA0 negative input
OPA1P	I	OPA1 positive input
OPA1N	I	OPA1 negative input
OPA3P	I	OPA3 positive input
OPA3N	I	OPA3 negative input
OPA0O	O	OPA0 output
OPA1O	O	OPA1 output
OPA3O	O	OPA3 output
ADC		
ADCA0~ ADCA7	I	ADC A channel input
ADCB0~ ADCB7	I	ADC B channel input
VREFHI	I	ADC reference voltage high
VREFLO	I	ADC reference voltage low

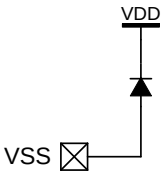
I/O	Pin Type	Function Description
ERU		
ERU0PDO	O	ERU0 voltage signal output
ERU0GO	O	ERU0 gate control signal output
ERU1PDO	O	ERU1 voltage signal output
ERU1GO	O	ERU1 gate control signal output
ERU2PDO	O	ERU2 voltage signal output
ERU2GO	O	ERU2 gate control signal output
ERU3PDO	O	ERU3 voltage signal output
ERU3GO	O	ERU3 gate control signal output
Power		
VDD	P	Power
VSS	P	Ground
VDDA	P	Analog power
VSSA	P	Analog ground

Notes： In Pin Type column: “P” denotes Power pins, “I/O” denotes normal input/output pins, “I” denotes input pins, “O” denotes output pins; “A” denotes analog pin.

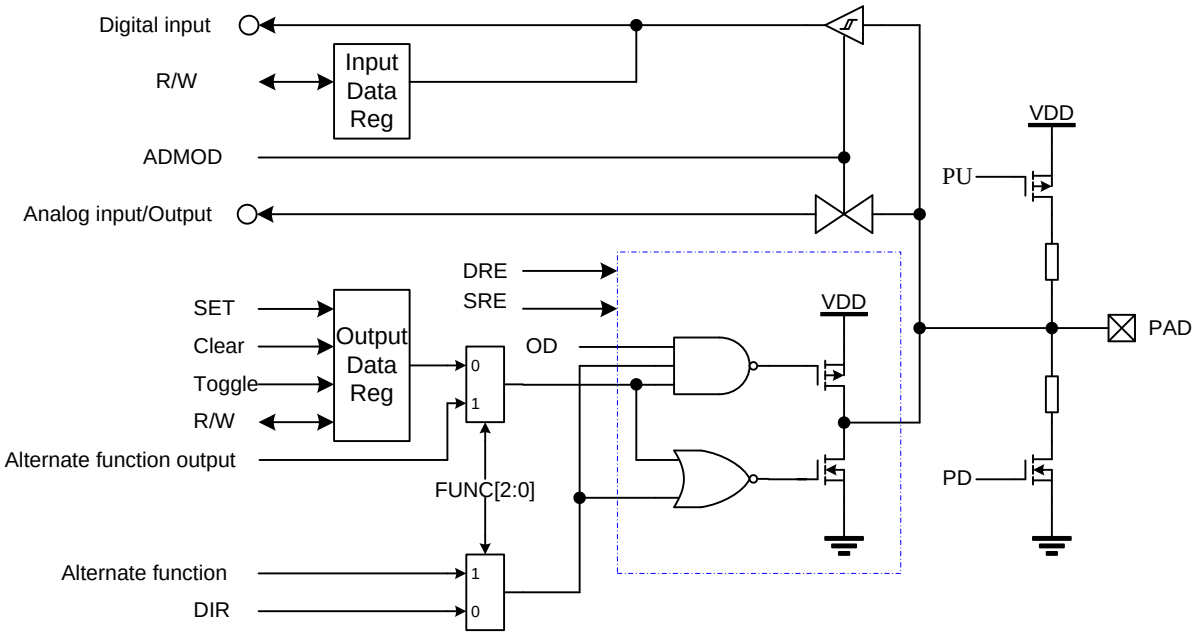
PIN STRUCTURE



VDD structure



VSS structure



GPIO structure

ABSOLUTE MAXIMUM RATINGS

Device may cause permanent damage if operating condition exceeds the “absolute maximum ratings”. We don’t recommend customer to operate device out of the range. If device works in absolute maximum condition for long time, reliability will be affected.

Power supply characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	-0.3	-	6.0	V
Kernel voltage	V_{CORE}	-	-0.3	1.5/1.7	2.0	
Input voltage	V_{IN}	-	-0.3	-	V_{DD}+0.5	

Note：All voltage are referenced by V_{SS}.

Current characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Total current flowing into VDD	I_{VDD}	-	-	-	100	mA
Total current flowing out of VSS	I_{VSS}	-	-	-	100	
Pin injection current	I_{INJ}	$V_{IN}>V_{DD}$ 或 $V_{IN}<V_{SS}$	-4	-	4	
		$V_O>V_{DD}$ 或 $V_O<V_{SS}$	-4	-	4	
Total injection current	ΣI_{INJ}	-	-20	-	20	

Thermal characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Ambient temperature	T_A	-	-40	-	105	°C
Storage temperature	T_{STG}	-	-55	-	125	
Junction temperature	T_J	-	-	-	150	
Thermal resistance	θ_{JA}	TSSOP-30-225-0.5	-	68	-	°C /W
		SSOP-24-225-0.635	-	130	-	
		LQFP-48-7*7-0.5	-	78	-	
		LQFP-32-7*7-0.8	-	89	-	
Total power consumption	P_D	-	-	-	500	mW

Note：Thermal resistance is related with package form, PCB board design, ambient wind speed and power consumption.

Recommend working condition

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	2.0	5.0	5.5	V
CPU frequency	F_{CPU}	V_{DD}=2.7~5.5V	-	48	64	MHz

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the typical values are the test results at VDD=5.0V, T_A =25°C

Unless otherwise specified, the max. and min. values are the test results at ambient temperature(T_A=25°C)

Current characteristic

Obey the following conditions when measuring current characteristic:

* All IO are set output low voltage, no load.
* Unless otherwise specified, all peripherals are closed.

Table 1：Power supply characteristic

Symbol	Characteristic	Test condition			Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	M_{CLK} = RCH=16MHz			2.0	--	5.5	V
		M_{CLK} = RCH+PLL=64MHz			2.7	--	5.5	
I_{DD}	Operating current, considering the temperature	RCH provides system clock	MClk=16MHz	V_{DD}=5.0	--	2.2	--	mA
		CRYH provides system clock, min. gain	MClk=16MHz	V_{DD}=5.0	--	3.5	--	
		RCH+PLL	MClk=48MHz	V_{DD}=5.0	--	8	--	
		RCL provides system clock	MClk=F_{RCL}	V_{DD}=5.0	--	170	--	uA
	Note: when one clock is working, others are off, except HSPLL, because it depends on RCH or CRYH input.							
I_{IDLE}	IDLE current	RCH provides system clock	MClk=16MHz	V_{DD}=5.0	--	1.0	--	mA
		CRYH provides system clock, min. gain	MClk=16MHz	V_{DD}=5.0	--	2.2	--	
		RCH+PLL	MClk=48MHz	V_{DD}=5.0	--	4.8	--	
		RCL provides system clock	MClk=F_{RCL}	V_{DD}=5.0	--	150	--	uA
I_{STOP}	STOP current	LVR ON		V_{DD}=5.0	--	60	--	uA
		LVR OFF		V_{DD}=5.0	--	45	--	

Note：Typical values are results of sampling test, not tested in mass production.

Table 2：Module operating current

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
RCL operating current	I_{RCL}^*		--	1	--	uA
RCH operating current	I_{RCH}^*		--	190	--	uA
CRYH(1M) module operating current	I_{CRYH}^*	Min. gain	--	0.2	--	mA

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
CRYH(16M) module operating current	I_{CRYH}*	Min. gain	--	1.2	--	mA
LVD operating current	I_{LVD}*		--	15	--	uA
LVR operating current	I_{LVR}*		--	15	--	uA
HSPLL module operating current	I_{PLL1}*		--	1	--	mA
ADC operating current	I_{ADC}*	AD continuous working @MClk=24MHz	--	4	--	mA
OPA0/1/3 operating current	I_{OPA}*	On, internal 1X follow @each OPA	--	1.5	--	mA
CMP0/CMP10 operating current	I_{CMP0}*		--	15	--	uA

Note： The suffix * parameter refers to the simulated value, without testing

IO characteristic

Table 3：IO characteristic

Characteristic	Symbol	Test condition		Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C；Full temperature working condition: -40～105°C							
High input voltage	V_{IH}	All IO		$0.7V_{DD}$	--	V_{DD}	V
Low input voltage	V_{IL}	All IO		0	--	$0.3V_{DD}$	V
Driving condition when V_{DD}=5.0V							
Output pin source current	I_{OH}	V_{OH}=0.9V_{DD}	All IO DS=0	--	4.7	--	mA
			All IO DS=1	--	11.2	--	
Output pin sink current	I_{OL}	V_{OL}=0.1V_{DD}	All IO DS=0	--	7.7	--	mA
			All IO DS=1	--	15.0	--	
Internal pull-up resistor	Rpu	V_{IN}=0V	All IO	--	50	--	kΩ
Input leakage current	I_{IL}	High-impendence input power supply or GND	All IO	--	--	1	uA
Effective pulse width	T_{PW}(IO)	NRST，5.0V		1.2	--	--	ms
	Note: it may not be detected if the min. pulse width of input signal is less than this parameter.						

System monitoring and reset characteristic

Table 4：System monitoring and reset

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C；Full temperature working condition: -40～105°C						
POR reset voltage	V_{PORR}	--	--	1.8	--	V

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Low reset voltage	V_{LVR}	LVRS=00	--	2.3	--	V
		LVRS=01	--	2.7	--	
		LVRS=10	--	3.7	--	
		LVRS=11	--	4.1	--	
LVR release hysteresis voltage	$V_{HYS(LVR)}$		--	40	--	mV
LVD voltage	V_{LVD}	L_{VDS} = 000	--	2.4	--	V
		L_{VDS} = 001	--	2.7	--	
		L_{VDS} = 010	--	3.0	--	
		L_{VDS} = 011	--	3.3	--	
		L_{VDS} = 100	--	3.6	--	
		L_{VDS} = 101	--	3.9	--	
		L_{VDS} = 110	--	4.2	--	
		L_{VDS} = 111	--	4.5	--	
LVD release hysteresis voltage	$V_{HYS(LVD)}$	$V_{DD}\geqslant 3.0$	--	60	--	mV
		$V_{DD}<3.0$	--	35	--	
Power-on reset delay time	T_{PWRT}	--	--	2.5	--	ms
LVR reset delay time	T_{DLVR}	--	--	0.3	--	
STOP wake exit time	T_{STOP}	--	--	30	--	us

Note：The suffix * parameter refers to the simulated value, without testing

Oscillation and clock characteristics

Table 5：Oscillator and clock characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C；Full temperature working condition: -40～105°C						
Internal RCH after calibration	F_{RCH}	2.7~5.5V, -10～65°C	15.68	16	16.32	MHz
		2.2~5.5V, -40～105°C	15.36	16	16.64	
RCH start time	T_{RCHSTR}^{*}	--	--	10	--	us
Internal RCL	F_{RCL}	5V, -40～85°C	7	32	50	KHz
		2.0~5.5V, -40～105°C	5	32	55	
RCL start time	T_{RCLSTR}^{*}	--	--	100	--	us
RCL Stabilization delay counted period	T_{DRCL}	--	64	64	64	Cycles
CRYH start time	T_{CRHHST}	16MHz	--	TBD	--	ms
High frequency Stabilization delay counted period	T_{DCRYH}	Can be set through software	2^7	--	2^{10}	Cyc

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
CRYH frequency range	F_{CRYH}	2.7V<V_{DD}	4	--	24	MHz
HSPLL reference clock frequency range	F_{PLLREF}	2.7～5.5V	1	--	4	MHz
HSPLL output frequency range	F_{PLL}	Input clock source 1、4MHz	1	--	96	MHz
HSPLL lock time	$T_{PLLLOCK}$	2.7~5.5V, -40～85℃	--	100	--	us

Note：The suffix * parameter refers to the simulated value, without testing

RAM minimum retention voltage

Table 0-6：RAM data retention voltage

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C；Full temperature working condition: -40～105°C						
RAM retention voltage	V_{DR}	−40°C < TA < +125°C	0.9	--	--	V

OPA characteristic

Table 0-7：OPA characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C，Input common mode voltage Vcm=V_{DD}/2						
Input offset voltage	Vos	--	-5	0	5	mV
Offset voltage drift	⊿Vos/⊿T*	--	--	0.5	--	uV/°C
Input common mode voltage range	Vcmr*	--	0	--	V_{DD}-1.2	V
Output voltage range	Vor*	--	0.1	--	V_{DD}-0.2	V
Common mode rejection ratio	CMRR*	--	--	100	--	dB
Power supply rejection ratio	PSRR*	--	--	80	--	dB
slew rate	SR*	Load 20pF	--	10	--	V/us
Gain bandwidth product	GBP*	Load 20pF	--	10	--	MHz
Built-in loop amplifier proportional accuracy	Mratio*	--	-2	0	2	%

Note：The suffix * parameter refers to the simulated value, without testing

Analog comparator characteristic

Table 0-8：Analog comparator characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C，Input common mode voltage Vcm=V_{DD}/2						
Input offset voltage	Vos*	--	-3	0	3	mV
Input common mode voltage range	Vcmr	--	0	-	V_{DD}	V
Common mode rejection ratio	CMRR	--	--	0.7	--	mV/V
Hysteresis voltage	Vhys0	--	--	16	--	mV
Response time	Trt	Overdrive voltage ±0.1V	--	500	--	ns

Note：The suffix * parameter refers to the simulated value, without testing

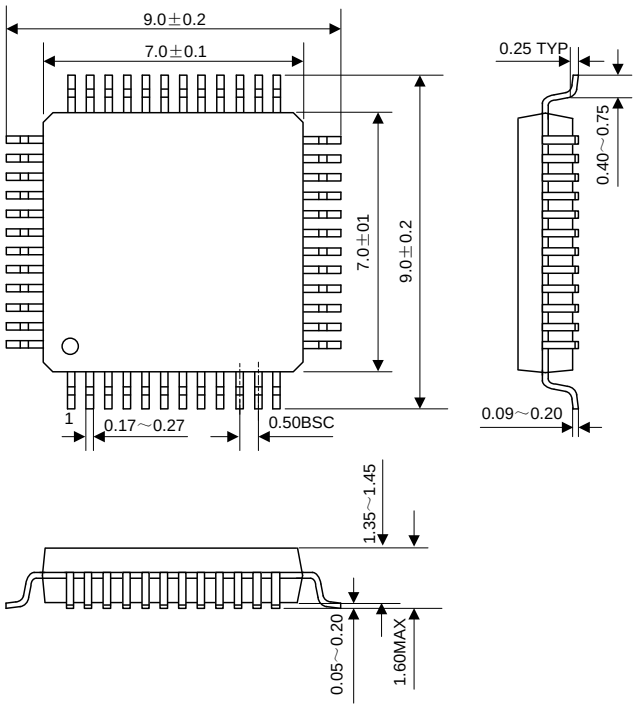
ADC characteristic

Table 0-9：ADC characteristic

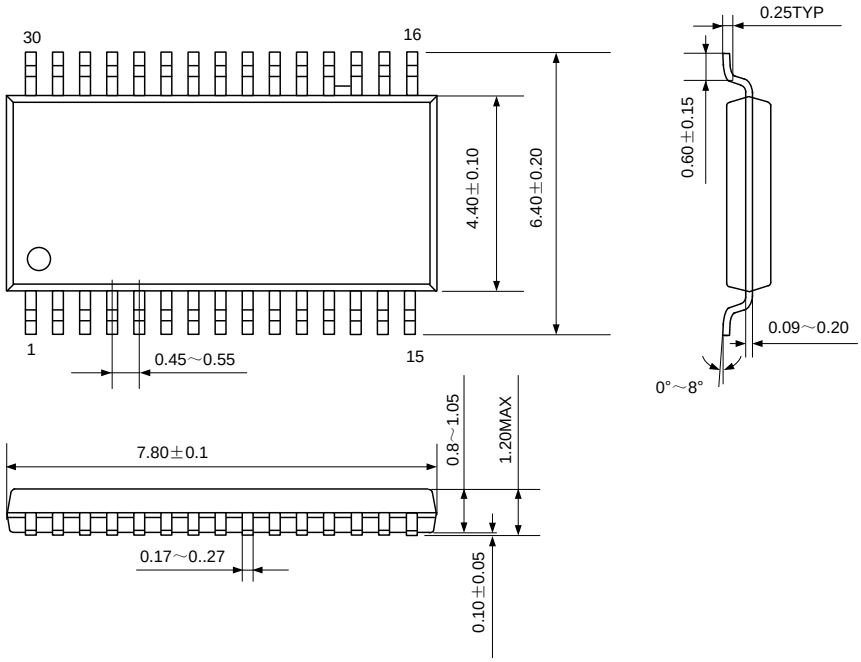
Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
ADC operating voltage range	V_{DDAD}	Fadclk=24MHz	4.5	5	5.5	V
Input analog voltage range	V_{ADIN}	--	0	--	V_{DDAD}	V
Analog channel impedance	R_{ADIN}	--	--	--	1	kΩ
Input source impedance	R_{AS}	Fadclk=24MHz	--	--	1	kΩ
ADC clock frequency	Fadclk	--	--	--	24	MHz
Conversion time	Tconv	--	--	20	-	Cyc
Built-in temperature sensor voltage	Vts			1.01		V
Built-in temperature sensor voltage temperature drift	Vtsslope			3.2		mV/°C
Differential nonlinearity	DNL	--	--	--	±4	LSB
Integral nonlinearity	INL	--	--	--	±4	LSB
Offset error	Ezs	--	--	--	TBD	LSB
Gain error	Efs	--	--	--	TBD	LSB
Total uncorrected error	E_{TUE}	--	--	--	TBD	LSB
Resolution ratio	NR	--	--	12	--	Bit

PACKAGE OUTLINE

LQFP-48-7×7-0.5 Unit：mm

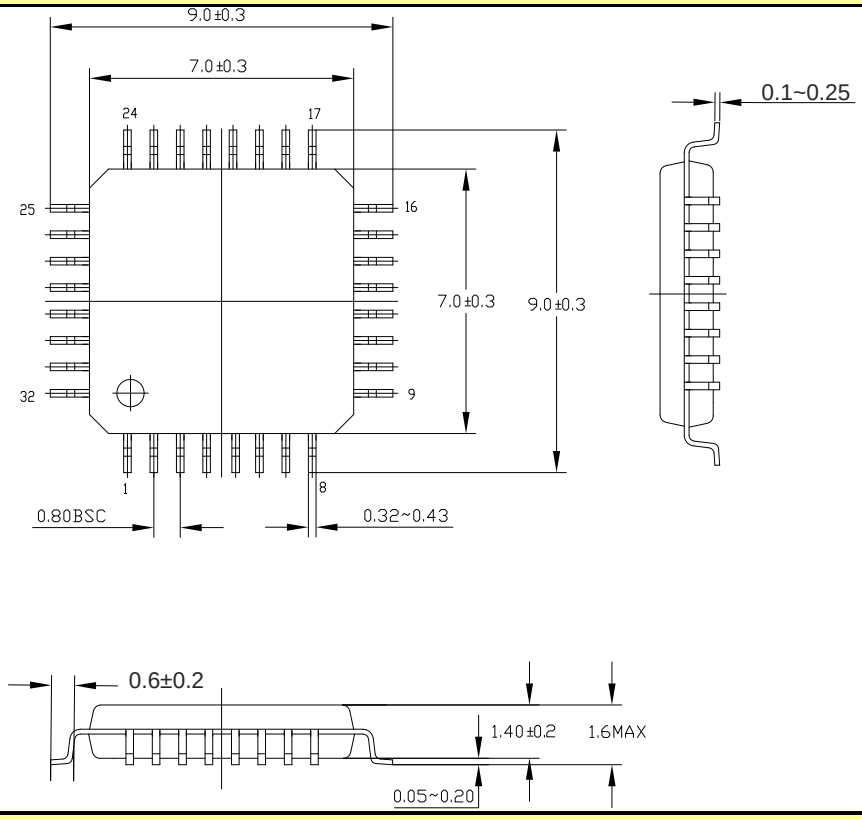


TSSOP-30-225-0.5 Unit：mm

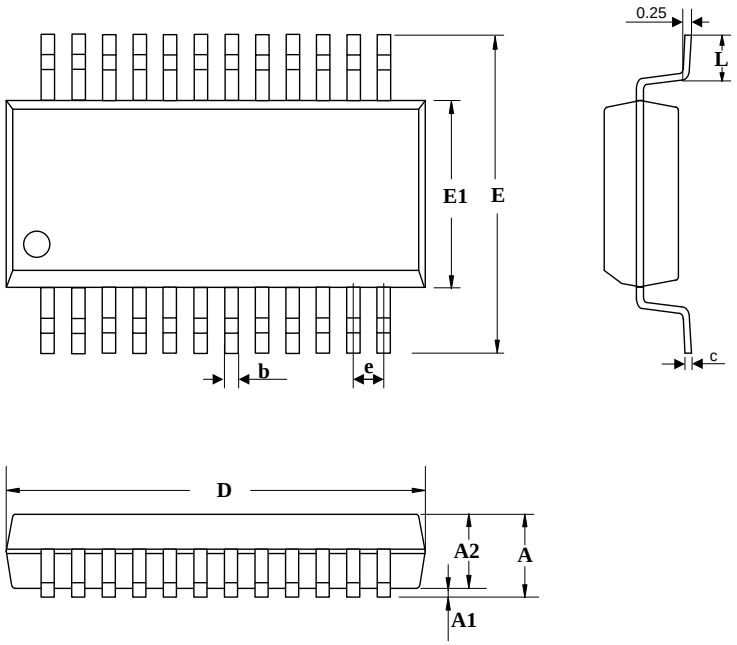


PACKAGE OUTLINE(continued)

LQFP-32-7x7-0.8 Unit：mm



SSOP-24-225-0.635 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.21	—	0.32
c	0.17	—	0.25
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
L	0.40	0.60	0.80

MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed..
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

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Rev： 1.4

Revision history：

1. Modify max system clock

Rev： 1.3

Revision history：

1. Add SSOP-24 package.

Rev： 1.2

Revision history：

1. Add LQFP-32 package.

Rev： 1.1

Revision history：

1. Modify description and block diagram

Rev： 1.0

Revision history：

1. First release