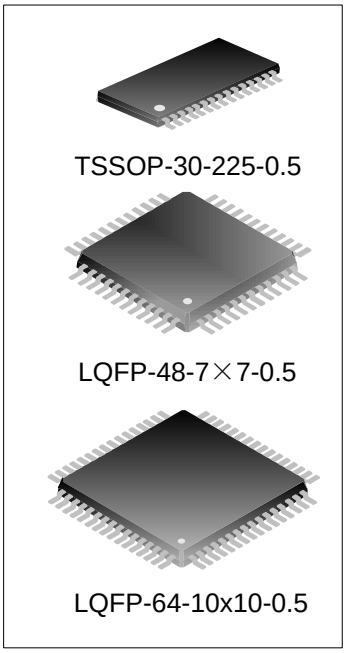
Cortex-M0MCU With enhanced PWM and ADC

DESCRIPTION

SC32F5832（64） is a high performance microcontroller which is designed intended for motor control and digital power application. It uses Cortex-M0 core with maximum operating frequency 72MHz, and ADC sample rate up to 1Msps.a Co-processor unit can meet a variety of multiplication, division, shift and other complex operations.

SC32F5832 supports single power, intigrates high precision high speed and low speed oscillators, and supports a variety of low power mode.The integration of multi-channel enhanced PWM, multi-channelanalog comparator and high speed operational amplifier, make it suitable for a variety of motor and power control application and minimize the system cost..



APPLICATION

- PMSM controller
- BLDC controller
- Universal/private frequency converter
- AC-DC inverter
- Digital control power supply

FEATURES

ARM 32bit Cortex-M0

- Maximum support 72MHz
- Built-in Nested Vectored Interrupt Controller (NVIC)
- Supports single cycle 32bit*32bit multiplication operations
- 6 channel DMA controller, supports Timer0, SPI and UART0/1
- Support MAC、DIV、CRC、Cordic function

Memory

- 32/64Kbyte FLASH，data retention >10 years
- 4/6Kbyte RAM, with parity check

Development support

- Serial Wire Debug(SWD)
- Support MEMORY and peripheral protection

Power supply and Reset

- Operating voltage：2.0V~5.5V
- Built-in 1.5V LDO
- Built-in Power-On-Reset (POR)
- Built-in Low-Voltage-Reset (LVR) with 4 reset points optional :2.3V，2.7V，3.7V，4.3V
- Built-in Low-Voltage-Detect (LVD) with 8 levels optional: 2.4V，2.7V，3.0V，3.3V，3.6V，3.9V，4.2V，

4.5V

Clock system

- 1~24MHz crystal oscillator
- Built-in 32KHz low frequency oscillator(RCL)
- Built-in 16MHz high precision oscillator (RCH)
- PLL supports up to 144MHz

GPIO

- Supports up to 48 I/O ports
- programmable pull-up resistor,open-drain mode, programmable digital input glitch filter, and programmable inputinverter
- Programmable output drive on all GPIO pins
- All GPIO pins can be used as edge and level sensitive interrupt sources

Timer

- One 16-bit Timer0 with up to 4IC/OC/PWM or pulse counter andquadrature (incremental) encoder input
- One 32-bit Timer6 with 2 independent timers,
- 16-bit, motor control PWM timer with dead-time generation and emergency stop
- 2 watchdog timers (Independent and Window)
- SysTick timer :24-bit downcounter

Communication interface

- 2-channel UART
- 1-channel SPI (12Mbit/s)

Analog Modules

- 2-channels rail to rail CMP0 and CMP1(including 3 independent comparator), input hysteresisoptional.
- 4-channels general operation amplifier, both input and output are open
- 1-channel12bit ADC, 16 channel inputs, maximum conversion rate is 1Msps

Operation mode

- Normal operating mode
- IDLE mode
- STOP mode

Operation Temperature

- -40~105℃

Package Type

- TSSOP-30
- LQFP-48，LQFP-64

ORDERING INFORMATION

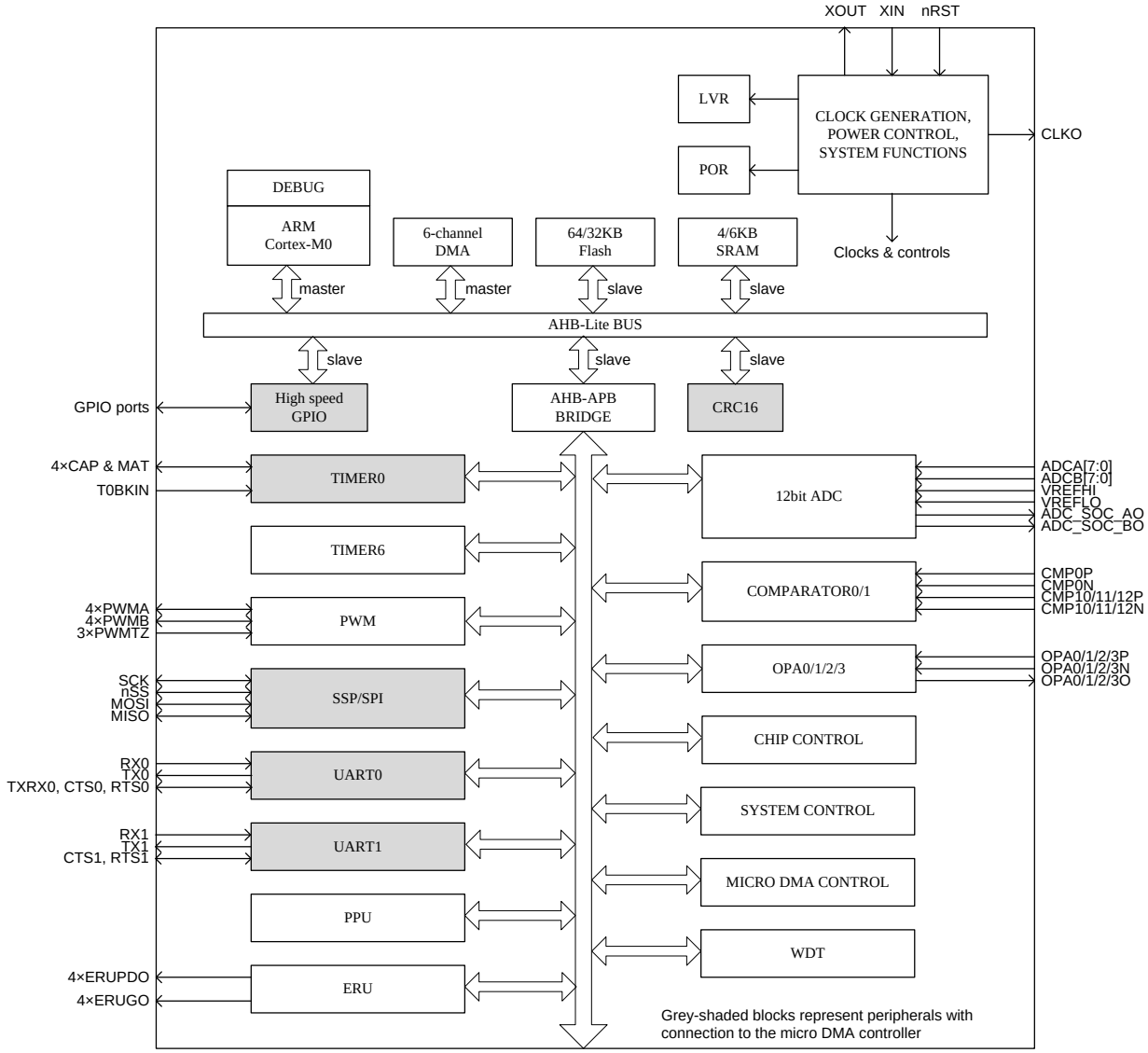
ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SC32F5832LL1G	LQFP-48-7x7-0.5	5832LL1G	Halogen free	Tray
SC32F5864LL1G	LQFP-48-7x7-0.5	5864LL1G	Halogen free	Tray
SC32F5832LB1G	LQFP-64-10x10-0.5	5832LB1G	Halogen free	Tray
SC32F5864LB1G	LQFP-64-10x10-0.5	5864LB1G	Halogen free	Tray
SC32F5832JV1G	TSSOP-30-225-0.5	5832JV1G	Halogen free	Tube
SC32F5832JV1GTR				Reel
SC32F5864JV1G	TSSOP-30-225-0.5	5864JV1G	Halogen free	Tube
SC32F5864JV1GTR				Reel

RESOURCE INFORMATION

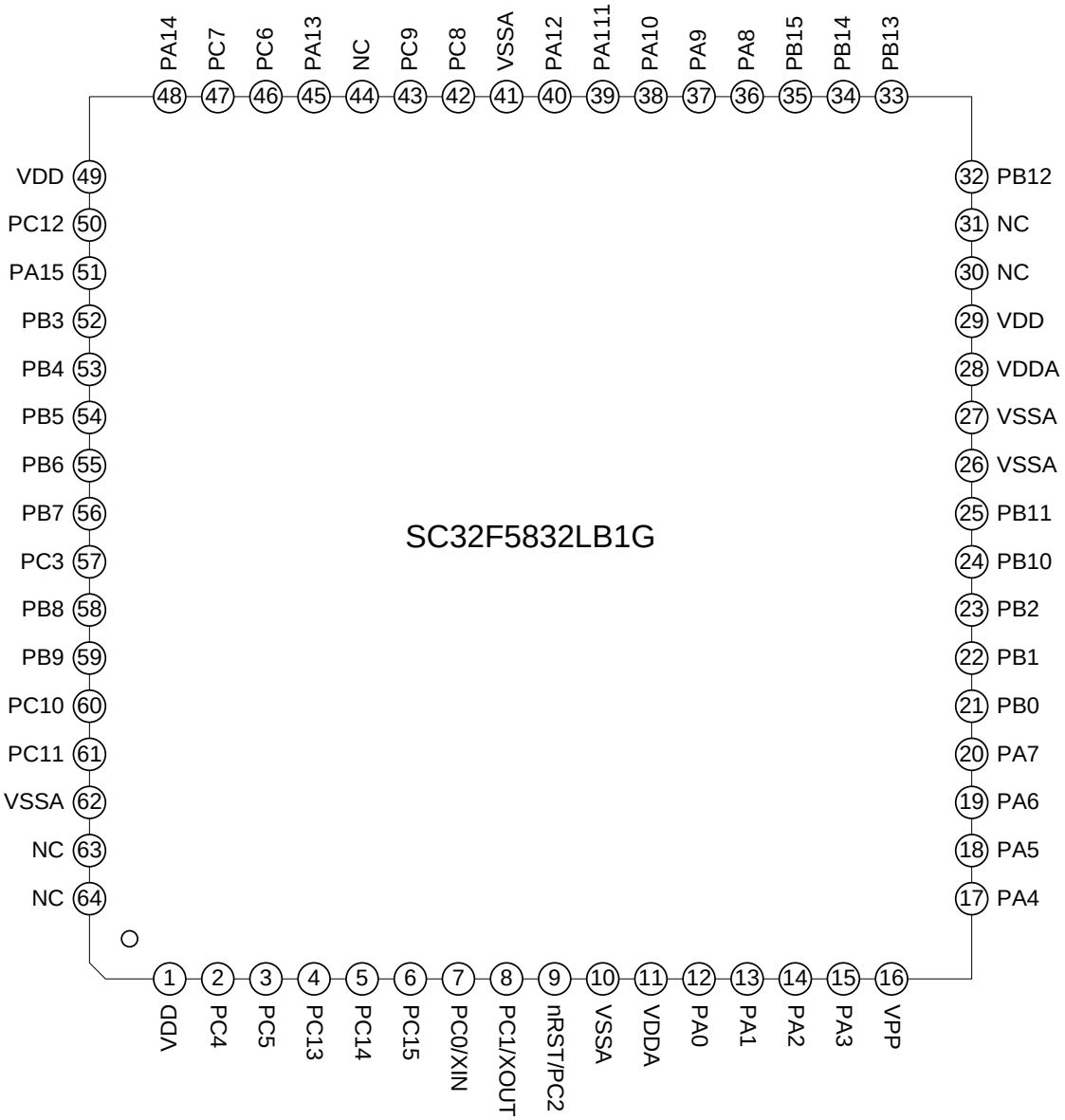
Feature	TSSOP-30	LQFP-48	LQFP-64
FLASH	32/64K Byte		
RAM	4/6K Byte		
I/O	26	42	48
T0	1	1	1
T6	2	2	2
PWM	4*2	4*2	4*2
ACMP	2（1+3）	2（1+3）	2（1+3）
OPA	4	4	4
ADC	10ch+4ch（OPAxOUT）	16ch	16ch
UART	2	2	2
SPI	1	1	1

BLOCK DIAGRAM

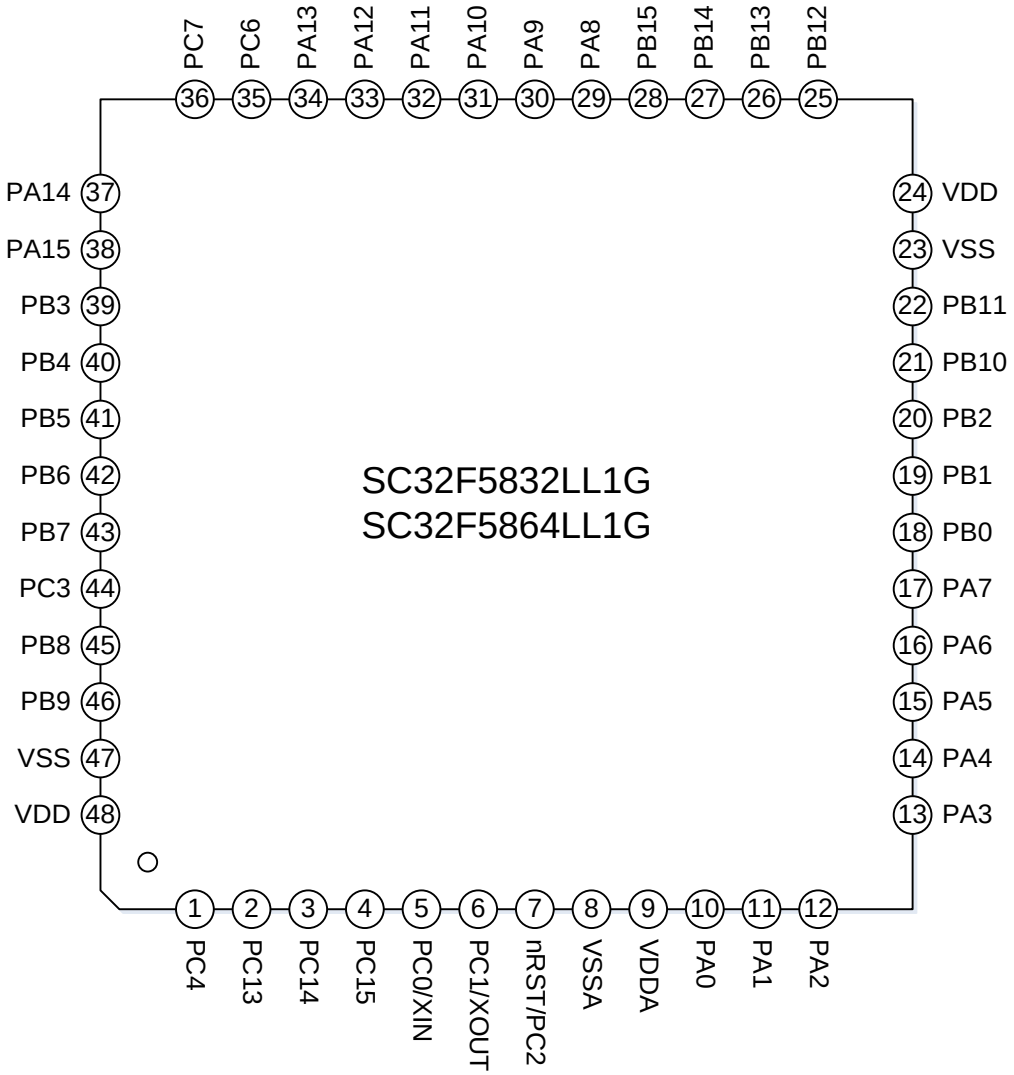


PIN CONFIGURATION

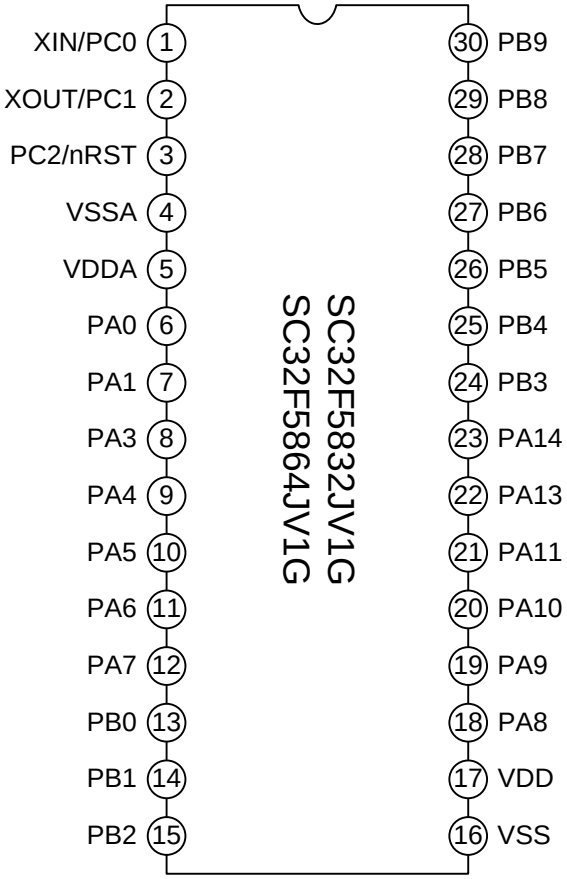
LQFP-64：SC32F5832/64LB1G



LQFP-48：SC32F5832/64LL1G



TSSOP-30：SC32F5832/64JV1G



PIN DESCRIPTION

PIN MULTIPLEX

Pin No.			Power	Digital								Analog		
-LB	-LL	-JV		ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT0	ALT1	ALT2
2	1	--	--	PC4	PWM 2B	PWM 1B	--	--	T0ETR	ERU1 PDO	ERU1 GO	--	--	--
3	--	--	--	PC5	PWM 4B	PWM TZ1	--	--	T0BKIN	EXTS YNI	--	--	--	--
4	2	--	--	PC13	PWM 0A	PWM 1A	--	UART 0RX	T0CH 3	UART 1_RX	--	ADC B7	--	--
5	3	--	--	PC14	PWM 1A	PWM 2B	--	UART 0TX	T0CH 3N	UART 1TX	--	ADC A7	--	--
6	4	--	--	PC15	PWM	PWM	--	--	T0CH	--	--	ADC	--	--

					2A	2A			4			A6		
7	5	1	XIN	PC0	T0CH 3	--	--	--	PWM TZ1	ERU0 PDO	ERU0 GO	--	CP12 P	--
8	6	2	XOUT	PC1	--	--	--	--	XCLK OUT	EXTS YNO	--	--	CP12 N	--
9	7	3	NRST	PC2	--	--	--	--	--	--	--	--	--	--
10	8	4	VSSA	--	--	--	--	--	--	--	--	--	--	--
11	9	5	VDDA	--	--	--	--	--	--	--	--	--	--	--
12	10	6	--	PA0	UART 0CTS	UART 1CTS	--	--	--	--	--	ADC A5	OPA0 P	CP0P
13	11	7	--	PA1	UART 0RTS	UART 1RTS	--	--	--	--	--	ADC A4	OPA0 N	CP0N
14	12		--	PA2	UART 0TX	UART 1TX	UART 0TXR X	--	XCLK INA	--	--	ADC A3	OPA0 O	--
15	13	8	--	PA3	UART 0RX	UART 1RX	T0CH 2	--	--	--	--	ADC A2	OPA3 P	--
16			VDD	--	--	--	--	--	--	--	--	--	--	--
17	14	9	--	PA4	--	--	--	--	SPI0 NSS	--	--	ADC A1	OPA3 N	--
18	15	10	--	PA5	--	--	--	--	SPI0 SCK	--	--	ADC A0	OPA3 O	VREF HI
19	16	11	--	PA6	PWM TZ0	PWM TZ2	T0CH 1	--	SPI0 MISO	T0BK IN	--	ADC B0	OPA2 O	VREF LO
20	17	12	--	PA7	PWM 0B	--	T0CH 2	--	SPI0 MOSI	T0CH 1N	--	ADC B1	OPA2 N	--
21	18	13	--	PB0	PWM 0A	--	T0CH 3	--	--	T0CH 2N	--	ADC B2	OPA2 P	--
22	19	14	--	PB1	PWM 1B	--	T0CH 4	--	--	T0CH 3N	--	ADC B3	ELVI	--
23	20	15	--	PB2	--	--	--	--	XCLK OUT	--	--	ADC B4	--	--
24	21		--	PB10	--	--	--	--	--	ERU2 PDO	ERU2 GO	ADC B5	--	--
25	22	--	--	PB11	--	--	--	--	--	--	--	ADC	--	--

												B6		
26	23	16	VSS	--	--	--	--	--	--	--	--	--	--	--
27			VSSA	--	--	--	--	--	--	--	--	--	--	--
28			VDDA	--	--	--	--	--	--	--	--	--	--	--
29	24	17	VDD	--	--	--	--	--	--	--	--	--	--	--
30	--	--	NC	--	--	--	--	--	--	--	--	--	--	--
31	--	--	NC	--	--	--	--	--	--	--	--	--	--	--
32	25	--	--	PB12	PWM TZ0		SPI0 NSS	T0BK IN	--	--	--	--	--	--
33	26	--	--	PB13	PWM 0B	PWM 0B	SPI0 SCK	T0CH 1N	--	--	--	--	--	--
34	27	--	--	PB14	PWM 1B	PWM 0A	SPI0 MISO	T0CH 2N	--	T0CH 1	--	--	--	--
35	28	--	--	PB15	PWM 2B	PWM 1B	SPI0 MOSI	T0CH 3N	--	T0CH 1N	T0CH 2	--	--	--
36	29	18	--	PA8	PWM 0A	PWM 1A	--	T0CH 1	--	--	--	--	--	--
37	30	19	--	PA9	PWM 1A	PWM 2B	UART 0TX	T0CH 2	--	--	T0BKI N	--	--	--
38	31	20	--	PA10	PWM 2A	PWM 2A	UART 0RX	T0CH 3	--	--	--	--	--	--
39	32	21	--	PA11	PWM 4B	PWM TZ0	UART 0CTS	T0CH 4	SPI0 NSS	T0CH 1	T0CH 1	--	--	--
40	33	--	--	PA12	PWM 4A	--	UART 0RTS	T0ET R	SPI0 SCK	UART 0RX	T0CH 1N	--	--	--
41	--	--	VSS	--	--	--	--	--	--	--	--	--	--	--
42	--	--	--	PC8	--	--	UART 0RX	UART 0TXR X	SPI0 MISO	UART 0TX	SPI0I O	--	--	--
43	--	--	--	PC9	--	--	UART 0TX	--	SPI0 MOSI	--	--	--	--	--
44	--	--	NC	--	--	--	--	--	--	--	--	--	--	--
45	34	22	--	PA13	SPDA T	IR_O UT	UART 0RX	--	--	--	--	--	--	--
46	35	--	--	PC6	--	--	UART 0TX	UART 0TXR X	EXTS YNO	ERU3 PDO	ERU3 GO	--	--	--
47	36	--	--	PC7	--	--	--	--	--	--	--	--	--	--
48	37	23	--	PA14	SPCL K	--	UART 0TX	UART 1TX	--	--	--	--	--	--

49	--	--	VDD	--	--	--	--	--	--	--	--	--	--	--
50	--	--		PC12	--	--	--	--	--	--	--	--	--	--
51	38	--	--	PA15	--	SPI0 NSS	UART 0RX	UART 1RX	EXTS YNI	ERU1 PDO	ERU1 GO	--	--	--
52	39	24	--	PB3	PWM TZ1	SPI0 SCK	--	XCLK OUT	--	--	--	--	OPA1 P	--
53	40	25	--	PB4	T0CH 1	SPI0 MISO	--	--	--	--	--	--	OPA1 N	--
54	41	26	--	PB5	T0CH 2	SPI0 MOSI	--	--	--	--	--	--	OPA1 O	--
55	42	27	--	PB6	T0CH 3	--	UART 1TX	--	T0CH 1	--	--	CP10 P	--	--
56	43	28	--	PB7	T0CH 4	--	UART 1RX	--	T0CH 1N	--	--	CP10 N	--	--
57	44	--	--	PC3	--	--	XCLK INB	EXTS YNO	--	ERU0 PDO	ERU0 GO	--	--	--
58	45	29	--	PB8	--	--	T0CH 4	EXTS YNI	T0CH 2	--	--	CP11 P	--	--
59	46	30	--	PB9	--	PWM TZ2	IR_O UT	--	T0CH 2N	--	--	CP11 N	--	--
60	--	--	--	PC10	PWM 0B	PWM 0B	--	--	T0CH 3	--	--	--	--	--
61	--	--	--	PC11	PWM 1B	PWM 0A	--	--	T0CH 4	T0CH 3N	--	--	--	--
62	47	--	VSS	--	--	--	--	--	--	--	--	--	--	--
63	--	--	--	NC	--	--	--	--	--	--	--	--	--	--
64	--	--	--	NC	--	--	--	--	--	--	--	--	--	--
1	48	--	VDD		--	--	--	--	--	--	--	--	--	--

PIN DESCRIPTION

I/O	Pin Type	Function Description
PORT		
PA.0-PA.15	I/O	16-bit bidirectional I/O ports, bit operation available
PB.0-PB.15	I/O	16-bit bidirectional I/O ports, bit operation available
PC.0-PC.15	I/O	16-bit bidirectional I/O ports, bit operation available

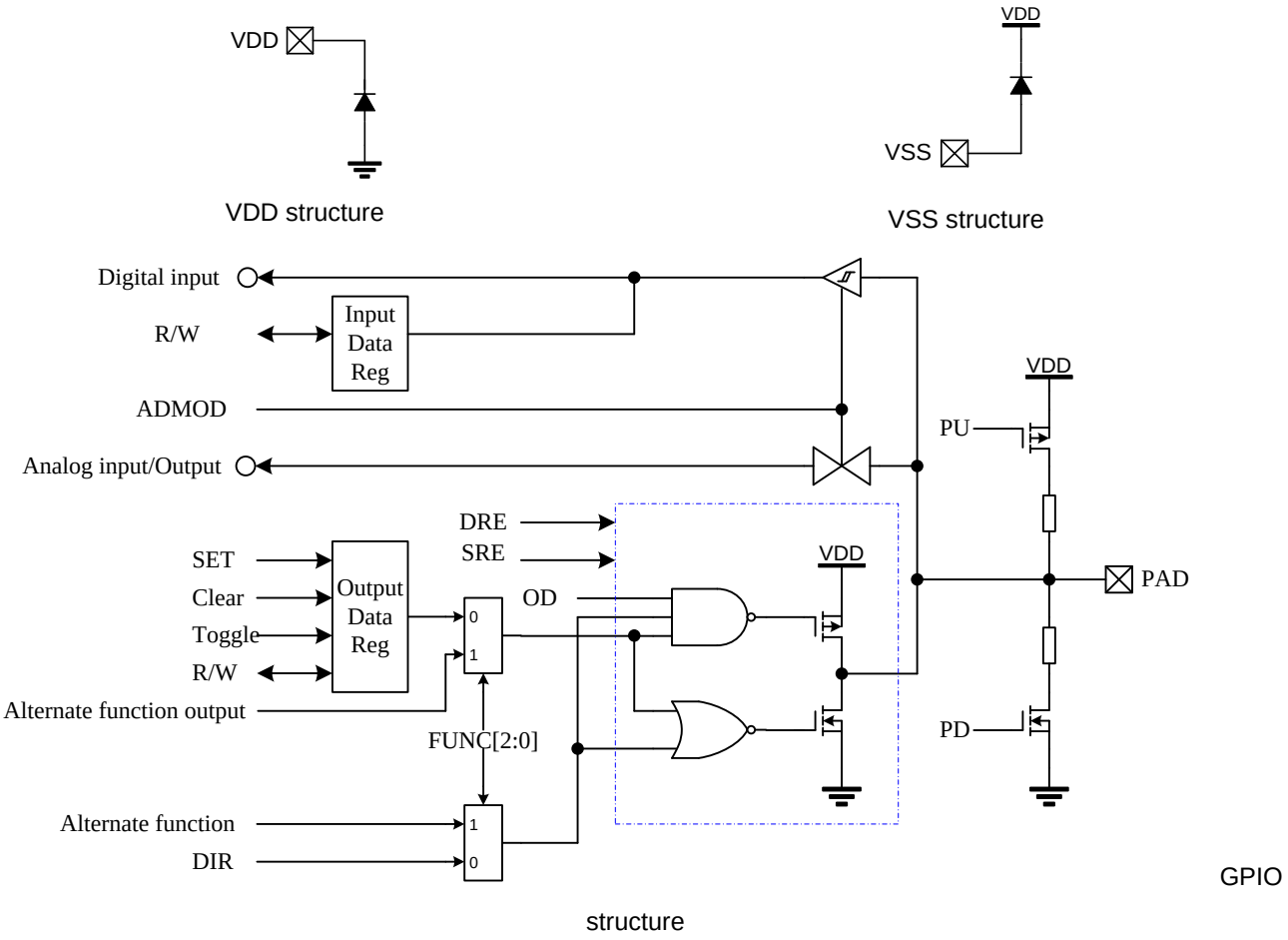
I/O	Pin Type	Function Description
系统		
NRST	I	External reset input, low voltage active
XIN	I	External oscillator input
XOUT	O	External oscillator output
XCLKOUT	O	Internal clock output
EXTSYNO	O	PWMsynchronous pulse output
EXTSYNI	O	PWMsynchronous pulse output
ELVI	I	External low voltage detect input
TIMER		
T0CH1~ T0CH4	I/O	Timer0 capture input and output (positive end)
T0CH1N~ T0CH4N	I/O	Timer0 capture input and output (negative end)
T0BKIN	I	Timer0 brake input
IR_OUT	O	Carrier output
PWM		
PWM0A	O	PWM0 Achannel output
PWM0B	O	PWM0 Bchannel output
PWM1A	O	PWM1 Achannel output
PWM1B	O	PWM1 Bchannel output
PWM2A	O	PWM2Achannel output
PWM2B	O	PWM2 Bchannel output
PWM4A	O	PWM4Achannel output
PWM4B	O	PWM4 Bchannel output
PWMTZ0~ PWMTZ2	I	PWM brake input(emergency brake)
COMMUNICATION INTERFACE		
SPI0NSS	I/O	SPIenable pin
SPI0SCK	I/O	SPIclock input
SPI0MISO	I/O	SPImaster input/slave output
SPI0MOSI	I/O	SPI master output/slave input
SPI0IO	I/O	3 wire mode SPI data line
UART0CTS	I	UART0 send clear
UART0RTS	O	UART0 send request
UART0RXTX	I/O	UART0half-duplex UART data line
UART0TX	O	UART0 data output
UART0RX	I	UART0 data input
UART1TX	O	UART1 data output
UART1RX	I	UART1 data input
Analog comparator		

I/O	Pin Type	Function Description
CP0P	I	Comparator 0 positive input
CP0N	I	Comparator 0 negative input
CP10P	I	Comparator 10 positive input
CP10N	I	Comparator 10 negative input
CP11P	I	Comparator 11 positive input
CP11N	I	Comparator 11 negative input
CP12P	I	Comparator 12 positive input
CP12N	I	Comparator 12 negative input
Operational amplifier		
OPA0P	I	OPA0 positive input
OPA0N	I	OPA0 negative input
OPA1P	I	OPA1 positive input
OPA1N	I	OPA 1 negative input
OPA2P	I	OPA 2 positive input
OPA2N	I	OPA 2 negative input
OPA3P	I	OPA 3 positive input
OPA3N	I	OPA 3 negative input
OPA0O	O	OPA 0 output
OPA1O	O	OPA 1 output
OPA2O	O	OPA 2 output
OPA3O	O	OPA 3 output
ADC		
ADCA0~ ADCA7	I	ADC A channel input
ADCB0~ ADCB7	I	ADC B channel input
VREFHI	I	ADC reference voltage high
VREFLO	I	ADC reference voltage low
ERU		
ERU0PDO	O	ERU0 voltage signal output
ERU0GO	O	ERU0 gate control signal output
ERU1PDO	O	ERU1 voltage signal output
ERU1GO	O	ERU1 gate control signal output
ERU2PDO	O	ERU2 voltage signal output
ERU2GO	O	ERU2 gate control signal output
EERU3PDO	O	ERU3 voltage signal output
ERU3GO	O	ERU3 gate control signal output
Power and Ground		
VDD	P	Power

I/O	Pin Type	Function Description
VSS	P	Ground
VDDA	P	Analog power
VSSA	P	Analog ground
VPP	P	High voltage program

Notes： In Pin Type column: “P” denotes Power pins, “I/O” denotes normal input/output pins, “I”denotes input pins, “O” denotes output pins;

PIN STRUCTURE



ABSOLUTEMAXIMUMRATINGS

Device may cause permanent damage if operating condition exceeds the “absolute maximum ratings”. We don’t recommend customer to operate device out of the range. If device works in absolute maximum condition for long time, reliability will be affected.

Power supply characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	-0.3	-	6.0	V
Core voltage	V_{CORE}	-	-0.3	1.5	2.0	

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	-	-0.3	-	V_{DD}+0.5	

Note： All voltage are referenced by V_{SS}

Current characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Total current flowing into VDD	I_{VDD}	-	-	-	100	mA
Total current flowing out of Vss	I_{VSS}	-	-	-	100	
Pin injection current	I_{INJ}	$V_{IN}>V_{DD}$ 或 $V_{IN}<V_{SS}$	-4	-	4	
		$V_O>V_{DD}$ 或 $V_O<V_{SS}$	-4	-	4	
Total injection current	ΣI_{INJ}	-	-20	-	20	

Thermal characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Ambient temperature	T_A	-	-40	-	105	°C
Storage temperature	T_{STG}	-	-55	-	125	
Junction temperature	T_J	-	-	-	150	
Thermal resistance	θ_{JA}	TSSOP-30-225-0.5	-	68	-	°C/W
		LQFP-48-7*7-0.5	-	78	-	
		LQFP-64-10*10-0.5	-	65	-	
Total power consumption	P_D	-	-	-	500	mW

Note：Thermal resistance is related with package form, PCB board design, ambient wind speed and power consumption.

Recommend working condition

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	2.0	5.0	5.5	V
CPU frequency	F_{CPU}	V_{DD}=2.7~5.5V,MClk=PLL/2=72MHz	-	72	-	MHz

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the typical values are the test results at VDD=5.0V, T_A =25°C

Unless otherwise specified, the max. and min. values are the test results at ambient temperature(T_A=25°C)

Current characteristic

Obey the following conditions when measuring current characteristic:

* All IO are set output low voltage, no load.
* Unless otherwise specified, all peripherals are closed.

Table 1：Power supply characteristic

Symbol	Characteristic	Test condition			Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	MClk = RCH=16MHz			2.0	--	5.5	V
		MClk = PLL/3=48MHz			2.7	--	5.5	
		MClk =PLL/2=72MHz			2.7	--	5.5	
		M_{CLK} =PLL(CRY16M)/2=72MHz			2.7	--	5.5	
I_{DD}	Operating current, considering the temperature	RCH provides system clock	MClk=16MHz	V_{DD}=5.0	--	2.2	--	mA
		CRYH provides system clock, min. gain	MClk=16MHz	V_{DD}=5.0	--	3.5	--	
		RCH+PLL	MClk=48MHz	V_{DD}=5.0	--	8	--	
			MClk=72MHz	V_{DD}=5.0	--	10	--	
		RCL provides system clock	MClk=F_{RCL}	V_{DD}=5.0	--	170	--	uA
	Note: when one clock is working, others are off, except HSPLL, because it depends on RCH or CRYH input.							
I_{IDLE}	IDLE current	RCH provides system clock	MClk=16MHz	V_{DD}=5.0	--	1.0	--	mA
		CRYH provides system clock, min. gain	MClk=16MHz	V_{DD}=5.0	--	2.2	--	
		RCH+PLL	MClk=48MHz	V_{DD}=5.0	--	4.8	--	
			MClk=72MHz	V_{DD}=5.0	--	5.6	--	
		RCL provides system clock	MClk=F_{RCL}	V_{DD}=5.0	--	0.15	--	
I_{STOP}	STOP current	LVR ON	V_{DD}=5.0		--	60	--	uA
		LVR OFF	V_{DD}=5.0		--	45	--	

Note：Typical values are results of sampling test, not tested in mass production.

Table 2：Module operating current

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
RCLoperating current	I_{RCL}^*		--	1	--	uA
RCH operating current	I_{RCH}^*		--	190	--	uA

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
CRYH(1M)module operating current	I_{CRYH}*	Min. gain	--	0.2	--	mA
CRYH(16M)module operating current	I_{CRYH}*	Min. gain	--	1.2	--	mA
LVDoperating current	I_{LVD}*		--	15	--	uA
LVR operating current	I_{LVR}*		--	15	--	uA
HSPLL module operating current	I_{PLL1}*	144MHz	--	1	--	mA
ADCoperating current	I_{ADC}*	AD continuous working @MClk=24MHz	--	4	--	mA
OPA0/1/2/3operating current	I_{OPA}*	On, internal 1X follow @each OPA	--	1.5	--	mA
CMP0operating current	I_{CMP0}*		--	15	--	uA
CMP1 operating current	I_{CMP1}*	ON @each CMP	--	15	--	uA

Note： The suffix * parameter refers to the simulated value, without testing

IO characteristic

Table 3：IOcharacteristic

Characteristic	Symbol	Test condition		Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C；Full temperature working condition: -40～105°C							
High input voltage	V_{IH}	All IO		0.7V_{DD}	--	V_{DD}	V
Low input voltage	V_{IL}	All IO		0	--	0.3V_{DD}	V
Driving condition when V_{DD}=5.0V							
Output pin source current	I_{OH}	V_{OH}=0.9V_{DD}	All IO DS=0	--	4	--	mA
			AllIO DS=1	--	9	--	
Output pin sink current	I_{OL}	V_{OL}=0.1V_{DD}	AllIO DS=0	--	7	--	mA
			AllIO DS=1	--	11	--	
Internal pull-up resistor	Rpu	V_{IN}=0V	All IO	--	50	--	kΩ
Input leakage current	I_{IL}	High-impendence input power supply or GND	All IO	--	--	1	uA
Effective pulse width	T_{PW}(IO)	NRST，5.0V		1.2	--	--	ms
	Note: it may not be detected if the min. pulse width of input signal is less than this parameter.						

System monitoring and reset characteristic

Table 4：System monitoring and reset

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C；Full temperature working condition: -40～105°C						
POR release voltage	V_{PORR}	--	--	1.8	--	V
VDD rising speed	S_{VDD}	make sure to generate internal POR signal	0.05	-	100	V/ms
LDO output voltage	V_{MVR}	--	--	1.5	--	V
LVR voltage	V_{LVR}	LVRS=00	--	2.3	--	V
		LVRS=01	--	2.7	--	
		LVRS=10	--	3.7	--	
		LVRS=11	--	4.1	--	
LVR release hysteresis voltage	$V_{HYS(LVR)}$		--	40	--	mV
LVD voltage	V_{LVD}	L_{VDS} = 000	--	2.4	--	V
		L_{VDS} = 001	--	2.7	--	
		L_{VDS} = 010	--	3.0	--	
		L_{VDS} = 011	--	3.3	--	
		L_{VDS} = 100	--	3.6	--	
		L_{VDS} = 101	--	3.9	--	
		L_{VDS} = 110	--	4.2	--	
		L_{VDS} = 111	--	4.5	--	
LVD release hysteresis voltage	$V_{HYS(LVD)}$	V_{DD}≥3.0	--	60	--	mV
		V_{DD}<3.0	--	35	--	
POR delay time	T_{PWRT}	--	--	2.5	--	ms
LVR delay time	T_{DLVR}	--	--	0.3	--	
STOP wake exit time	T_{STOP}	--	--	30	--	us

Note：The suffix * parameter refers to the simulated value, without testing

Oscillation and clock characteristics

Table 5：Oscillator and clock characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C；Full temperature working condition: -40～105°C						
Internal RCH frequency after calibration	F_{RCH}	2.7~5.5V, -10～65°C	15.68	16	16.32	MHz
		2.2~5.5V, -40～105°C	15.36	16	16.64	
RCH start time	T_{RCHSTR}^{*}	--	--	10	--	us
Internal RCLfrequency	F_{RCL}	5V, -40～85°C	7	32	50	KHz
		2.0~5.5V, -40～105°C	4	32	55	
RCL start time	T_{RCLSTR}^{*}	--	--	100	--	us
RCL stabilization delay counting cycle	T_{DRCL}	--	64	64	64	Cycles
CRYH start time	T_{CRHHST}	16MHz	--	10	--	ms

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
High frequency Stabilization delay counting cycle	T_{DCRYH}	Can be set through software	2^7	--	2^{10}	Cyc
CRYH frequency range	F_{CRYH}	2.7V<V_{DD}	4	--	24	MHz
HSPLL reference clock frequency range	F_{PLLREF}	2.7～5.5V	1	--	4	MHz
HSPLL output frequency range	F_{PLL}	Input clock source1、4MHz	1	--	144	MHz
HSPLL lock time	$T_{PLLLOCK}$	2.7~5.5V, -40～85℃	--	100	--	us

RAM minimum retention voltage

Table 0-6：RAM data retention voltage

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C；Full temperature working condition: -40～105°C						
RAM retention voltage	V_{DR}	−40°C < TA < +125°C	0.9	--	--	V

OPA characteristic

Table 0-7：OPA characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C，Input common mode voltage Vcm=V_{DD}/2						
Input offset voltage	Vos	--	-5	0	5	mV
Offset voltage drift	⊿Vos/⊿T*	--	--	0.5	--	uV/℃
Input common mode voltage range	Vcmr*	--	0	--	V_{DD}-1.2	V
Output voltage range	Vor*	--	0.1	--	V_{DD}-0.2	V
Common mode rejection ratio	CMRR*	--	--	100	--	dB
Power supply rejection ratio	PSRR*	--	--	80	--	dB
Slew rate	SR*	Load 20pF	--	10	--	V/us
Gain bandwidth product	GBP*	Load 20pF	--	10	--	MHz
Built-in loop amplifier proportional accuracy	Mratio*	--	-2	0	2	%

Note：The suffix * parameter refers to the simulated value, without testing

Analog comparator characteristic

Table 0-8：Analog comparator characteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=5.0V，temperature=25°C，Input common mode voltage Vcm=V_{DD}/2						
Input offset voltage	Vos*	--	-3	0	3	mV

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input common mode voltage range	Vcmr	--	0	-	V_{DD}	V
Common mode rejection ratio	CMRR	--	--	0.7	--	mV/V
COMP0 hysteresis voltage	Vhys0	--	--	16	--	mV
COMP1 hysteresis voltage	Vhys11	--	--	8	--	mV
	Vhys12	--	--	16	--	mV
	Vhys13	--	--	32	--	mV
	Vhys14	--	--	110	--	mV
Response time	Trt	Overdrive 电压±0.1V	--	500	--	ns

Note：The suffix * parameter refers to the simulated value, without testing

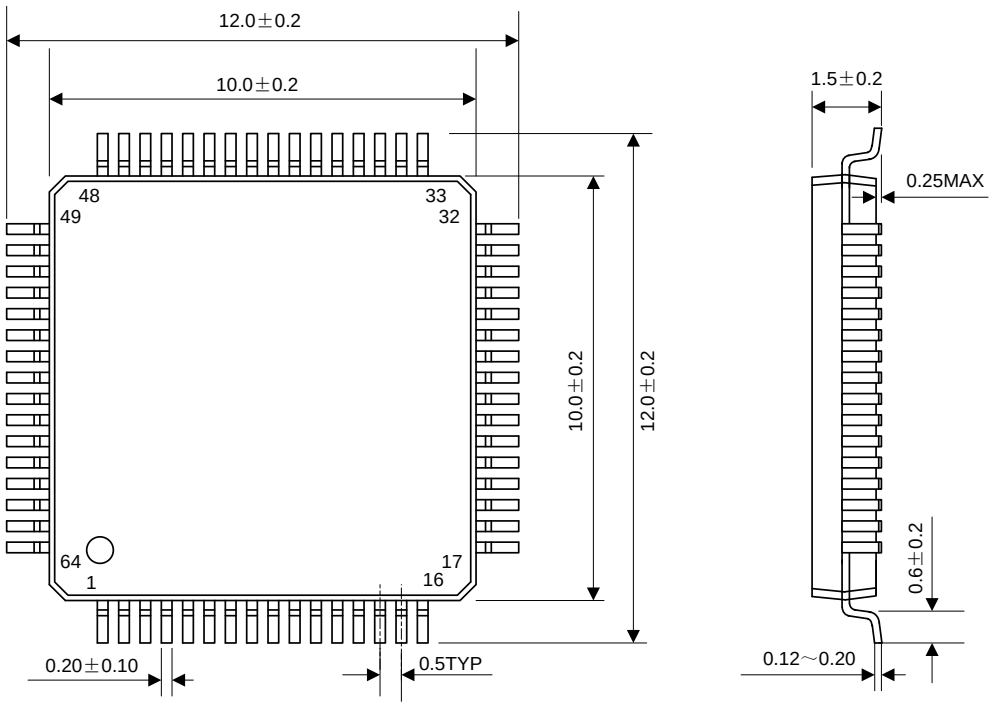
ADC characteristic

Table 0-9：ADCcharacteristic

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
ADC operating voltage range	V_{DDAD}	Fadclk=24MHz	4.5	5	5.5	V
Input analog voltage range	V_{ADIN}	--	0	--	V_{DDAD}	V
Analog channel impedance	R_{ADIN}	--	--	--	1	kΩ
Input source impedance	R_{AS}	Fadclk=24MHz	--	--	1	kΩ
ADC clock frequency	Fadclk	--	--	--	24	MHz
Conversion time	Tconv	--	--	20	-	Cyc
Built-in temperature sensor voltage	Vts			1.01		V
Built-in temperature sensor voltage temperature drift	Vtsslope			3.2		mV/℃
Differential nonlinearity	DNL	--	--	--	±4	LSB
Integral nonlinearity	INL	--	--	--	±4	LSB
Offset error	Ezs	--	--	--	TBD	LSB
Gain error	Efs	--	--	--	TBD	LSB
Total uncorrected error	E_{TUE}	--	--	--	TBD	LSB
Resolution ratio	NR	--	--	12	--	Bit

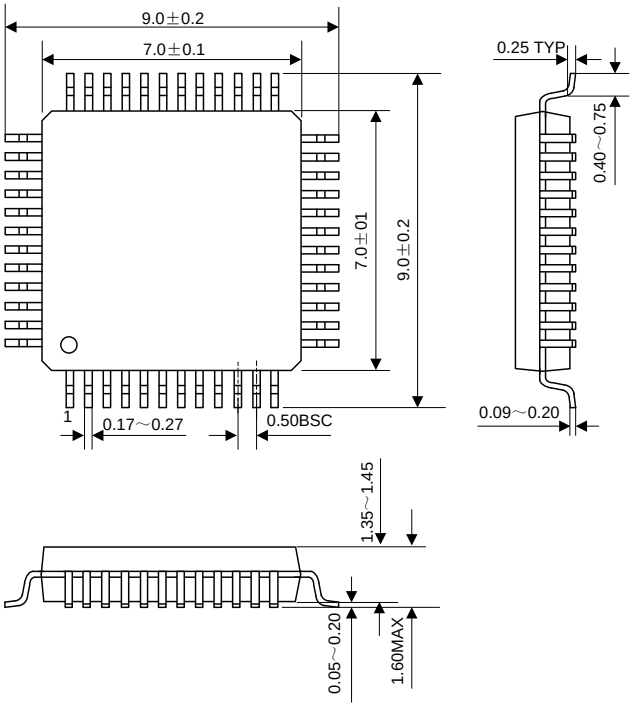
PACKAGE OUTLINE

LQFP-64-10×10-0.5 **Unit：mm**

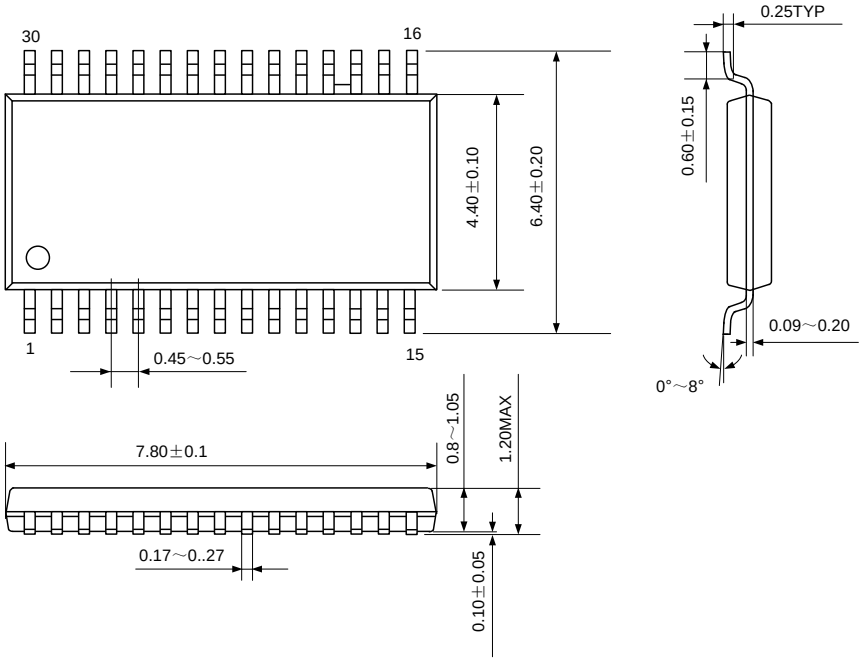


PACKAGE OUTLINE(2)

LQFP-48-7×7-0.5 Unit：mm



TSSOP-30-225-0.5 Unit：mm



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation

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Rev.： 1.1

Revision history：

1. Modify description and block diagram
2. Modify pin configuration and pin description of LQFP-64

Rev.： 1.0

Revision history：

1. First release