SC3503 Fast Turn-Off Synchronous Rectifier Controller

1 Description

SC3503 is a smart secondary-side driver IC designed to drive N-Channel power MOSFET used as synchronous rectifiers in isolated flyback converters. The MOSFET can replace Schottky diode so the system can achieve higher efficiency and superior heat dissipation performance.

The SR MOSFET is turned on when VDS falls below turn-on threshold, and turned off when VDS exceeds turn-off threshold. The SR conduction voltage drop is continuously monitored to minimize the conduction loss. The extremely fast turn-off comparator and driving circuitry ensures the safety of the SR MOSFET, even in current continuous mode (CCM) condition.

The IC can work well in wide output voltage range, even in short circuit conditions. The patented turn on detection circuity prevents SR turn on when Vds rings severely. The wide VDD range and gate driver technology make the controller ideal for wide output voltage range applications, such as adapters, chargers, USB Power Delivery (USB-PD), etc.

This chip supports both high side rectification and low side rectification.

2 Features

- High output voltage up to 22V
- Wide output range, even down to 0V.
- No need of auxiliary winding for power supply.
- Patented programmable turn on detection circuitry prevents MOSFET from mistake turn-on.
- Compliant with multiple types of MOSFETs
- High efficiency can meet CoC V5 and DoE VI.
- 10nS turn off propagation delay
- High switching frequency up to 1MHz.
- Extremely low quiescent current leads to low stand by power.
- Supports DCM, CCM, and Quasi-Resonant mode converters.
- Supports both high and low side synchronous rectification.
- SOT23-6 package available.

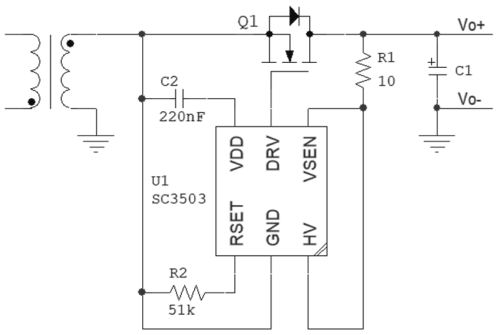
3 Applications

- Universal AC-DC Adaptors
- USB PD and QC Chargers
- Flyback Power Supplies with Variable Output Voltage
- AC-DC auxiliary supplies

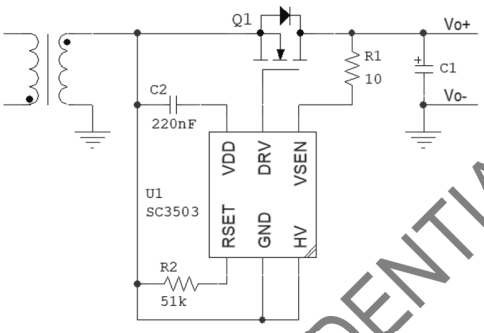
4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC3503SAER	SOT23-6	2.9mm x 2.8mm x 1.1mm

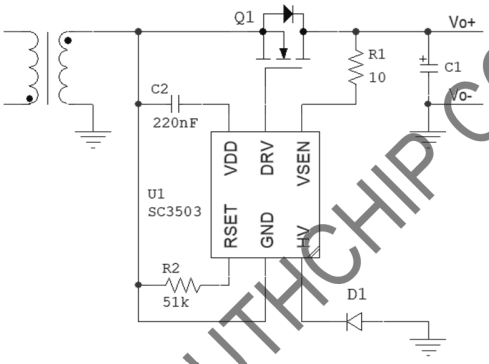
5 Typical Application Circuit



For low output voltage (VDD_{REG}=8.0V)

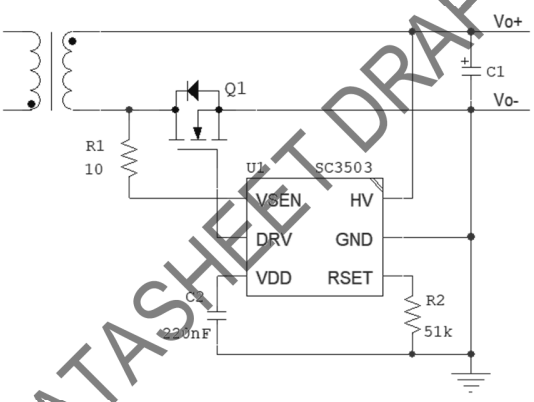


For low output voltage and Low V_{GS} MOSFET (VDD_{REG}=6.0V)

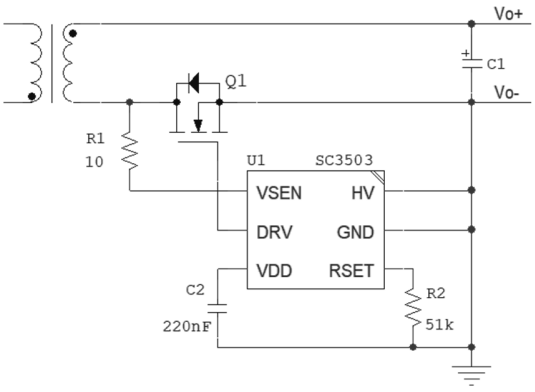


For High output voltage (VDD_{REG}=8.0V)

Figure.1 Typical Application circuit (high side)



For High V_{GS} MOSFET (VDD_{REG}=8.0V)

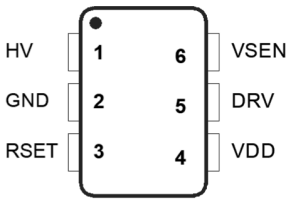


For Low V_{GS} MOSFET (VDD_{REG}=6.0V)

Figure.2 Typical Application circuit (low side)

6 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	HV	PWR	Internal power supply linear regulator input
2	GND	PWR	Ground
3	RSET	I	Auto adaptive turn-on detection
4	VDD	PWR	Power supply of IC
5	DRV	O	SR MOSFET gate driver
6	VSEN	I	SR MOSFET drain voltage sense

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

Item	Description	Min.	Typ.	Max.	Unit
Voltage range at terminals (2)	VDD, DRV to GND	-0.3	-	+12	V
	VSEN, HV to GND	-1	-	+120	V
	VSEN, HV to GND (Less than 100ns pulse width)	-3		+125	V
	RSET to GND	-0.3	-	+6.5	V
T_J	Operating Junction temperature range	-40	-	150	°C
T_{stg}	Storage temperature range	-65	-	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE (1)		SOT23-6(2.9mmx2.9mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	220	°C/W
θ_{JC}	Junction to case resistance	110	°C/W

(1) Measured on JESD51-7, 2-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) (1) HV and VSEN	-1	1	kV
	Human body model (HBM) (1) others	-2	2	kV
	Charged device model (CDM) ESD stress voltage (2) (3)	-1	1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

Item	Description	Min.	Typ.	Max.	Unit
VDD to GND	VDD voltage range to GND	4		10	V
HV, VSEN to GND	HV, VSEN voltage range to GND	-1		+115	V
C_{VDD}	VDD Capacitor	0.1	0.22	1	uF
R_{RSET}	Resistance of RSET pin connect to GND in RD mode	51		510	kΩ
R_{VSEN}	Resistance of VSEN pin connect to SR-MOS drain	0	10	200	Ω
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

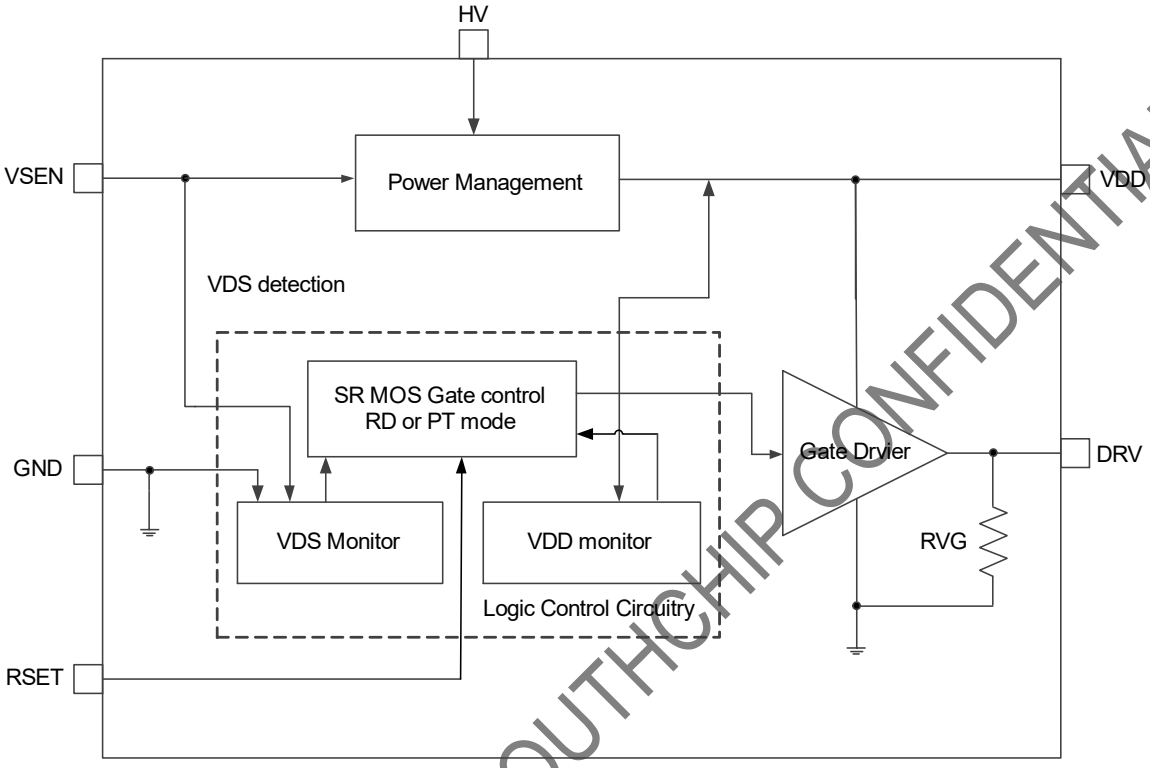
7.5 Electrical Characteristics

VDD=6V/8V, T_J= -40°C~125°C, unless otherwise noted.

PARAMETER		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE						
$V_{DD\_UVLO\_ON}$	Under voltage lockout	Rising edge	4.50	4.75	5.00	V
$V_{DD\_UVLO\_HYS}$	Under voltage lockout threshold hysteresis	Falling edge		0.25		V
VDD_{REG}	VDD regulation voltage	VSEN =12V, HV=12V	7.50	7.90	8.30	V
		VSEN =12V, HV=3V	5.60	5.90	6.20	V
SUPPLY CURRENT						
I_{VDD}	VDD charging current	VDD =7V, HV=40V	40	70		mA
		VDD =4V, VSEN=30V	40	70		mA
I_{CC}	Operating current	VDD =8V, C_{LOAD} =2.2nF, F_{SW}=100KHz		2.8	3.4	mA
		VDD =6V, C_{LOAD} =2.2nF, F_{SW}=100KHz		2.2	2.8	mA
I_{Q_VDD}	RD mode	VDD =8V		105	135	uA
	PT mode	VDD =8V		130	170	uA
I_{SD_VDD}	VDD Shutdown current	VDD =UVLO-0.1V		80	110	uA
CONTROL CIRCUITRY						
V_{MON}	Monitor voltage (VSEN)		-55	-40	-25	mV
$V_{DS\_TON\_TH}$	VDS Turn-on threshold		-150	-110	-70	mV
V_{TNOFF_TH}	Turn-off threshold (VSEN-GND)		-9	-3	3	mV
T_{D_ON}	Turn-on delay	C_{LOAD} =2.2nF		20	45	nS
T_{D_OFF}	Turn-off delay	C_{LOAD} =2.2nF		20	40	nS
T_{DOFF_PRO}	Turn-off propagation delay			10		nS
T_{ON_BLK}	Turn-on blanking time	C_{LOAD} =2.2nF	0.30	0.40	0.50	uS
T_{RSET}	RD mode	R_{RSET} =510KΩ		100		nS
	RD mode	R_{RSET} =51KΩ		20		nS
GATE DRIVER						
V_{DRV_L}	DRV low	I_{LOAD} =10mA		0.01	0.02	V
V_{DRV_H}	DRV high	I_{LOAD} =0mA		VDD		V
I_{DRV_SOURCE}	Maximum source current (1)			0.5		A
I_{DRV_SINK}	Maximum sink current (1)			4		A
R_{DRV_DOWN}	Pull-down R_{DS_ON} impedance	V_{DRV} = LOW		0.65	1.3	Ω
R_{VG}	Pull-down impedance			200		kΩ

(1) Guaranteed by characterization and design.

8 Functional Block Diagram



Function Block Diagram

9 Detailed Description

The SC3503 is designed for flyback converters, which can work in secondary side current discontinuous conduction mode (DCM), continuous conduction mode (CCM), and quasi-resonant (QR) mode. The control circuitry turns on the SR MOSFET when MOSFET's body diode conduct, and turn off it when secondary side current drops to near zero level. The IC supports both high side and low side SR.

9.1 VDD Supply

The SC3503 has a special power supply management system to adapt to high-side and low-side SR. Usually a capacitor about 100nF to 1uF is needed to connect between VDD and GND. Larger VDD capacitance leads to longer start up time and larger Vds spike, while smaller one may cause larger ripple on VDD.

The capacitor at VDD affords a stable power supply for IC. It can be charged up by both HV and VSEN. GND can be regards as the ground of IC.

The HV charges VDD via an 70mA current source, and the VDD will be regulate at 8V.

The VSEN charges VDD via an 70mA current source, and the VDD will be regulate at 6V.

9.2 UVLO

The Under Voltage Lock Out (UVLO) module of SC3503 monitors the voltage on the VDD pin. When VDD voltage is higher than $V_{DD\_UVLO\_ON}$, all parts of IC start work normally. The hysteresis of UVLO is 200mV. As soon as the voltage drops below ($V_{DD\_UVLO\_ON}$-$V_{DD\_UVLO\_HYS}$), the IC stops all modules and reenters UVLO mode.

9.3 Turn On

When SR MOSFET body diode conducts, the MOSFET need a gate drive pulse to transfer the secondary inductor current from body diode to SR MOSFET. But when the system works in DCM, the V_{DS} resonant voltage after secondary side current drops to zero may lower than 0V, this may lead the SR MOSFET conducts by mistake. For this reason, a circuit which can prevent false turn on is needed. SC3503 offer two modes to avoid this case.

In RD (rising detection) mode, SC3503 integrates a detection circuit. As soon as the SR MOSFET V_{DS} high than 0V, a built-in rising timer (T_{RISING}) begins to count. When the primary side MOSFET turns off, the SR MOSFET VDS will lower than -100mV from the set value, as the falling time ($T_{FALLING}$). An external resistor on RSET pin is needed to adjust the time T_{RSET}. If T_{RISING} is lower than the time T_{RSET} or T_{RISING}-$T_{FALLING}$ is higher than the time T_{CAL}, the SR MOSFET gate driver will pull high after a very short turn on delay time. Otherwise, the driver output will keep low level until next cycle.

In PT (platform time) mode, the circuit that can monitor the VSEN platform time is used to distinguish the turn on of primary side MOSFET or ringing in DCM/QR mode. If it's a valid primary side MOSFET turn on, the synchronous rectifier MOS will be turn on when the VDS is below -0.1V.

9.4 Minimum On time

When SR turn on, the SR starts to conduct with its maximum current. Because of transformer leakage inductance, MOSFET lead inductance and parasitic capacitance, a large ringing in VDS may occurred when SR MOSFET starts turn on. The ring may turn off the SR MOSFET by mistake. The ringing voltage can be reduced through appropriate snubber circuit and low package inductance MOSFET. To further improve the noise immunity, a turn on blanking time T_{ON_BLK} is needed after SR turn on. This function ensures that the SR on state lasts for a certain time.

9.5 Conduction Stage

After SR turn on, the secondary side current transfer from MOSFET body diode to MOSFET, no matter high side or low side SR. The current reaches its maximum level at the beginning, and then it descends at a fixed slope. The VDS can be calculated by the following equation:

$$V_{DS} = -Is * Rds(on)$$

Due to the Rds(on) changes very little in a fixed Vgs, the V_{DS} is a straight line with a fixed slope at the initial conduction stage.

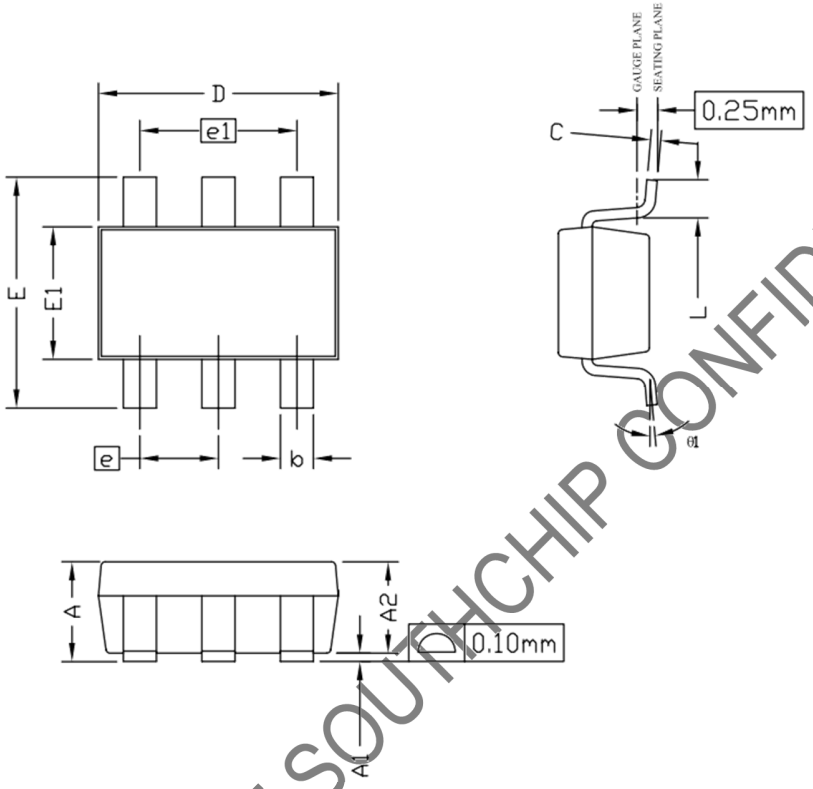
Since the current of secondary side inductor is decreasing, the VDS voltage is increasing in conduction stage. When VDS rises above -40mV, the gate of SR MOSFET can be pulled down. Lowering VGS will cause the MOSFET to withdraw from the deep saturation region gradually and turn off quickly when it needs to be turned off.

9.6 Turn Off Stage

When the VDS rises above -3mV (typ.), the SR MOSFET will be turn off quickly with 10nS propagation delay. The maximum sink current will be 4A. This large sink current ensure SR MOSFET turn off quickly even in CCM.

MECHANICAL DATA

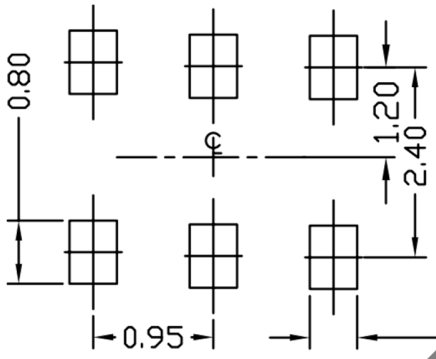
SOT23-6 (2.9mmx2.8mmx1.1mm)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	---	1.25	0.035	---	0.049
A1	0.00	---	0.15	0.00	---	0.006
A2	0.70	1.10	1.20	0.028	0.043	0.047
b	0.30	0.40	0.50	0.012	0.016	0.020
C	0.08	0.13	0.20	0.003	0.005	0.008
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.50	2.80	3.10	0.098	0.110	0.122
E1	1.50	1.60	1.70	0.059	0.063	0.067
e	0.95 BSC.			0.037BSC.		
e1	1.90 BSC.			0.075 BSC.		
L	0.30	---	0.60	0.012	---	0.024
θ1	0°	---	8°	0°	---	8°

RECOMMENDED FOOTPRINT

Example Board Layout



UNIT: mm

NOTES:

A. Publication IPC-7351 is recommended for alternate designs
B. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad