SC3806

PFC and PWM Combo Controller

Description

The SC3806 is a controller for power factor correction, switched mode power supplies. Internally synchronized leading-edge PFC and trailing-edge PWM in one IC. Its input current shaping is close to the leading edge modulation average current topology.

SC3806 allows the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply fully compliant to IEC1000-3-2 specifications.

An over-voltage comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and input voltage brownout protection. The PWM section can be operated in current mode or voltage mode, at up to 200 KHz, and includes an accurate 50% duty cycle limit to prevent transformer saturation.

SC3806's PWM can be used in current or voltage mode. In voltage mode, feed-forward from the PFC output bus can reduce secondary out ripple.

Features

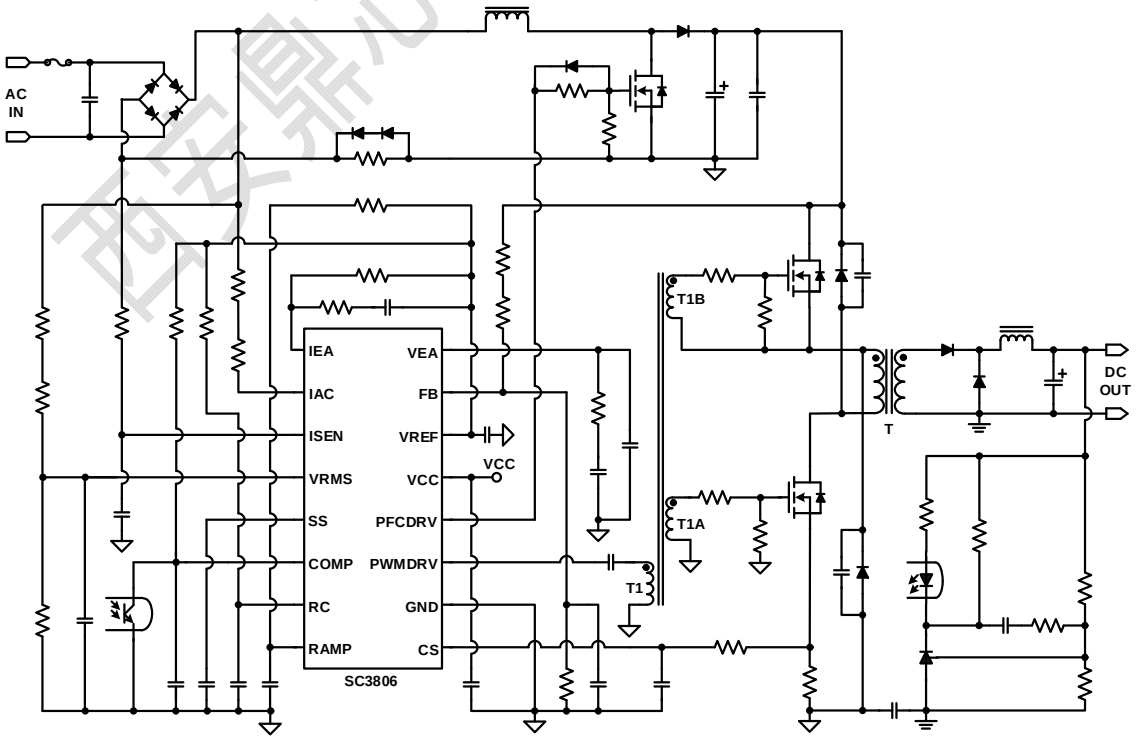
- Internally synchronized PFC and PWM
- Slew rate enhanced voltage error amplifier with advanced input current shaping technique
- Average current, continuous boost leading edge PFC
- PFC using Input Current Shaping Technique
- High PF with low total harmonic distortion
- Reduced ripple current in bulk capacitor between PFC and PWM sections
- Current-fed gain modulator for improved noise immunity
- Overvoltage and brown-out protection, UVLO, and soft start
- SOP16 and DIP-16 package

Applications

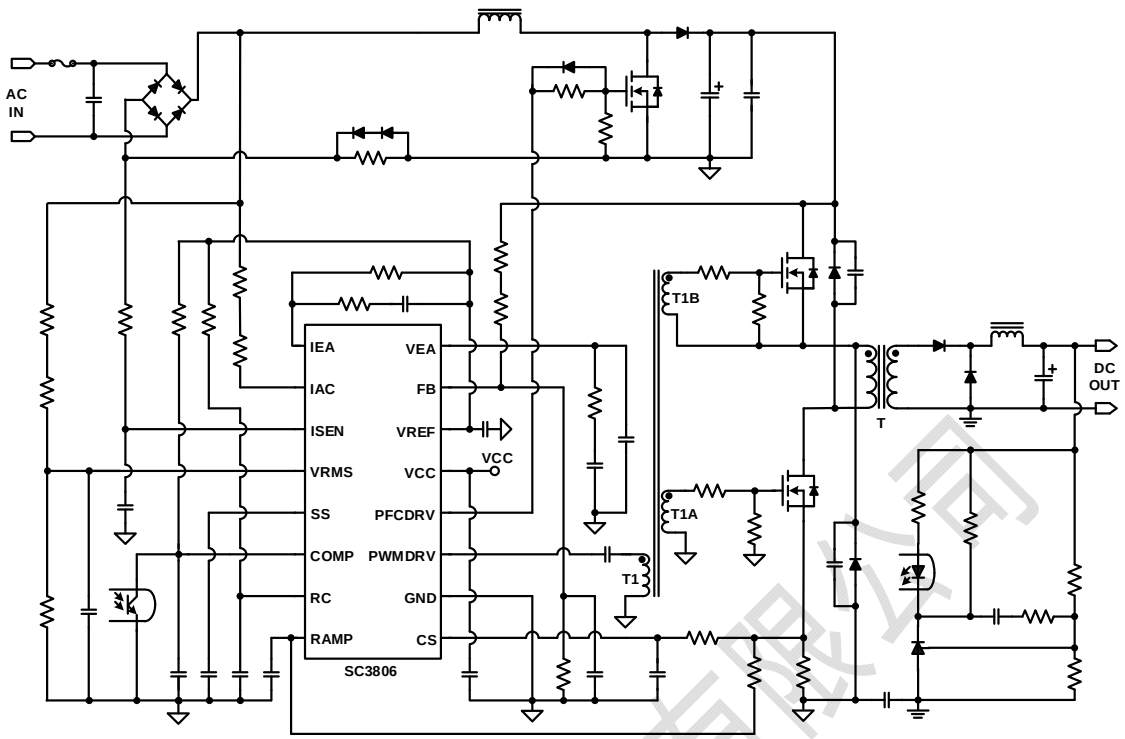
Offline AC/DC flyback converter for

- PC power supply
- Monitor power supply
- Internet server power supply

Typical Application



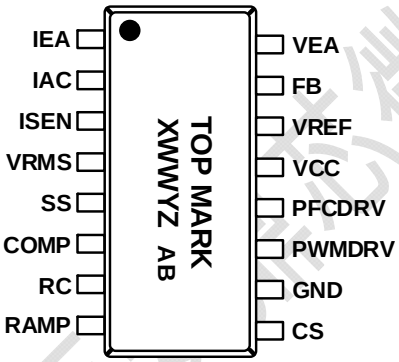
Voltage Mode



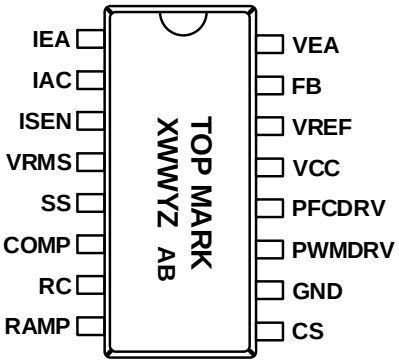
Current Mode

Pin Configuration

SOP-16 (TOP VIEW)



DIP-16 (TOP VIEW)



X: Version WW: Week Code (01-52) Y: Year Code Z&AB: internal code

Ordering Information

Part number	Package		TOP MARK	Shipping
SC3806	SOP-16	Pb-free	SC3806	Tape & Reel
SC3806T	DIP-16	Pb-free	SC3806T	Tape & Reel

Pin Descriptions

Name	Pin	Description
IEA	1	Output of PFC Current Error Amplifier. The signal from this pin is compared with an internal sawtooth to determine the pulse width for the PFC gate drive.
IAC	2	Input AC Current for PFC Gain Controller. For normal operation, this input provides a current reference for the multiplier.
ISEN	3	PFC Current Sense. The inverting input of the PFC current amplifier and the output of multiplier and PFC current sense comparator.
VRMS	4	Line-Voltage Detection. The pin is used for PFC line voltage compensation.
SS	5	PWM Soft-Start. During startup, the SS pin charges an external capacitor with a 10μA constant current source.
COMP	6	PWM Feedback Input. The control input for voltage-loop feedback of PWM stage.
RC	7	Oscillator RC Timing Connection. Oscillator timing set by RT and CT.
RAMP	8	PWM RAMP Input. In Current Mode, this pin functions as the current-sense input. In Voltage Mode, it is the feed-forward sense input from PFC output.
CS	9	Peak Current Limit Setting for PWM. The peak current limit setting for PWM.
GND	10	Ground
PWMDRV	11	PWM Gate Drive. The totem-pole output drive for the PWM MOSFET.
PFCDRV	12	PFC Gate Drive. The totem-pole output drive for PFC MOSFET.
VCC	13	Power Supply.
VREF	14	Reference Voltage. Buffered output for the internal 7.5V reference.
FB	15	Voltage Feedback Input for PFC. The feedback input for PFC voltage loop. The inverting input of PFC error amplifier.
VEA	16	Output of PFC Voltage Amplifier. The error amplifier output for PFC voltage feedback loop.

Absolute Maximum Ratings

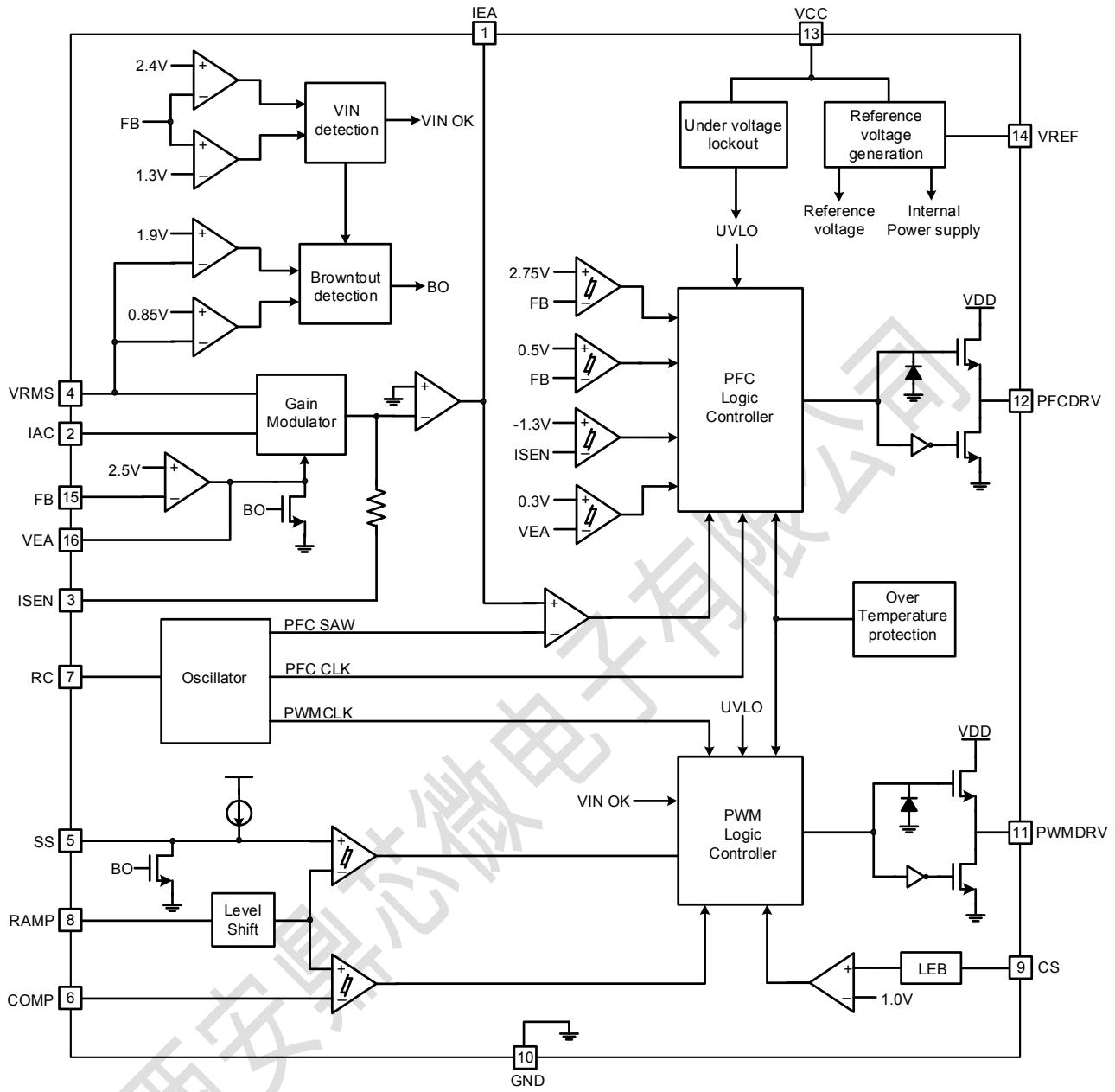
Symbol	Parameter	Min.	Max.	Unit
V_{CC}	VCC voltage		25.0	V
V_{IEA}	IEA voltage	0	VREF+0.3	V
V_{IAC}	IAC voltage	GND-0.3	7.0	V
V_{ISEN}	ISEN Voltage	-5.0	0.7	V
V_{VRMS}	VRMS voltage	GND-0.3	7.0	V
V_{SS}	SS voltage	GND-0.3	18.0	V
V_{COMP}	COMP voltage	GND-0.3	18.0	V
V_{RC}	RC voltage	GND-0.3	7.0	V
V_{RAMP}	RAMP voltage	GND-0.3	18.0	V
V_{CS}	CS voltage	GND-0.3	7.0	V
V_{PWMDRV}	PWMDRV Voltage	GND–0.3	VCC + 0.3	V
V_{PFCDRV}	PFCDRV Voltage	GND–0.3	VCC+ 0.3	V
V_{REF}	VREF Voltage	0	18.0	V
V_{FB}	FB Voltage	GND–0.3	7.0	V
V_{EA}	VEA Voltage	GND-0.3	7.0	V
I_{CC}	I_{CC} Current (Average)		10	mA
I_{PFCDRV}	Peak PFCDRV Current, Source or Sink		0.5	A
I_{PWMDRV}	Peak PWMDRV Current, Source or Sink		0.5	A
T_{STG}	Storage Temperature Range	-65	150	℃
T_J	Operating Temperature Range	-40	125	℃
T_L	Lead Temperature (Soldering, 10 sec)		260	℃
R_{JA}	Thermal Resistance (θJA)	DIP16	80	℃/W
		SOP16	100	℃/W
ESD	Human Body Model,JEDEC:JESD22-A114		2.5	KV
	Machine Model, JEDEC:JESD22- A115		250	V

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device’s reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	10.0	21.0	V
T_A	Operating Ambient Temperature	-40	125	℃

Block Diagram



Electrical Characteristics

(T_A = 25℃, V_{CC}=15.0V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VCC) Section						
I_{CC_ST}	Startup Current	VCC=V_{UVLO_OFF}-0.1V		10	20	μA
I_{CC_OP}	Operating Current	VCC=15V, C_L=0		2.5	4.0	mA
V_{UVLO_OFF}	VCC Under Voltage Lockout Exit		11.2	12.0	12.8	V
V_{UVLO_ON}	VCC Under Voltage Lockout Enter		9.2	10.0	10.8	V
V_{CC_OVP}	VCC Over Voltage Protection Voltage		22.0	23.0	24.0	V
$V_{CC\_OVP\_HY}$	VCC Over Voltage Protection Voltage Hysteresis			1.0		V
VREF Section						
V_{VREF}	Reference Voltage	I_{VREF}=0mA,C_{VREF}=0.1uF	7.35	7.5	7.65	V
$\triangle V_{VREF1}$	Load Regulation of Reference Voltage	C_{VREF}=0.1μF,I_{VREF}=0mA to 3.5mA		30	50	mV
$\triangle V_{VREF2}$	Line Regulation of Reference Voltage	C_{VREF}=0.1μF, V_{CC}=10V to16V			25	mV
$\triangle V_{VREF-DT}$	Temperature Stability	-40℃~105℃		0.4		%
$I_{VREF-MAX}$	Maximum Current	V_{VREF}>7.35V	5.0			mA
RC(Oscillator) Section						
Fs	Operation Frequency	R_T=6.8K,C_T=1000pf	60	64	67	KHz
$\Delta_{freq/V}$	Voltage Stability	10.0V<VCC<15.0V			2	%
$\Delta_{freq/T}$	Temperature Stability				2	%
V_{PP_RC}	Ramp Voltage	Valley to Peak		2.8		V
$I_{OSC-DIS}$	Discharge Current	V_{RAMP}=0V,V_{RC}=2.5V	6.5		15.0	mA
$T_{PFC-DEAD}$	PFC Dead Time			600		ns
Voltage Error Amplifier Section						
V_{REF}	Reference Voltage		2.45	2.50	2.55	V
A_V	Open Loop Gain			42		dB
Gmv	Transconductance	V_{NONINV}=V_{INV},V_{VEA}=3.75V	50	70	90	μmho
I_{FB_L}	Maximum Source Current	V_{FB}=2V,V_{VEA}=1.5V		50		μA
I_{FB_H}	Maximum Sink Current	V_{FB}=3V,V_{VEA}=6.0V		-50		μA
I_{BIAS}	Input Bias Current		-1		1	μA
V_{VEA_H}	Output High Voltage			6.0		V
V_{VEA_L}	Output Low Voltage			0.1		V

Current Error Amplifier Section						
Gmi	Transconductance	$V_{NONINV}=V_{INV}, V_{IEA}=3.75V$		88		μmho
V_{OFFSET}	Input Offset Voltage	$V_{VEA}=0V$,IAC open	-10		10	mV
A_I	Open Loop Gain			50		dB
I_{IEA_L}	Maximum Source Current	$V_{FB}=2V, V_{VEA}=1.5V$		50		μA
I_{IEA_H}	Maximum Sink Current	$V_{FB}=3V, V_{VEA}=6.0V$		-50		μA
V_{IEA_H}	Output High Voltage	$V_{ISEN}=0.6V, V_{IEA}=4.0V$		7.5		V
V_{IEA_L}	Output Low Voltage	$V_{ISEN}=-0.6V, V_{IEA}=1.5V$		0.1		V
Gain Modulator Section						
IAC	Input for AC Current	Multiplier Linear Range	0		65	μA
GAIN		$I_{AC}=17μA, V_{RMS}=1.08V, V_{FB}=2.25V$		7.94		
		$I_{AC}=20μA, V_{RMS}=1.22V, V_{FB}=2.25V$		6.75		
		$I_{AC}=25μA, V_{RMS}=1.5V, V_{FB}=2.25V$		3.95		
		$I_{AC}=51μA, V_{RMS}=3.0V, V_{FB}=2.25V$		0.94		
		$I_{AC}=62μA, V_{RMS}=3.8V, V_{FB}=2.25V$		0.68		
BW	Bandwidth	$I_{AC}=40μA$			2	KHz
Vo(gm)	Output Voltage= $5.7K\Omega X(I_{SEN}-I_{OFFSET})$	$I_{AC}=50μA, V_{RMS}=1.22V, V_{FB}=2.25V$		0.8		V
Soft-Start Section						
V_{SS_MAX}	Maximum Voltage		10.0	10.5	11.0	V
I_{SS}	Soft-start Current			10		μA
Brownout Section						
V_{RMS_UVL}	VRMS Threshold Voltage LOW			1.05		V
V_{RMS_UVL}	VRMS Threshold Voltage High			1.9		V
T_{UVP}	Under Voltage Protection Delay		0.75	1.0	1.25	s
Sagging Protection Section						
V_{RMS_SAG}	VRMS Threshold SAG LOW			0.85		V
T_{SAG}	SAG Protection Delay			30		ms
PFC OVP Section						
V_{PFC_OVP}	PFC Over Voltage Protection Threshold	Normal operation	2.70	2.75	2.80	V
$\triangle V_{PFC\_OVP}$	PFC OVP Hysteresis			0.25		V
Low Power Detect Section						
V_{VEAOFF}	VEA Voltage OFF PFCDRV		0.2	0.3	0.4	V

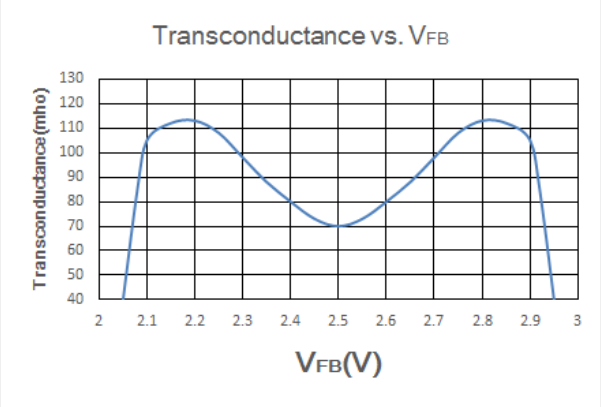
VIN OK Detect Section						
V_{IN_OK}	PWM ON Threshold Voltage		2.3	2.4	2.5	V
V_{IN_OFF}	PWM OFF Threshold Voltage		1.2	1.3	1.4	V
PFC Current Sense Section						
V_{PFC_SEN}	Peak Current Limit Voltage Threshold		-1.2	-1.3	-1.4	V
PFC UVP Protection Section						
V_{PFC_UVP}	PFC Under Voltage Protection Threshold		0.4	0.5	0.6	V
PWM CS Sense Section						
V_{CS_PK}	CS Peak Voltage Threshold		0.95	1.0	1.05	V
T_{PD}	Propagation Delay to Output			250		ns
T_{LEB}	Leading-Edge Blanking Time			250		ns
V_{PWM_LS}	PWM Comparator Level Shift		1.3	1.5	1.8	V
PFCDRV Section						
$D_{\_MIN}$	Minimum Duty Cycle	V_{IEA}>4.5V			0	%
$D_{\_MAX}$	Maximum Duty Cycle	V_{IEA}<1.2V	94	97		%
V_{LOW_PFC}	Output Low Voltage	I_{OUT}=-100mA			1.5	V
V_{HIGH_PFC}	Output High Voltage	I_{OUT}=100mA,VCC=15V	8.0			V
V_{PFCDRV_CLAMP}	PFCDRV Output Clamp Voltage	VCC=18.0V		15.0		V
T_{R_PFC}	Rise time	C_L=4.7nF, 2V~9V		65		ns
T_{F_PFC}	Fall time	C_L=4.7nF, 9V~2V		40		ns
PWMDRV Section						
$D_{\_MAXPWM}$	Maximum Duty Cycle		49.0	49.5	50	%
V_{LOW_PWM}	Output Low Voltage	I_{OUT}=-100mA			1.5	V
V_{HIGH_PWM}	Output High Voltage	I_{OUT}=100mA,VCC=15V	8.0			V
V_{PFCDRV_CLAMP}	PFCDRV Output Clamp Voltage	VCC=18.0V		15.0		V
T_{R_PWM}	Rise time	C_L=4.7nF, 2V~9V		65		ns
T_{F_PWM}	Fall time	C_L=4.7nF, 9V~2V		40		ns

Note:

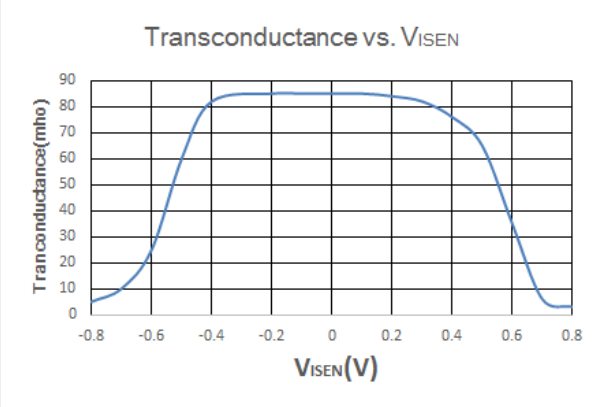
1. Limits are guaranteed by 100% testing, or correlation with worst-case test condition.
2. The gain is the maximum gain of modulation with a given V_{RMS} voltage when V_{VEA} is saturated to high.
3. $Gain = K \times 5.375V$； $K = \dfrac{(I_{SEN} - I_{OFFSET})}{I_{AC} \times (V_{EA} - 0.625)}$； $V_{EA(MAX)} = 6.0V$

Typical Performance Characteristics

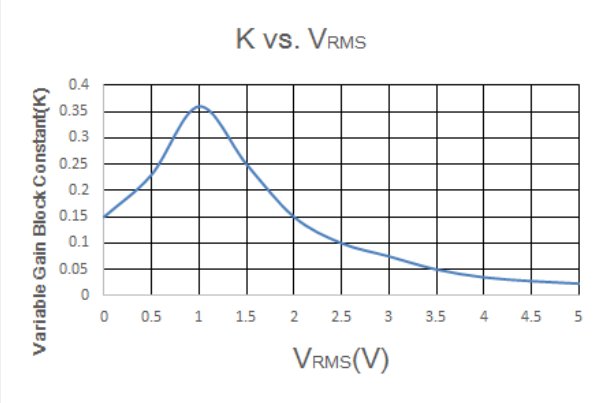
(T_A = 25℃, V_{CC}=15V, unless otherwise noted)



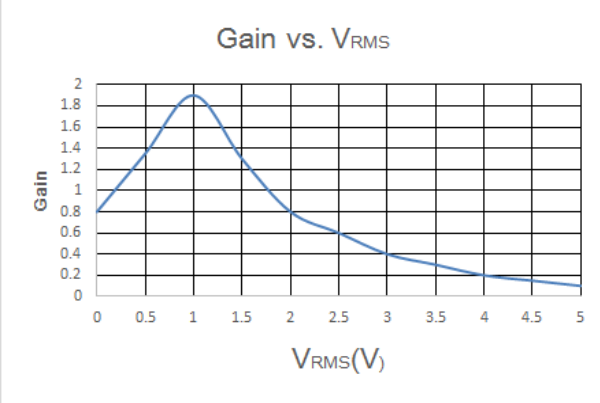
Voltage Error Amplifier(Gmv) Transconductance



Current Error Amplifier(Gmi) Transconductance



Gain modulator Transfer Characteristic(K)



Gain vs. V_{RMS}

$$K = \frac{I_{GAINMOD} - I_{OFFSET}}{I_{AC} \times (6 - 0.625)} mV^{-1}$$

$$Gain = \frac{I_{SEN} - I_{OFFSET}}{I_{AC}}$$

Functional Description

Gain Modulator

Gain Modulator plays an important role in PFC section, because it provides the reference to the current control amplifier for the input current shaping， as show in figure 1, The gain modulator's output current is a function of V_{EA}, I_{AC} and V_{RMS}. The gain modulator's gain is given as a ratio between I_{MO} and I_{AC} with a given V_{RMS} when V_{EA} is saturated to high. The gain is inversely proportional to V_{RMS}^2, as shown in figure 2 , to implement line feed-forward. This automatically adjusts the reference of current control error amplifier according to the line voltage, such that the input power of PFC converter is not changed with line voltage, as shown as Figure 3.

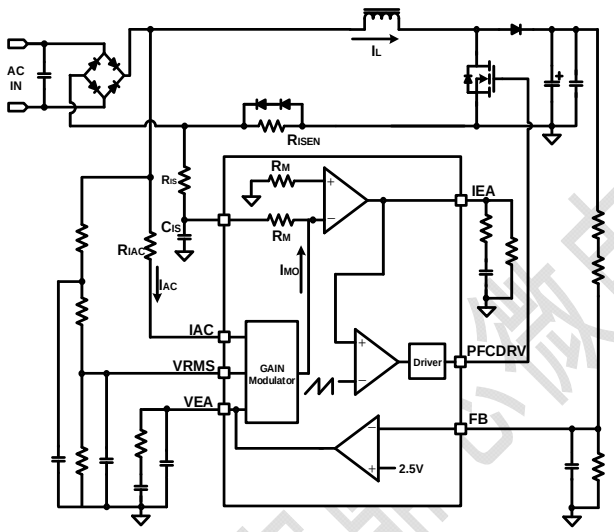


Figure 1. PFC Modulation Block

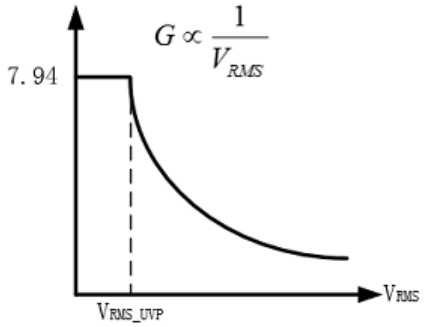


Figure 2. Modulation Gain Characteristics

To sense the VRMS value of the line voltage, averaging circuit with two poles is typically employed, as shown in figure 1. Notice that the input voltage of PFC is clamped at the peak of the line voltage once the PFC stops switching because the junction capacitance of the bridge diode is not discharged, as shown in figure 4. Therefore, the voltage divider for V_{RMS} should be designed considering the brownout protection trip-point and minimum operation line voltage.

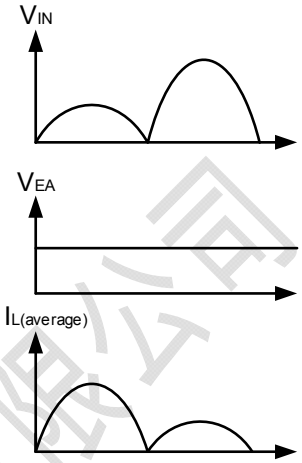


Figure 3. Line Feed-forward operation

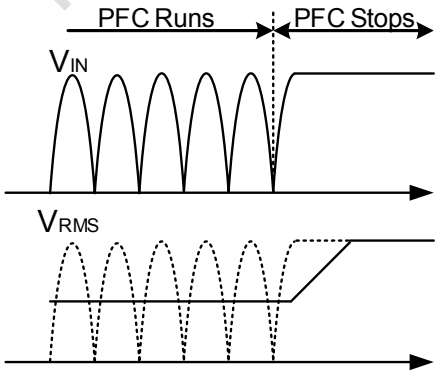


Figure 4. V_{RMS} According to the PFC Operation

The rectified sinusoidal signal is obtained by the current flowing into the IAC pin. The resistor R_{IAC} should be large enough to prevent saturation of the gain modulator, calculating as:

$$\frac{\sqrt{2}\times V_{LINE\_MIN}}{R_{IAC}}\times G_{MAX} < 135uA$$

Where V_{LINE_MIN} is the line voltage that trips brownout protection, G_{MAX} is the maximum modulator gain when V_{RMS} is 1.08V (which can be found in the datasheet), and 135uA is the maximum output current of gain modulator.

Current control of boost stage

The SC3806 employs two control loops for power factor correction, as shown in figure 1: a current control loop and a voltage-control loop. The current-control loop shapes inductor current as shown in figure 5 based on the reference signal obtained at the IAC pin calculated as:

$$I_L \times R_{SEN} = I_{MO} \times R_M = I_{AC} \times G \times R_M$$

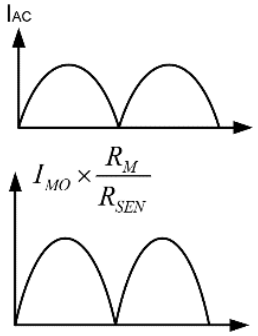


Figure 5. Inductor Current Shaping

The current-control feedback loop also has pulse-by-pulse current limit comparator that forces the PFC switch to turn off until the next switching cycle if the ISEN pin voltage drops below -1.3V.

Voltage control of boost stage

The voltage-control loop regulates PFC output voltage using an internal error amplifier such that the feedback voltage V_{FB} is the same as the internal reference voltage of 2.5V.

Brownout Protection

The build-in internal brownout protection comparator monitors the voltage of the VRMS pin. Once VRMS pin voltage is lower than 1.05V, the PFC stage is shut down to protect the system from over current. SC3806 starts up the boost stage once V_{RMS} voltage increase above 1.9V.

Oscillator

The internal oscillator frequency is determined by the timing resistor R_T and capacitor C_T on the RC pin as shown in Figure 6. The frequency of the internal oscillator is given:

$$F_{OSC} = \frac{1}{0.56 \times R_T \times C_T + 360 \times C_T}$$

Because the PWM stage generally uses a forward converter, it is necessary to limit the maximum duty cycle at 50%. To have a small tolerance of the maximum duty cycle, a frequency divider with toggle flip-flops is used, as illustrated in Figure 6. The operation frequency of PFC and PWM stage is 1/4 of oscillator frequency.

The dead time for the PFC gate drive signal is determined by:

$$T_{DEAD} = 360 \times C_T$$

The dead time should be smaller than 2% of the switching period to minimize line current distortion around the line zero crossing.

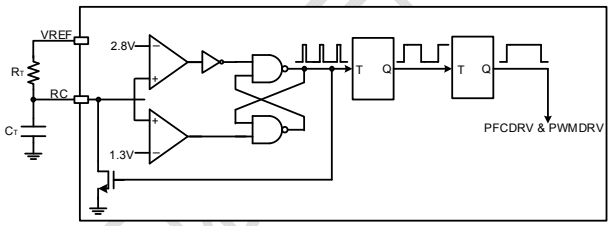


Figure 6. Oscillator Configuration

PWM stage

The PWM stage is capable of current mode or voltage mode operation. In current mode, the PWM ramp is usually derived directly from a current-sensing resistor or current transformer in the primary side of the output stage, and is thereby representative of the current flowing in the converter's output stage. CS, which provides cycle-by-cycle current limiting, is typically connected to RAMP in such applications.

For voltage mode operation, RAMP can be connected to a separate RC timing network to generate a voltage ramp against which the COMP voltage is compared. Under these conditions, the voltage feed-forward from the PFC bus can be used for better line transient response.

No voltage error amplifier is included in the PWM stage, as this function is generally performed by TL431, in the secondary side. To facilitate the design of opto-coupler feedback circuitry, an offset voltage is built into the inverting input of PWM comparator. This allows COMP to command a zero percent duty cycle when its pin voltage is below 1.5V.

PWM current limit

The CS pin is a direct input to the cycle-by-cycle current limiter for the PWM section. If the input

voltage at this pin exceeds 1V, the output of the PWM is disable until the start of the next PWM clock cycle.

PWM Soft-Start

PWM startup is controlled by the soft-start capacitor. A current source of 10uA supplies the charging current for the soft-start capacitor. PWM startup is prohibited until the soft-start capacitor voltage reached 1.5V.

V_{IN} OK comparator

The V_{IN} OK comparator monitors the output of the PFC stage and inhibits the PWM stage if this voltage less than 2.4V. Once this voltage goes above 2.4V, the PWM stage begins soft-start. The PWM stage is shut down when FB voltage drops below 1.3V.

PFC Over-Voltage Protection

In the SC3806, the PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load changes suddenly. A resistor divider from the high- voltage DC output of the PFC is fed to FB pin. When the voltage V_{FB} exceeds 2.75V, the PFC output driver is shut down. The PWM section continues to operate. The OVP comparator has 250mV of hysteresis and the PFC does not restart until the voltage V_{FB} drops below 2.50V.

Line sag protection

When the line sags below its normal operational range, the PFC part keeps operating until the brownout protection is triggered, which has 1s debounce time. Due to the low line voltage , the gain modulator for current loop is saturated and input current of PFC is limited, resulting in a drop of the PFC output voltage at heavy-load condition. Since the PWM section has a V_{IN} OK comparator that shuts down PWM operation when the FB voltage drops below 1.3V, the downstream DC/DC converter can stop operation while the PFC output voltage drops during line sag. Once the downstream converter stops operation, even the limited PFC input current can charge up the PFC output since the PFC part has no load current. Because this can cause repeated startup and shutdown of downstream converter during line sag. SC3806 has line sag protection.

There are two conditions that trigger line sag protection. The first condition is when V_{RMS} is lower than V_{RMS_SAG}(0.85V) , another condition is that V_{FB} is lower than Vin-off (1.3V). Once line sag protection is triggered, the PWM and the PFC stop operation until V_{RMS} increase above 1.9V.

Leading/Trailing Modulation

Conventional PWM techniques employ trailing-edge modulation, in which the switch turns on right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the on-time of the switch. Figure 7 shows a typical trailing-edge control scheme.

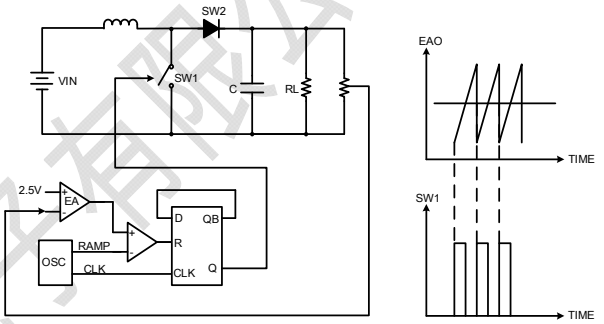


Figure 7. Typical Trailing-edge Control Scheme

In the case of leading-edge modulation, the switch is turned off exactly at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch is turned on. The effective duty-cycle of the leading-edge modulation is determined during off-time of the switch. Figure 8 shows a leading-edge control scheme.

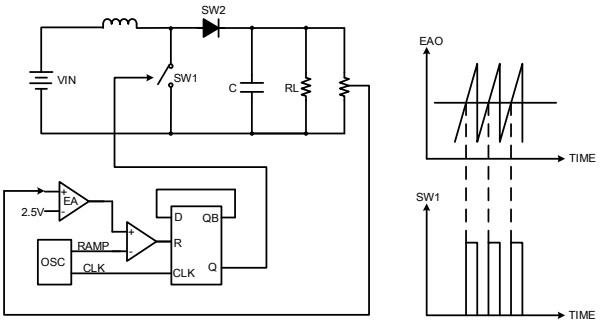


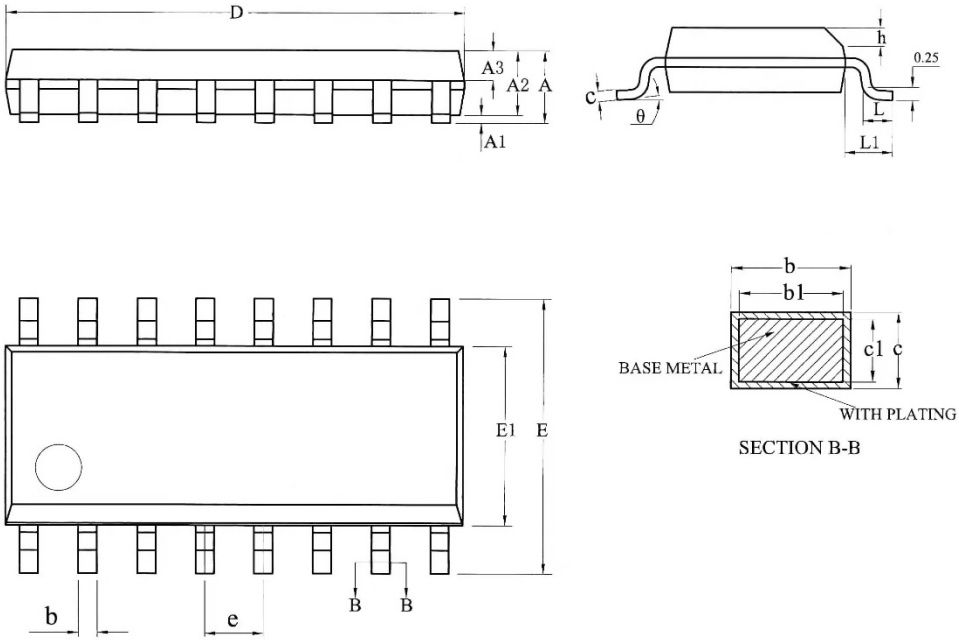
Figure 8. Typical Leading-edge Control Scheme

One of the advantages of this control technique is that it requires only one system clock. Switch(SW1) turns off and Switch(SW2) turns on at the same instant to minimize the momentary no-load period, thus lowering ripple voltage

generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using the leading-edge modulation method.

Package Information

SOP-16 package

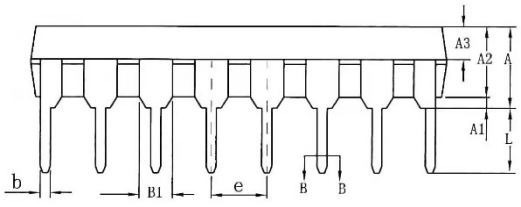


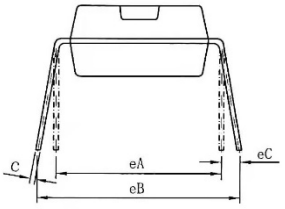
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

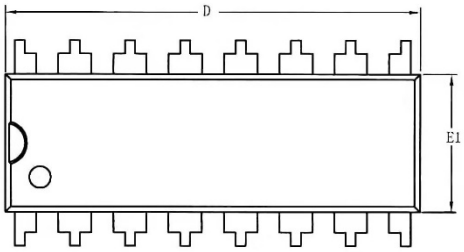
Note:

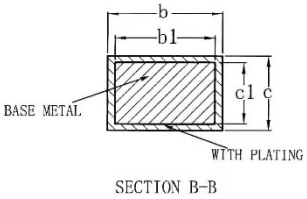
1. All dimensions are in millimeters
2. Package length does not include mold flash protrusion or gate burr
3. Package WIDTH does not include mold flash protrusion
4. Drawing is not to scale

DIP-16 package









SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	—	—
A2	3.20	3.30	3.40
A3	1.47	1.52	1.57
b	0.44	—	0.52
b1	0.43	0.46	0.49
B1	1.52RFE		
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	19.00	19.10	19.20
E1	6.25	6.35	6.45
e	2.54BSC		
eA	7.62REF		
eB	7.62	—	9. 30
eC	0	—	0. 84
L	3.00	—	—

Note:

1. All dimensions are in millimeters
2. Package length does not include mold flash protrusion or gate burr
3. Package WIDTH does not include mold flash protrusion
4. Drawing is not to scale

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