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Dual Synchronous Buck Controller with Tracking Start-up/Shutdown

Features

- VIN Range 3-25V
- Outputs Adjustable from 0.75 to 5.25V, or
- Preset Output Voltages:
  - VOUT1 = 1.8 or 1.5V
  - VOUT2 = 1.25 or 1.05V
- Proportional or Coincident Tracked Start-up and Shut-down of Both Outputs
- Adjustable Soft-start Rates for Each Output
- Regulated Shutdown for Each Output
- Low Shutdown Power
- Constant On-Time for Fast Dynamic Response
- Adjustable Switching Frequency
- Separated Frequencies for Minimal Switching Interaction:
  - VOUT1 = up to 600kHz
  - VOUT2 = up to 720kHz
- Power Save or Continuous Operation at Light Load
- Over-Voltage and Under-Voltage Fault Protection
- Cycle-by-Cycle Valley Current Limit
- DC Current Sense Using Low-Side RDSON Sensing, or RSENSE In Source of Low-Side MOSFET for Greater Accuracy
- Separate Power Good Outputs
- Separate Enable/Power Save Inputs
- 3.1A Non-Overlapping Gate Drive
- SmartDrive™ for High-side MOSFET
- MLP 4x4 24 Pin Lead-free Package
- Industrial Temperature Range
- WEEE and RoHS Compliant

Applications

- Notebook and Sub-Notebook Graphics
- Voltage Controllers
- Tablet PCs
- Embedded Applications

Description

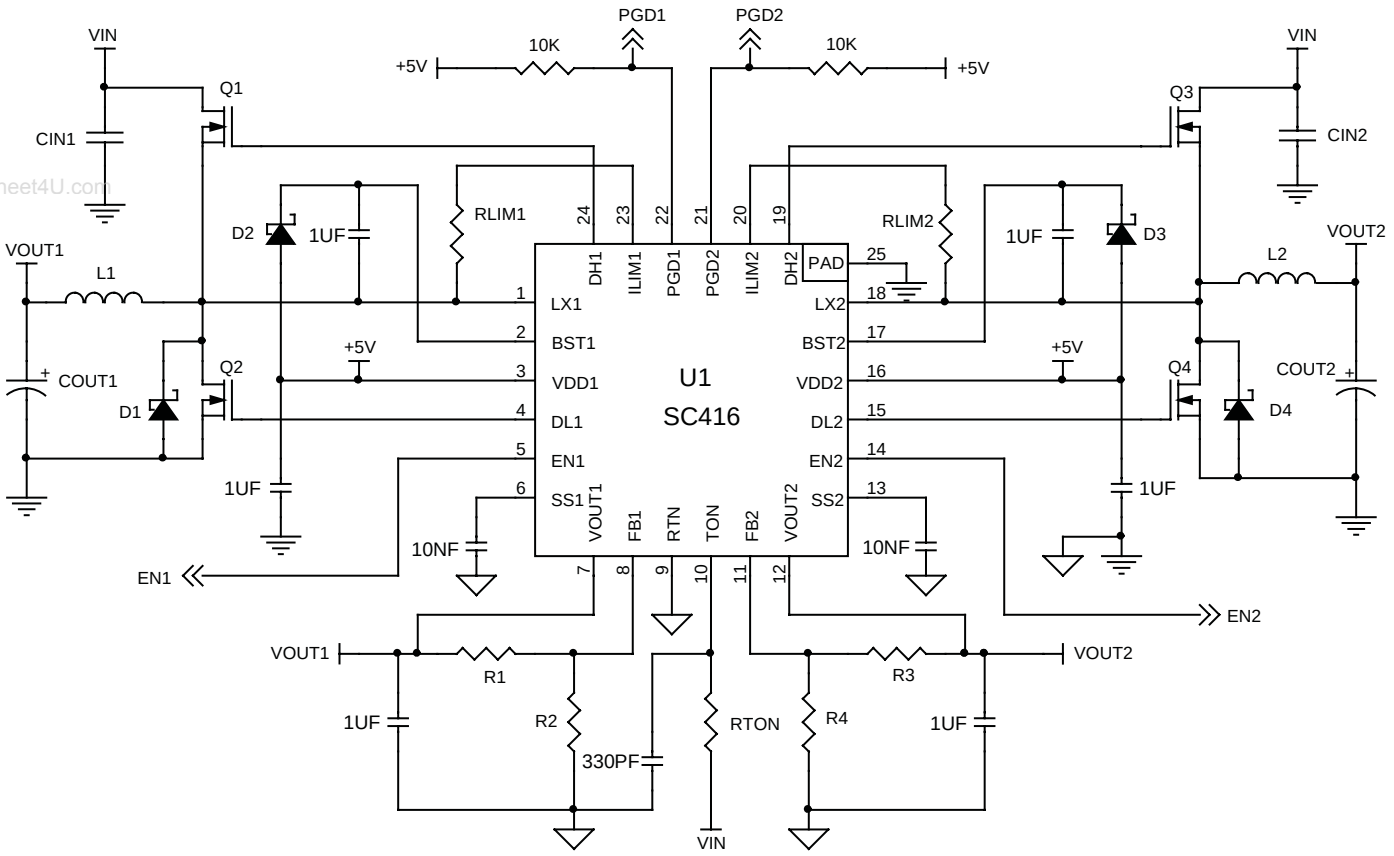
The SC416 is a versatile, constant on-time, pseudo-fixed-frequency, dual synchronous buck PWM controller intended for notebook computers and other battery operated portable devices. The SC416 contains all the features needed to provide cost-effective control of two independent switchmode power supplies.

The SC416 provides adjustable voltage tracking during start-up and shut-down, making it an effective solution for a variety of applications where the voltage differential between supply rails must meet defined limits during all operating conditions including start-up and shut-down. The SC416 supports proportional tracking which gives equal start-up and shut-down times for both outputs, and can also provide coincident tracking where the two output voltages are equal during the lower voltage's start-up and shut-down ramp.

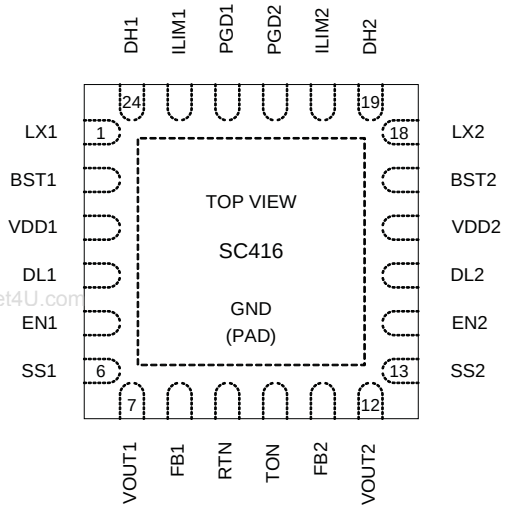
The two DC outputs are adjustable from 0.75V to 5.25V. Additional features for each output include cycle-by-cycle current limit, voltage soft-start, under-voltage and over-voltage protection, programmable over-current protection, regulated shutdown, selectable power save and non-overlapping gate drive. The SC416 provides two enable/power save inputs, two soft-start inputs, two power good outputs and an on-time adjust input.

The constant on-time topology provides fast dynamic response. The excellent transient response means that SC416 based solutions require less output capacitance than competing fixed frequency converters. Switching frequency is constant until a step in load or line voltage occurs, at which time the pulse density and frequency moves to counter the change in output voltage. After the transient event, the controller frequency returns to steady state operation. At light loads with power save enabled, the SC416 reduces switching frequency for improved efficiency.

Typical Application Circuit



Pin Configuration



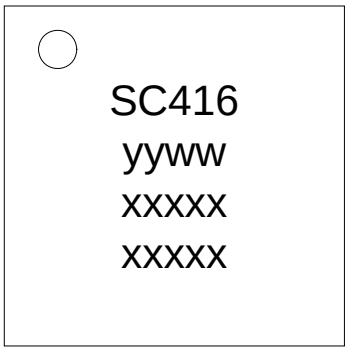
MLPQ24: 4x4 24 LEAD

Ordering Information

Device	Package
SC416MLTRT[1][2]	MLPQ-24 4X4
SC416EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Available in lead-free package only. Device is WEEE and RoHS compliant.

Marking Information



nnnn = Part Number (example: SC416
yyww = Date Code (example: 0652)
xxxxx = Semtech Lot No. (example: 09010
xxxxx 01-10)

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Absolute Maximum Ratings

DHx, BSTx to GND (DC) ..... -0.3 to +30V
DHx, BSTx to GND (transient - 100nsec max) ..... -2.0 to +33V
LXx, TON to GND (DC) ..... -0.3 to +25V
LXx, TON to GND (transient - 100nsec max) ..... -2.0 to +28V
BST1 to LX1, BST2 to LX2 (DC) ..... -0.3 to +6.0V
BST1 to LX1, BST2 to LX2 (transient - 100nsec max) ..... -0.3 to +7.5V
DLx to GND (DC) ..... -0.3 to +6.0V
GND to RTN ..... -0.3 to +0.3V
VDDx to RTN ..... -0.3 to +6.0V
ENx, FBx, ILIMx, PGDx, SSx, VOUTx to RTN..... -0.3 to VDDx +0.3V
Peak IR Reflow Temperature(10-40s)..... 260°C
ESD Protection Level[2] 2kV

Thermal Information

Junction to Ambient[1] ..... 29°C/W
Storage Temperature Range ..... -60 to +150°C
Operating Junction Temperature Range ... -40 to +125°C
Lead Temperature (Soldering) 10 sec ..... 260°C

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES-
(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.
(2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Test Conditions: V_{IN} = 15V, V_{OUT} = 1.5V, T_A = 25 °C, 0.1% resistor dividers; RTON = 1Meg; VDD1/2 = 5.0V; GND connects to PAD pin.

Parameter	Conditions	25°C			-40° to 85°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VIN Input Voltage		3.0		25			V
VDDx Input Voltage		4.5		5.5			V
VDD1 + VDD2 Shutdown Current	EN1, EN2 = 0V		7			10	µA
VDD1 + VDD2 Operating Current	EN1, EN2 = 5V (Powersave Mode) FB1, FB2 > REF		800			1200	µA
Regulation							
FB1, FB2 On-Time Threshold	0 to 85°C -40 to 85°C		0.75		0.7425 0.7388	0.7575 0.7612	V
VOUTx Output Voltage Range	External Resistors				0.75	5.25	V
VOUT1 On-Time Threshold	FB1 = 5V; 0 to 85°C FB1 = 5V; -40 to 85°C		1.8		1.7775 1.7685	1.8225 1.8315	V
	FB1 = RTN; 0 to 85°C FB1 = RTN; -40 to 85°C		1.5 1.5		1.4812 1.4737	1.5188 1.5263	V

Electrical Characteristics (continued)

Parameter	Conditions	25°C			-40° to 85°C		Units
		Min	Typ	Max	Min	Max	
Regulation (Continued)							
VOUT2 On-Time Threshold	FB2 = 5V; 0 to 85°C FB2 = 5V; -40 to 85°C		1.25 1.25		1.2343 1.2281	1.2656 1.2718	V
	FB2 = RTN; 0 to 85°C FB2 = RTN; -40 to 85°C		1.05 1.05		1.0368 1.0316	1.0631 1.0684	V
VOUTx Line Regulation Error			0.04				%/V
VOUTx Load Regulation Error			0.3				%
Timing							
VOUTx On-Time[1] *VOUTx Set to 1.5V*	VOUT1; RTON = 1Meg VOUT2; RTON = 1Meg VOUT1; RTON = 499K VOUT2; RTON = 499K		400 330 200 167		320 260	480 400	nsec
Minimum On-Time	DH1, DH2		50				ns
Minimum Off-Time	DL1, DL2		330				ns
Soft-Start/Shutdown							
Soft-Start SSx Current Source			5		3.5	6.5	µA
Shutdown SSx Current Sink			5		3.5	6.5	µA
Soft-Start Ramp Time	CSSx = 4.7nF		700				µsec
SSx Shutdown Discharge Resistance	ENx = RTN, VOUTx < 300mV		16				Ω
VOUTx Shutdown Discharge Resistance	ENx = RTN, VOUTx < 300mV		16				Ω
Analog Inputs/Outputs							
VOUT1 Input Resistance	EN1 = VDD1		120				kΩ
VOUT2 Input Resistance	EN2 = VDD2		90				kΩ
FBx Input Bias Current					-1	+1	µA
Current Sense							
ILIMx Source Current			10		9	11	µA
ILIMx Comparator Offset	ILIMx - GND				-10	+10	mV
Current Limit (Negative)	LXx - GND		80		60	100	mV
Zero Crossing Detector Threshold	LXx - GND				-7	+7	mV
Power Good							
PGDx Threshold	1% Hysteresis Typical, with Respect to Regulation Point		-12		-9	-15	%
PGDx Threshold Delay Time [2]			5				µs

Electrical Characteristics (continued)

Parameter	Conditions	25°C			-40° to 85°C		Units
		Min	Typ	Max	Min	Max	
PGDx Leakage						1	µA
Fault Protection							
VDD1 Under-Voltage Lockout	VDD1 Falling Edge		4.0		3.7	4.35	V
VOUTx Under-Voltage Fault	VOUTx Falling Edge		-30		-35	-25	%
VOUTx Under-Voltage Fault Delay (2)			8				clks
VOUTx Over-Voltage Fault			+20		+17	+23	%
VOUTx Over-Voltage Fault Delay (2)			5				µs
Thermal Shutdown (2)	Latching, >10°C Hysteresis		160				°C
Inputs/Outputs							
EN1, EN2 Input Low Voltage	VOUTx Disabled					1.2	V
ENx Input - Forced Continuous Mode Operation	ENx = Open (float)		2.0				V
ENx Input High Voltage	VOUTx Enabled, Power Save Enabled				3.1		V
ENx Input Resistance	R Pull Up to VDDx		1.5				MΩ
	R Pull Down to RTN		1				MΩ
FBx Input Low Voltage				0.3			V
FBx Input High Voltage					VDDx -0.3		V
Power Good Output Low Voltage	R_{PGDx} = 10kΩ to VDDx					0.4	V
Gate Drivers							
Shoot-Thru Protection Delay(2)	DHx or DLx Rising		30				ns
DLx Pull-Down Resistance	DL Low		0.8			1.6	Ω
DLx Sink Current (2)	V_{DLx} = 2.5V		3.1				A
DLx Pull-Up Resistance	DLx High		2			4	Ω
DLx Source Current (2)	V_{DLx} = 2.5V		1.3				A
DHx Pull-Down Resistance	DHx Low, BSTx - LXx = 5V		2			4	Ω
DHx Pull-Up Resistance(3)	DHx High, BSTx - LXx = 5V		2			4	Ω
DHx Sink/Source Current (2)	V_{DHx} = 2.5V		1.3				A

Notes:
1) RTON = 1Meg.
2) Guaranteed by design.
3) Semtech's SmartDriver™ FET drive first pulls DH high with a pull-up resistance of 10Ω (typical) until LX = 1.5V (typical). At this point, an additional pull-up device is activated, reducing the resistance to 2Ω (typical). This negates the need for an external gate or boost resistor.

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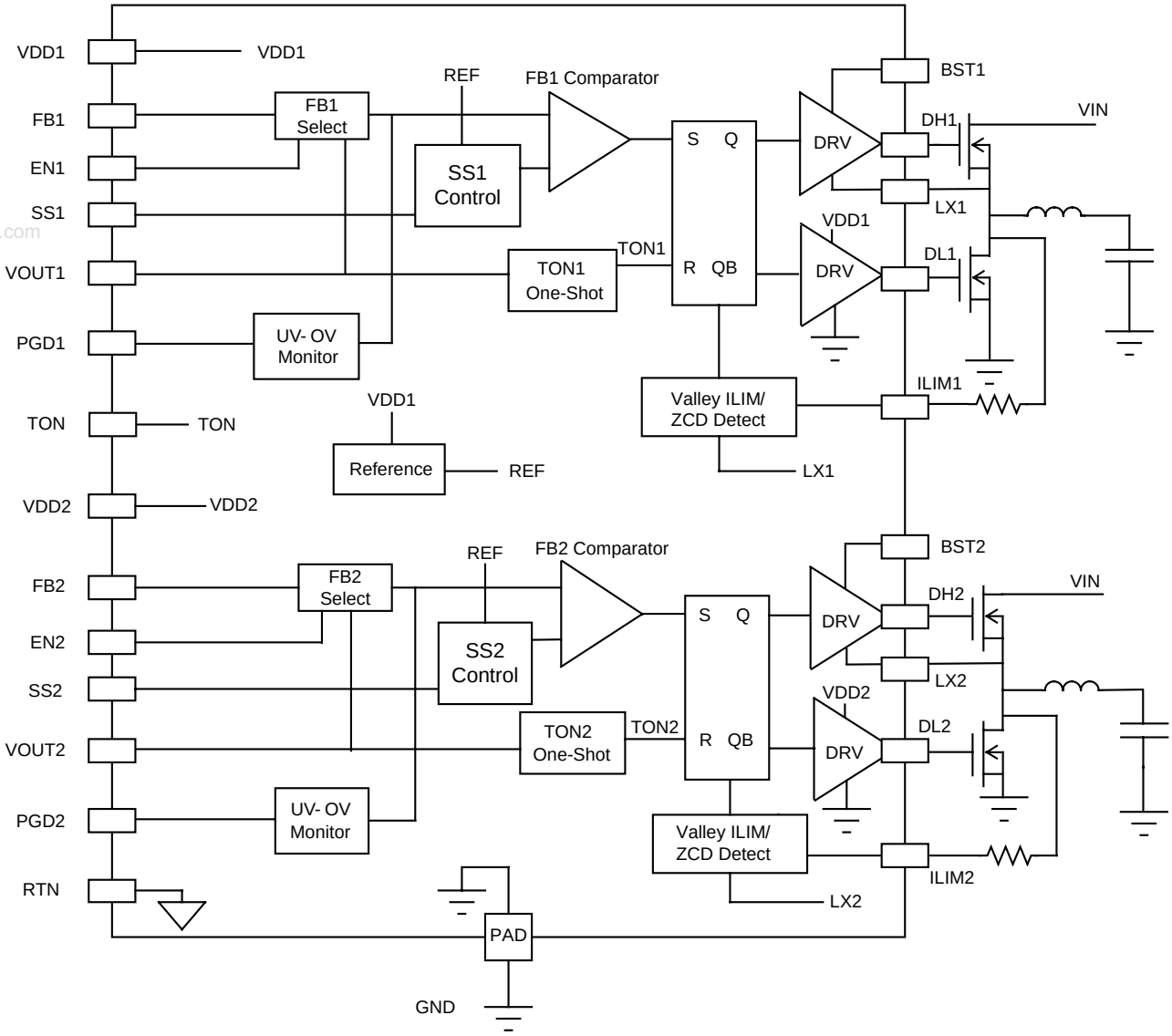
Pin Descriptions

Pin #	Pin Name	Pin Function
1	LX1	Switching (phase) node for VOUT1
2	BST1	Boost capacitor connection for VOUT1 high-side gate drive
3	VDD1	5V power input for VOUT1 analog circuits and gate drive outputs. Under-voltage lockout for the 5V supply is sensed on VDD1 only.
4	DL1	Gate drive output for the VOUT1 low-side external MOSFET
5	EN1	Enable input for VOUT1: ground to disable the VOUT1 switcher, leave open to enable VOUT1 switcher with power save disabled, connect to VDD1 to enable VOUT1 in power save mode
6	SS1	Soft-start and ramped shutdown input for VOUT1. For independent startup connect a capacitor to RTN. For tracked startup, connect to a capacitor or to a resistor divider connected to the other output; see the Voltage Tracking section.
7	VOUT1	Connect to the output capacitor of VOUT1 - used for On-Time generation and for VOUT1 regulation when FB1 is connected to VDD1 or RTN
8	FB1	Feedback input for VOUT1 - connect to an external resistor divider to adjust VOUT1, or connect to RTN or VDD1 to select internal feedback.
9	RTN	Analog return (ground) for both VOUT1 and VOUT2
10	TON	On-time adjust input - connect a resistor from VIN to TON to program the on-time - the on-time one-shot for VOUT1 is internally set at 20% greater than for VOUT2 to prevent frequency interaction between the two converters
11	FB2	Feedback input for VOUT2 - connect to an external resistor divider to adjust VOUT2 or connect to RTN or VDD2 to select internal feedback
12	VOUT2	Connect to the output capacitor of VOUT2 - used for On-Time generation and for VOUT2 regulation when FB2 is connected to VDD2 or RTN
13	SS2	Soft-start and ramped shutdown input for VOUT2. For independent startup connect a capacitor to RTN. For tracked startup, connect to a capacitor or to a resistor divider connected to the other output; see the Voltage Tracking section.
14	EN2	Enable input for VOUT2 - ground to disable the VOUT2 switcher - leave open to enable VOUT2 switcher with power save disabled - connect to VDD2 to enable VOUT2 in power save mode
15	DL2	Gate drive output for the VOUT2 low-side external MOSFET
16	VDD2	5V power input for VOUT2 analog circuits and gate drive outputs. VDD2 must connect to the same supply as VDD1.
17	BST2	Boost capacitor connection for VOUT2 high-side gate drive
18	LX2	Switching (phase) node for VOUT2
19	DH2	Gate drive output for the VOUT2 high-side external MOSFET
20	ILIM2	Current limit input for VOUT2 - connect through a resistor to the drain of the VOUT2 low-side MOSFET
21	PGD2	Open-drain Power Good output for VOUT2
22	PGD1	Open-drain Power Good output for VOUT1
23	ILIM1	Current limit input for VOUT1 - connect through a resistor to the drain of the VOUT1 low-side MOSFET
24	DH1	Gate drive output for the VOUT1 high-side external MOSFET
T	PAD	Power ground for VOUT1 and VOUT2 gate drivers and thermal pad for heatsinking

Block Diagram



SC416 Block Diagram

Applications Information

SC416 Synchronous Buck Controller

The SC416 is a dual synchronous controller which simplifies the task of designing a dual-output power supply with synchronized or tracking ramps for startup and shutdown.

VIN and +5V Bias Supplies

The SC416 requires an external +5V bias supply in addition to the VIN supply. If stand-alone capability is required, the +5V supply can be generated with an external linear regulator.

Pseudo-Fixed Frequency Constant On-Time PWM Controller

The PWM control method for each output is a constant-on-time, pseudo-fixed frequency PWM controller, see Figure 1. The ripple voltage seen across the output capacitor's ESR provides the PWM ramp signal. The on-time is determined by an internal one-shot whose period is proportional to output voltage and inversely proportional to input voltage. A separate one-shot sets the minimum off-time (typically 330ns). The two converters are designed to operate at different frequencies to reduce interaction; side2 frequency is set typically 20% higher than side1.

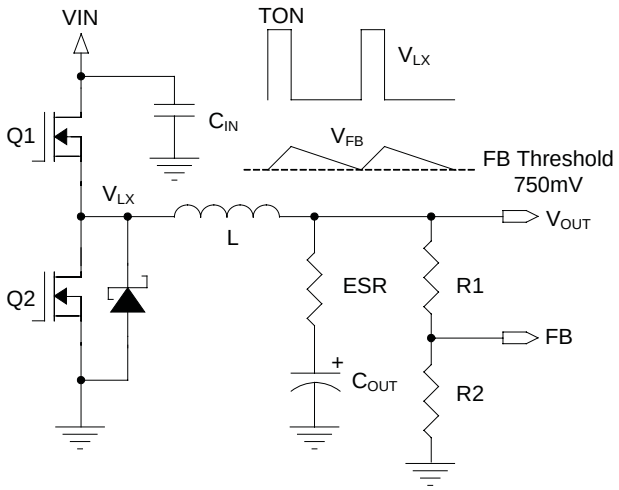


Figure 1

On-Time One-Shot (TON)

Each internal on-time one-shot comparator has two inputs. One input looks at the output voltage via the VOUT pin, while the other input samples the input voltage via the TON pin and converts it to a proportional current. This current charges an internal on-time capacitor. The TON on-time is the time required for this capacitor to charge from zero volts to VOUT, thereby making the on-time directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a fairly constant switching frequency with no clock generator.

The nominal frequency is set through an external resistor RTON connected between VIN and the TON pin. To minimize interaction between the two converters, side2 is set to operate at a slightly higher frequency. The general equations for the side1 and side2 on-times are:

$$TON1 = 3.30 \times (RTON + 37) \times (VOUT/VIN) + 35$$
$$TON2 = 2.75 \times (RTON + 37) \times (VOUT/VIN) + 35$$

(TON in nsec, RTON in kΩ)

Switch-Mode Operation

The switch-mode operation is explained below, and is identical for both sides except for the TON timing.

The output voltage is sensed at the FB pin and is compared to the internal 750mV reference. (The output voltage can also be sensed at the VOUT pin which uses an internal resistor divider, see VOUT Voltage Selection.) When the sensed voltage drops below 750mV, this triggers a single TON pulse, which is fed to the DH high-side driver. The DH pulse-width follows TON according to the TON equation, and after that time DH drives low to shut off the high-side MOSFET. After DH drives low, the DL output drives high to energize the low-side MOSFET.

Once high, DL has a minimum pulse width of typically 330nsec which is the minimum off-time. At the end of the minimum off-time, DL continues to stay high until

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Applications Information (continued)

one of the following occurs:

- The FB comparator input drops to the 750mV reference, as sensed through the FB pin or the VOUT pin
- The Zero Cross detector trips, if psave is active
- The Negative Current Limit detector trips

If DL drives low because FB has dropped to 750mV, then another DH on-time is started. This is normal operation at heavy load (fully synchronous operation with either DH or DL high except during transitions).

The Zero Cross detector monitors the voltage across the low-side MOSFET during the DL high time and detects when it reaches zero. If DL drives low because of the Zero Cross detector, and psave is active, then both DH and DL will remain low until FB drops to 750mV, at which point the next DH on-time will begin. If a Zero Cross is detected on eight consecutive cycles, then for each subsequent switching cycle DL will shut off when the Zero Cross detector trips; see the Psave Operation section. When this occurs, both DH and DL will stay low until FB drops to 750mV, which will begin the next DH on-time. This is normal operation at light load, see the Psave Operation section.

The Negative Current Limit detector trips when the drain voltage at the low-side MOSFET reaches +80mV, indicating that a large negative current flows through the inductor from VOUT. When this occurs, DL drives low. Both DH and DL will then stay low until FB drops to 750mV, which will begin the next DH on-time. Tripping Negative Current Limit is rare.

To help reduce noise interaction between sides, the rising edge of each DH driver is inhibited momentarily if the other side is switching. For example, if side1 is performing a DH or DL transition (up or down), then side2's DH driver is held off for roughly 30nsec to allow side1 to finish switching.

VOUT Voltage Selection

Output voltage is regulated by comparing VOUT as seen through a resistor divider to the internal 750mV reference, see Figure 2. Each output can be adjusted to a voltage between 0.75 – 5.25V. The output voltage is set by the equation:

$$V_{OUT} = 0.75 \bullet (1 + R1/R2)$$

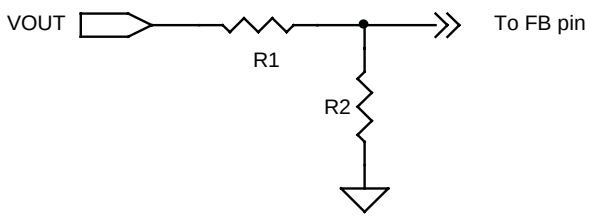


Figure 2

Note: the parallel resistance of R1 and R2 should not be less than 2kΩ. Using a smaller resistance can cause the IC to default to the internal preset output voltages shown below.

There are fixed output voltages accessible through each FB pin. If the FB pin is connected to either RTN or +5V, then the IC will ignore the FB pin and instead regulate the output voltage using the VOUT pin which is connected to internal resistors. The voltage selections available are as shown:

FB Internal Voltage Selection		
	FBx = RTN	FBx = +5V
Side1	1.5V	1.8V
Side2	1.05V	1.25V

Note that each FB input operates independently.

Applications Information (continued)

Enable/Psave Inputs

Each converter has a separate Enable pin. Each EN input operates as follows:

EN = GND. This turns the converter off.

EN = open (float). This turns the converter on with psave mode disabled (continuous conduction mode). In this case, the EN pin will float to approximately 2V due to an internal 1.5Meg/1Meg resistor divider from +5V to ground.

EN = high (3.1V min). This turns the converter on with psave mode enabled. At light loads, the converter will operate in psave mode.

Note that the two EN pins are separate, so each output can be disabled or operated with or without psave independently.

For tracking operation during startup, the two EN pins are typically tied together; see the Voltage Tracking section.

If both EN1 and EN2 are grounded, the device is placed into the lowest-power state, drawing typically 7µA from the +5V supply.

Psave Operation

Each output provides automatic psave operation at light loads if the ENx pin is set high. The internal Zero-Cross comparator looks for inductor current (via the voltage across the lower MOSFET) to fall to zero on eight consecutive switching cycles. Once observed, the controller enters psave mode and turns off the low-side MOSFET on each subsequent cycle when the current crosses zero. To add hysteresis, the on-time is also increased by 25% in Psave, for that converter only; it does not affect the other converter's on-time. The efficiency improvement at light loads more than offsets the disadvantage of slightly higher output ripple. If the inductor current does not cross zero on any switching cycle, the controller immediately exits Psave. Once Psave is exited, it requires 8 switching cycles at light load to re-enter psave. Since the controller counts zero crossings, the converter can sink current as long as the current does not cross zero on eight consecutive cycles. This allows the output voltage to recover quickly in response to negative load steps.

When operating in Psave mode at light loads, the LX waveform will not have the typical square wave shape seen when operating in continuous conduction mode. Shortly after DL drives low, and both MOSFETs are off, the LX voltage will show ringing. This ringing is caused by the LC circuit formed by the inductor and device capacitance of the MOSFETs and low-side diode. When the low-side MOSFET turns off the inductor current falls toward zero. When it reaches zero, the inductance and MOSFET capacitances will tend to ring freely. This is normal Psave operation as shown in Figure 3.

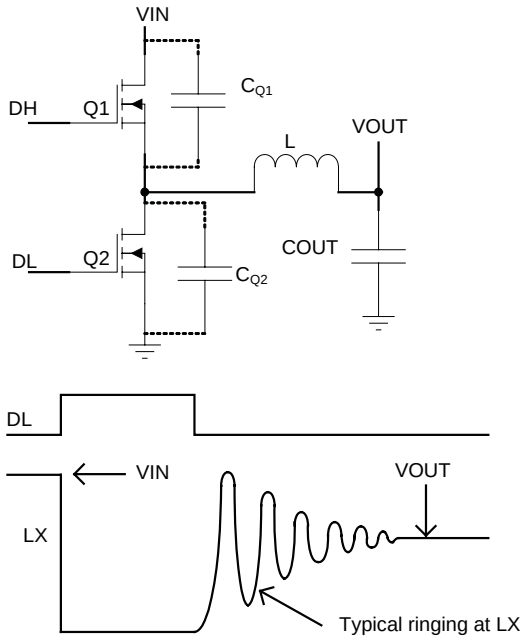


Figure 3

Applications Information (continued)

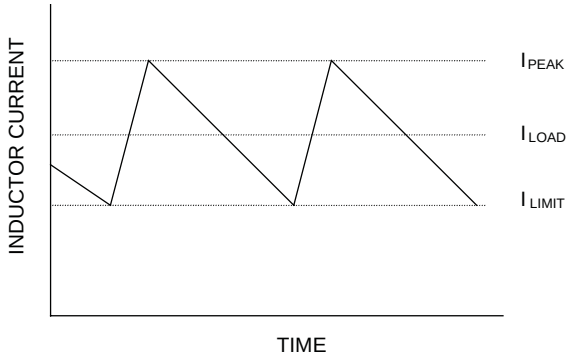
Smart Psave Protection

In some applications, circuits connected to VOUT can leak current from a higher voltage and thereby cause VOUT to slowly rise and reach the OVP threshold, causing a hard shutdown; the SC416 uses Smart Psave to prevent this. When the output voltage exceeds 8% above nominal (810mV at FB), that converter then exits Psave (if already active), and DL drives high to energize the low-side MOSFET. This will draw current from VOUT via the inductor causing VOUT to fall. When FB drops to the 750mV trip point, a normal TON switching cycle begins. This method cycles energy from VOUT back to VIN and prevents a hard OVP shutdown, and also minimizes operating power by avoiding continuous conduction-mode operation. If a light load is present, DH/DL switching continues for 8 consecutive cycles and then the IC returns to Psave mode to reduce operating power.

Current Limit

For current limiting, the RDSON of the lower MOSFET can be used as a current sensing element, or a sense resistor at the lower MOSFET source can be used if greater accuracy is needed. RDSON sensing is more efficient and less expensive. In both cases, the RILIM resistor sets the overcurrent threshold. RILIM connects from the ILIM pin to either the lower MOSFET drain (for RDSON sensing) or the high side of the current-sense resistor. RILIM connects to a 10µA current source from the ILIM pin which turns on when the low-side MOSFET is on (DL is high). If the voltage drop across the sense resistor or low-side MOSFET exceeds the voltage across RILIM, then the voltage at the ILIM pin will be negative or below GND, and current limit will activate. The high-side MOSFET is not allowed to turn on until the voltage drop across the sense resistor or MOSFET falls below the voltage across the RILIM resistor (ILIM pin reaches GND). If the overload at the output continues, the DH pulses will get farther apart, and the output voltage will fall. Eventually the output will fall enough to cause FB to drop to 525mV, activating the under-voltage protection and shutting down the converter.

The current sensing scheme actually regulates the inductor valley current, (see Figure 4). This means that if the current limit is set to 10A, the peak current through the inductor would be 10A plus the peak ripple current, and the average current through the inductor would be 10A plus ½ the peak-to-peak ripple current.



Valley Current Limit

Figure 4

The RDSON sensing circuit is shown in Figure 5 with RILIM = R1 and RDSON of Q2.

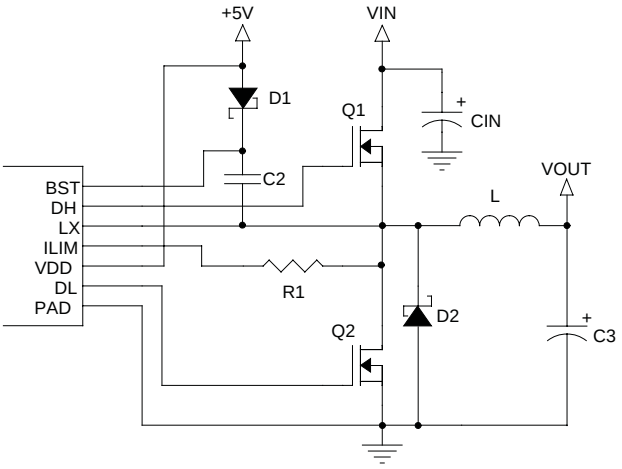


Figure 5

The resistor sensing circuit with RILIM = R1 and RSENSE = R4 is shown in Figure 6.

Applications Information (continued)

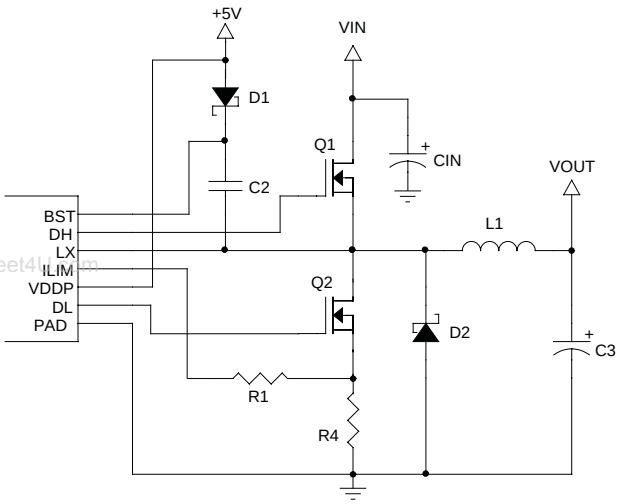


Figure 6

The following over-current equation can be used for both RDSON or resistive sensing. For RDSON sensing, the MOSFET RDSON rating is used for the value of RSENSE.

$$ILOC(Valley) = 10\mu A \times RILIM / RSENSE$$

Power Good Output

Each output provides a power good (PGD) output, which is an open-drain output requiring a pull-up resistor. When the output voltage as sensed at FB is -9% from the 750mV reference (682mV), PGD is pulled low. It is held low until the output voltage returns above -9% of nominal; the falling edge of VOUT does not latch PGD. PGD is held low during start-up and will not be allowed to transition high until soft-start is completed, when SS reaches 750mV. There is a 5µsec delay built into the PGD circuit to prevent false transitions.

PGD also transitions low if the FB pin exceeds +20% of nominal (900mV), which is also the over-voltage shutdown point.

Output Over-Voltage Protection (OVP)

When FB exceeds 20% of nominal (900mV), DL latches high and the low-side MOSFET is turned on. DL stays high and the output stays off until the EN/PSV input is toggled or VDD is recycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGD is also held low after an OVP.

Output Under-Voltage Protection (UVP)

When FB falls 30% below nominal (to 525mV) for eight consecutive clock cycles, the output is shut off; the DL/DH drives are pulled low to tri-state the MOSFETs, and the converter stays off until its EN/PSV input is toggled or the +5V supply at VDD1 supply is recycled. The other output remains on during a UVP event.

POR and UVLO

Under-voltage lockout circuitry (UVLO) inhibits switching and tri-states all DH/DL drivers until the +5V supply at VDD1 rises above 4.4V. An internal power-on reset (POR) occurs when VDD1 exceeds 4.4V, which resets the fault latches and quickly discharges the soft-start capacitors to prepare the PWM for startup switching. At this time the SC416 will exit UVLO and begin the startup cycle.

Startup Sequence

The startup sequence for each output relies on an external ramp at the SS pin. During startup, the FB comparator uses the SS ramp voltage as the reference until SS reaches 750mV, at which point the FB comparator switches over to the internal 750mV reference. The external ramp is typically created by connecting a capacitor to the SS pin, which will be charged by a constant current. Or, the SS pin can be connected to an external ramp provided by the other output's ramp-up as seen through a resistor divider. See the Voltage Tracking section.

Before starting, with EN low, the SS pin is internally tied to GND through 4kΩ. When EN is released, SS is briefly pulled to GND through 16 ohms to discharge the SS capacitance. Then the resistances are removed, startup begins, and a 5µA source current flows out of the SS pin.

Applications Information (continued)

If an external capacitor is connected to SS, with no other components, then the 5uA current into the capacitor creates a linear voltage ramp. The internal FB comparator tracks this SS ramp, which forces VOUT to track the SS ramp. The time in msec needed for the SS ramp to reach the 750mV reference is:

$$T_{START} = Css \times 150$$

(T_{START} in µsec, Css in nF)

At the end of this time, the SS pin has reached 750mV and the output voltage is at its nominal value. The FB comparator then switches over to the internal 750mV REF, and the SS pin is thereafter ignored. The 5µA current source remains on, so the Css capacitor continues to charge up to +5V.

The SS pin can be connected to a capacitor to provide a programmable ramp, or connected to a resistor divider from the other output to provide a synchronized startup, see the Voltage Tracking section.

The startup waveforms when using a capacitor for the voltage ramp are shown in Figure 7.

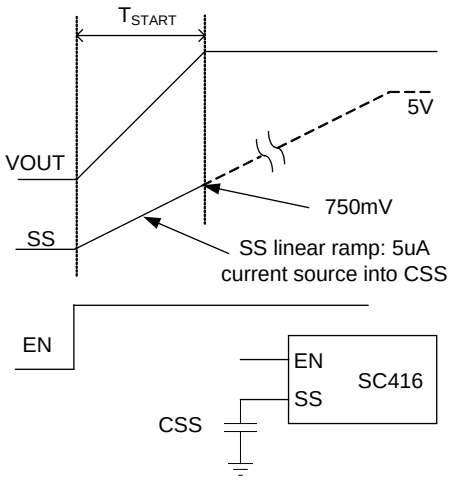


Figure 7

Shutdown Sequence

Each output has a controlled shutdown. The ramp-down sequence is optimized for use with an external SS capacitor. When the EN pin is set low, psave mode is disabled and the shutdown sequence begins. The SS pin stops sourcing 5uA, and an internal 4K pulldown resistor is enabled along with a 5uA current sink. The 4K resistor helps discharge of the SS capacitor (if used), which was previously charged to +5V by the 5uA current source. The SS capacitor discharges quickly; when the SS voltage reaches 810mV, the 4K resistor is released, leaving the 5µA current sink on (current into the SS pin), which discharges the SS capacitor from 810mV to 750mV at a slower rate.

When the SS voltage reaches 750mV, the ramp-down at VOUT begins. With SS at 750mV, the FB comparator ignores the internal 750mV reference and instead uses the SS ramp-down to regulate VOUT. As the SS pin ramps down from 750mV due to the current sink, VOUT follows the SS pin in a linear ramp-down.

Note that psave is disabled during the shutdown cycle to allow VOUT to actively track the SS ramp-down, even with no load.

The ramp-down continues until VOUT falls to 300mV as sensed at the VOUT pin, not the FB pin. At this point the switching is disabled, the DH and DL drivers are set low (both MOSFETs off), and an internal 16 ohm pulldown connects to the VOUT pin to finish soft-discharge of the output.

Applications Information (continued)

The general shutdown waveforms are shown in Figure 8.

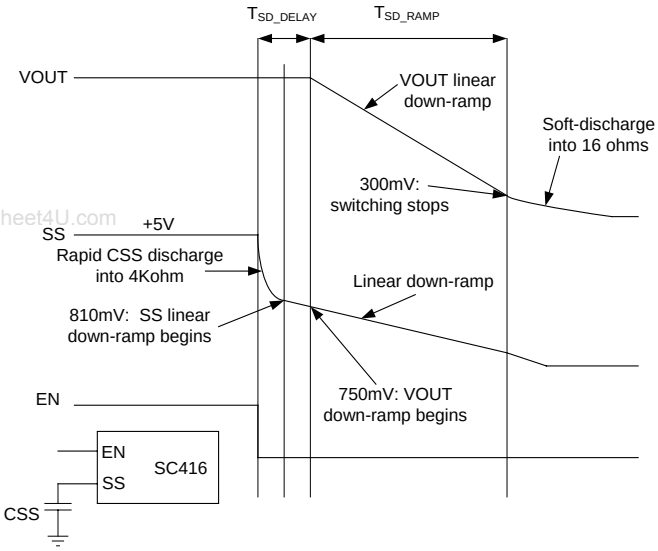


Figure 8

Note that due to the discharging of CSS from +5V to 750mV, there is a small delay between EN going low and VOUT beginning to ramp down. The delay is given by the equation:

$$T_{SD\_DELAY} = Css \times 19$$

(T_{SD_DELAY} in µsec, Css in nF)

After this delay, the time for the output to ramp down to the switch-off point of 300mV is given by:

$$T_{SD\_RAMP} = Css \times 150 \bullet (1 - 300mV/VOUT)$$

(T_{SD_RAMP} in µsec, Css in nF)

Once the output reaches 300mV, the shutdown sequence is complete. DH and DH stop switching, the internal 16 ohm discharge pulldown at VOUT is energized, and that side will go to the lowest-power state.

Voltage Tracking

The SC416 provides voltage tracking during both start-up and shutdown. The use of the SS pins determines the type of tracking. The two most common tracking schemes are proportional and coincident tracking.

Proportional Tracking (FB tracking)

Proportional tracking causes the output waveforms to have the same startup and shutdown ramp time as shown in Figure 9.

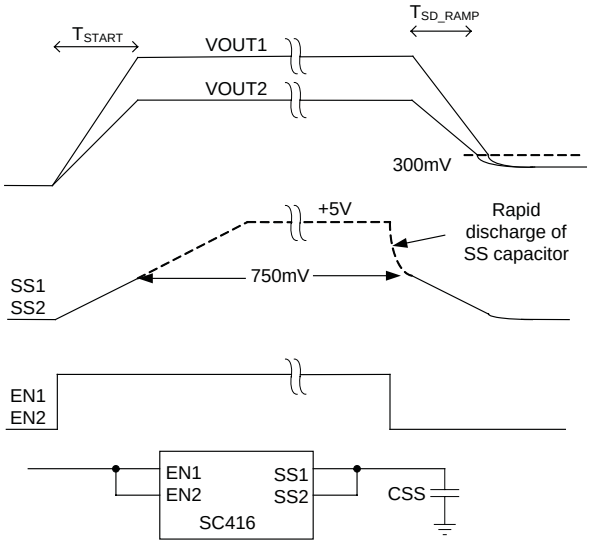


Figure 9

For proportional tracking, the two SS pins are tied together to share the same voltage ramp. The two EN pins must also be tied together. Since the SS pins are tied together, the startup and shutdown ramps for each side will track the same signal. Note that during startup and shutdown, the FB pins for each side will track the same SS signal; this method can also be called FB tracking.

Startup for proportional tracking (FB tracking) is as follows. When both EN pins are set high simultaneously, each SS pin sources 5uA. By connecting the SS pins together, the startup ramp rates for both FB1 and FB2 are forced to be the same. Since the total current source is

Applications Information (continued)

10µA instead of 5µA, the CSS capacitor must be twice as large as in the independent case. It is acceptable to use only one SS capacitor for both SS pins, and the startup time follows the equation:

$$T_{START} = Css \times 75$$

(T_{START} in µsec, Css in nF)

Once the SS pins reach 750mV, each FB comparator switches over to the internal 750mV reference, and the SS pin is ignored. CSS will continue to charge to +5V, just as in the independent case.

Shutdown for proportional tracking is similar to the independent case. Both EN pins are simultaneously pulled to GND to start the shutdown sequence. When the EN pins are set low, the two SS 5µA current sources are disabled, and the internal 4k pull-down of each SS pin is energized. This begins a quick discharge of CSS from the initial +5V starting point.

When CSS discharges down to 810mV, each 4k resistor is removed and each SS 5µA current sink is energized, to cause a more gradual ramp down to 750mV. When SS reaches 750mV, each FB comparator ignores the internal 750mV reference and uses the falling SS ramp as the reference. This causes both FB pins to fall at a constant linear rate. This in turn causes both VOUTs to fall linearly. This continues for each VOUT until it reaches 300mV, at which point all switching for that output will stop.

Note that the output ramp-down is controlled only until the point where the output voltage (as sensed at the VOUT pin, not the FB pin) reaches 300mV, and then switching stops. Also note that the two output voltages may not reach 300mV at the same time. With proportional tracking, the lower voltage will reach 300mV first; at that point, the lower voltage will enter soft-discharge into 16 ohms, but the other output will continue on the SS ramp-down until it also reaches 300mV. For the majority of applications this is acceptable since 300mV is typically too small to cause a voltage-differential problem for the load.

Coincident Tracking (VOUT tracking)

Coincident tracking has the lower output actively matching the higher output during startup and shutdown.

During startup, the two voltages track identically until the lower VOUT reaches its nominal point and then remains at that point. The higher voltage continues on a linear ramp until reaching its final value.

During shutdown, the higher voltage initially starts to fall while the lower voltage stays in regulation. When the higher voltage has dropped to the same level as the lower voltage, the lower voltage joins the ramp-down, and both voltages fall at the same rate. When the outputs reach 300mV, switching stops and the outputs will soft-discharge into their VOUT pins.

The waveforms and schematic for coincident tracking are shown in Figure 10.

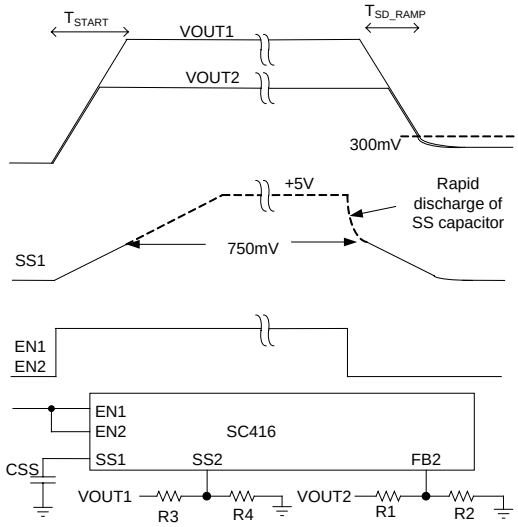


Figure 10

Note that both EN pins are tied together. For coincident tracking, the higher output voltage must act as the control, and the lower output must be the follower. Either side can act as controller or follower. In this case, VOUT1 is the higher output voltage. When the EN pins are set

Applications Information (continued)

high, both outputs start switching. SS1 is connected to a capacitor and therefore VOUT1 will follow the normal (independent) startup and shutdown operation.

SS2 does not have the typical capacitor connection; instead SS2 connects to VOUT1 through resistor divider R3/R4, which forces the SS2 voltage to be proportional to VOUT1. As VOUT1 rises during startup, SS2 also rises, and the FB2 comparator will force VOUT2 to track SS2 until SS2 reaches 750mV.

Note that FB2 sets the output voltage for VOUT2 through R1/R2. By setting the same ratio for R3/R4 as R1/R2, VOUT2 is forced to track VOUT1. This tracking continues until FB2 reaches 750mV, at which point VOUT2 ignores the SS2 ramp and switches over to the internal 750mV reference. SS2 will continue to rise above 750mV since it is connected to VOUT2 which continues to rise to its nominal value.

Note that during this time the SS2 pin will source 5uA, as if it were charging a capacitor. This current will flow through into R3/R4 and create an offset voltage at SS2. The full equation for SS2 voltage is:

$$VSS2 = VOUT1 \times (R4 / (R3 + R4) + 5\mu A \times (R3||R4)$$

The term for the SS2 offset is $(5\mu A \times R3||R4)$. When tracking VOUT1 during startup, SS2 will be slightly higher than the ideal value due to this offset term. This offset at SS2 is tracked by FB2. Because of the FB2 resistor divider, this causes a consequently higher offset at VOUT2. The net effect is that VOUT2 will be slightly higher than VOUT1 during startup tracking. The net offset is given by the following equation, where R5/R6 are the top and bottom resistor values used for the FB2 resistor divider:

$$VOUT1 - VOUT2 = 5\mu A \times (R3||R4) \times (1 + R5/R6)$$

Since the ratio of R5/R6 is dictated by the output voltage, the way to minimize the offset is to reduce R3 and R4. It is recommended to set the R3/R4 parallel combination to 1kΩ max, which limits the SS2 offset to 5mV.

For shutdown, both EN pins are pulled low to start the shutdown sequence. The higher output falls first (VOUT1 in this case) as described in the independent case. The SS2 pin also falls as VOUT1 falls. When SS2 has reached 750mV, the ramp-down of VOUT2 begins. The FB2 comparator switches over to the SS2 pin and tracks SS2 as it ramps down. SS2's ramp-down is in turn controlled by the ramp-down of VOUT1.

Note that during the initial time when both EN pins pulled low, the internal 4kΩ pulldown on SS2 is energized, along with the 5uA current sink. The connecting of the 4k pulldown affects the SS2 voltage, causing it to be significantly lower than predicted by the R3/R4 divider. If the SS2 voltage suddenly shoots below 750mV, this will cause the FB2 comparator to ignore the internal 750mV reference and switch over to the SS2 voltage. Also, the 4k resistor is released, which causes the SS2 voltage to go back above 750mV, since SS2 will now track VOUT1 through R3/R4. This can create an unwanted overshoot on VOUT2. This is easily prevented by placing a 10nF capacitor across R4, to prevent sudden changing of the SS2 voltage.

Modified Coincident Tracking (VOUT Proportional Tracking)

A modification of coincident tracking is to set R3/R4 (SS2 resistor divider) to a ratio other than R1/R2 (FB1 resistor divider). VOUT2 will still track SS2 during startup and shutdown, but VOUT2 can be made to ramp either quicker or slower than VOUT1, based on the R3/R4 ratio, see Figure 11.

Applications Information (continued)

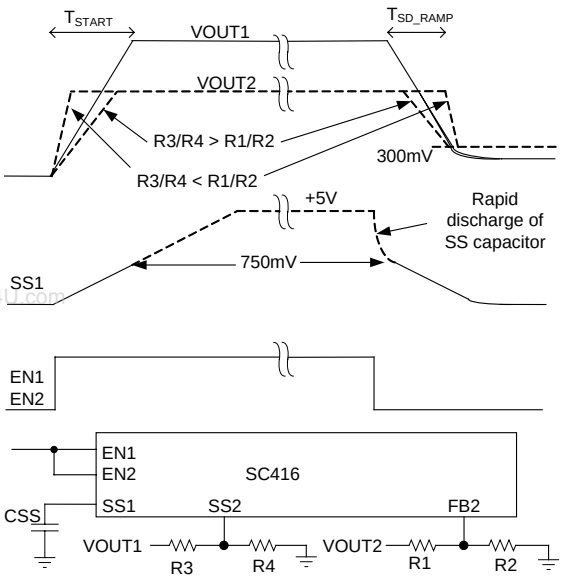


Figure 11

Note that R3/R4 must never exceed the FB resistor ratio for VOUT1. If this were the case, SS2 cannot exceed 750mV, and the FB2 comparator would never switch over to the internal 750mV reference: VOUT2 would not complete its startup cycle and would not reach the nominal regulation point. To prevent this it is recommended to set R3/R4 such that SS2 is greater than 850mV when VOUT1 is at the nominal point.

MOSFET Gate Drivers

The DH and DL drivers are optimized to drive moderate high-side and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off; another circuit monitors the DH output and prevents the low-side MOSFET from turning on until DH is fully off.

Note: be sure there is low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.

SmartDrive™

Each side uses Semtech's proprietary SmartDrive to reduce switching noise. The DH drivers will turn on the high-side MOSFET at a lower rate initially, allowing a softer, smooth turn-off of the low-side diode. Once the diode is off, the SmartDrive circuit automatically drives the high-side MOSFET on at a rapid rate. This technique reduces switching less while maintaining high efficiency, and also avoids the need for snubbers or series resistors in the gate drive.

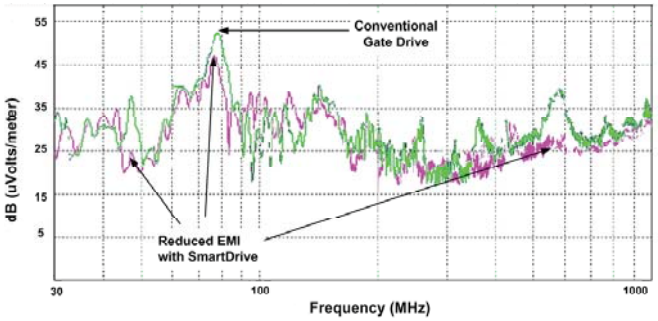


Figure 12

Design Procedure

Prior to designing a switch mode supply, the input voltage, load current, and switching frequency must be specified. The maximum input voltage (VINMAX) is determined by the highest AC adaptor voltage, and the minimum input voltage (VINMIN) is determined by the lowest supply voltage after accounting for voltage drops due to connectors, fuses, and switches.

In general, four parameters are needed to define the design:

1. Nominal output voltage (VOUT)
2. Static or DC output tolerance
3. Transient response
4. Maximum load current (IOUT)

Applications Information (continued)

There are two values of load current to consider: continuous load current and peak load current. Continuous load current is concerned with thermal stresses which drive the selection of input capacitors, MOSFETs and diodes. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors and design of the current limit circuit.

Design example: Side1 will be used.

VIN = 10V min, 20V max
VOUT1 = 1.8V +/- 4%
Load = 10A maximum

Inductor Selection

Low inductor values result in smaller size but create higher ripple current. Higher inductor values will reduce the ripple current but are larger and more costly. Because wire resistance varies widely for different inductors and because magnetic core losses vary widely with operating conditions, it is often difficult to choose which inductor will optimize efficiency. The general rule is that higher inductor values have better efficiency at light loads due to lower core losses and lower peak currents, but at high load the smaller inductors are better because of lower resistance. The inductor selection is generally based on the ripple current which is typically set between 20% to 50% of the maximum load current. Cost, size, output ripple and efficiency all play a part in the selection process.

The first step is to select the switching frequency. In this case VOUT1 will be used at a nominal 270kHz.

For 15V input and 1.8V output, the typical on-time should be:

$$TONtyp = VOUT/VIN/Frequency$$
$$TONtyp = 444nsec.$$

The timing resistor RTON is selected to provide TONtyp:

$$RTON = (TONtyp - 35) \times (VIN / (3.3 \times VOUT) - 37$$
$$RTON = 976K.$$

We will use RTON = 1Meg.

Note that side2 will run typically 20% faster than side1, in this case 320kHz.

During the DH on-time, voltage across the inductor is (VIN - VOUT). To determine the inductance, the ripple current must be defined. Smaller ripple current will give smaller output ripple and but will lead to larger inductors. The ripple current will also set the boundary for Psave operation. The switcher will typically enter Psave operation when the load current decreases to ½ of the ripple current; (i.e. if ripple current is 4A then Psave operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then Psave will occur for loads less than 20% of maximum current).

The equation for inductance is:

$$L = (VIN - VOUT) \times TON / I_{RIPPLE}$$

Use the maximum value for VIN, and for TON use the value associated with maximum VIN, and that side's TON using the RTON value selected. For selecting the inductor, we start with the highest VOUT setting and a maximum ripple current of 4A.

TON1 = 343 nsec at 20VIN, 1.8VOUT

$$L = (20V - 1.8V) \times 343\ nsec / 4A = 1.56\mu H$$

We will use 1.5µH which will slightly increase the maximum I_{RIPPLE} to 4.2A.

Note: the inductor must be rated for the maximum DC load current plus ½ of the ripple current.

The minimum ripple current is also calculated. This occurs when VIN is at the minimum value of 10V.

$$TON_{VINMIN} = 3.3 \times (RTON + 37) \times (VOUT/VIN) + 35$$
$$TON_{VINMIN} = 651nsec$$

$$I_{RIPPLE} = (VIN - VOUT) \times TON / L$$
$$I_{RIPPLE\_VINMIN} = (10 - 1.8) \times 651nsec / 1.5\mu H = 3.55A$$

SEMTECH

Applications Information (continued)

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The ESR requirement is driven by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple, plus ½ of the peak-to-peak ripple. Changing the ripple voltage will lead to a change in DC output voltage.

The design goal is +/-4% output regulation. The internal 750mV reference tolerance is 1%, and assuming 1% tolerance for the FB resistor divider, this allows 2% tolerance due to VOUT ripple. Since this 2% error comes from ½ of the ripple voltage, the allowable ripple is 4%, or 72mV for a 1.8V output. Although this is acceptable from a regulation standpoint, 72mV ripple is high for a 1.8V output and therefore more realistic ripple value of 36mV will be used (2% of VOUT).

The maximum ripple current of 4.2A creates a ripple voltage across the ESR. The maximum ESR value allowed would create 36mV ripple:

$$ESR_{MAX} = V_{RIPPLE}/I_{RIPPLEMAX} = 36mV / 4.2A$$
$$ESR_{MAX} = 8.6\ m\Omega$$

While the ESR is chosen to meet ripple requirements, the output capacitance (µF) is typically chosen based on transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, defines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in a very small time), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the equation:

$$COUT_{MIN} = \frac{L \times (IOUT + 1/2 \times I_{RIPPLEMAX})^2}{(V_{PEAK}^2 - VOUT^2)}$$

With a peak voltage VPEAK of 1.98V (180mV or 10% rise above 1.8V upon load release), the required capacitance is:

$$COUT_{MIN} = \frac{1.5\mu H \times (10 + 1/2 \times 4.2)^2}{(1.98^2 - 1.8^2)}$$

$$COUT_{MIN} = 323\mu F$$

The previous requirements (323µF, 6.4mΩ) will be met using a single 330µF 6mΩ device.

Note that output voltage ripple is often higher than expected due to the ESL (inductance) of the capacitor. See the FB/VOUT Ripple section.

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 750mV reference, the DL output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately -VOUT. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not much faster than the di/dt in the inductor, then the inductor current can track the changing load current, and there will be relatively less overshoot from a load release. The following can be used to calculate the needed capacitance for a given dILOAD/dt.

Peak inductor current:

$$IL_{PEAK} = ILOAD_{MAX} + 1/2 \times I_{RIPPLEMAX}$$
$$IL_{PEAK} = 10 + 1/2 \times 4.2 = 12.1A$$

Rate of change of Load current = dILOAD/dt

IMAX = maximum DC load current = 10A

$$COUT = \frac{IL_{PEAK} \times (L \times IL_{PEAK} / V_{OUT} - IMAX/(dILOAD/dt))}{2 \times (V_{PEAK} - VOUT)}$$

Example: Load dI/dt = 2.5A/µsec

Applications Information (continued)

This would cause the output current to move from 10A to zero in 4µsec.

$$COUT = \frac{12.1 \times (1.5\mu H \times 12.1 / 1.8 - 10 / (2.5A/1\mu sec))}{2 \times (1.98 - 1.8)}$$

$$COUT = 204\mu F$$

Note that 204µF is less than the 323uF needed to meet the harder (instantaneous) transient load release.

Stability Considerations

Unstable operation shows up in two related but distinctly different ways: fast-feedback loop instability due to insufficient ESR and double-pulsing.

Loop instability can cause oscillations at the output as a response to line or load transients. These oscillations can trip the over-voltage protection latch or cause the output voltage to fall below the tolerance limit. The best way for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Over one cycle of ringing after the initial step is a sign that the ESR should be increased.

SC416 ESR Requirements

The on-time control used in the SC416 regulates the valley of the output ripple voltage. This ripple voltage consists of a term generated by the ESR of the output capacitor and a term based on the capacitance charging and discharging during the switching cycle. A minimum ESR is required to generate the required ripple voltage for regulation. For most applications the minimum ESR ripple voltage is dominated by PCB layout and the properties of the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than one-third the switching frequency. The formula for minimum ESR is:

$$ESRMIN = 3 / (2 \times \pi \times COUT \times FREQ)$$

For applications using ceramic output capacitors, the ESR is generally too small to meet the above criteria. In these cases it is possible to create a ripple voltage ramp that mimics the ESR ramp. This virtual ESR ramp is created by integrating the voltage across the inductor, and coupling the signal into the FB pin as shown in Figure 13.

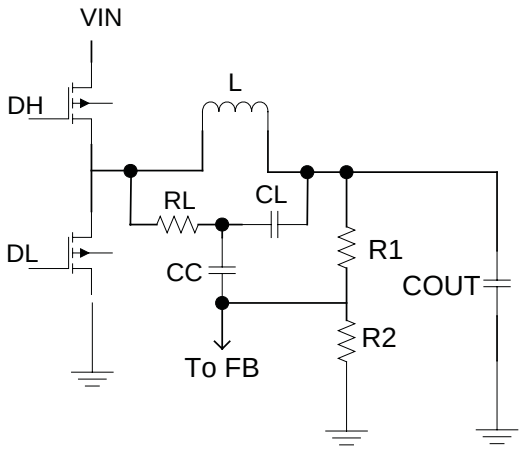


Figure 13

Double-pulsing

Double-pulsing occurs because the ripple waveform seen at the FB pin is either too small, or because the FB and VOUT ripple waveforms are very noisy and prone to cause premature triggering of the FB comparator. Both are discussed below.

Increasing FB Ripple

If the ripple waveform at FB is too small, the FB waveform will be susceptible to switching noise. Note that under normal conditions the FB voltage is within 10-20mV of the 750mV trip point. Noise can couple into the FB point from either side1 or side1, or from an external circuit. This causes the FB comparator to trigger too quickly after the 330ns minimum off-time has expired. Double-pulsing will result in higher ripple voltage at the output but in most cases is harmless.

A way to remedy this is to couple more ripple into FB from VOUT. Note that the feedback resistor divider attenuates the FB ripple. This can be compensated by placing a small capacitor in parallel with the top resistor, which effectively increases the ripple that appears at FB.

Applications Information (continued)

The schematic with added capacitor C is shown below.

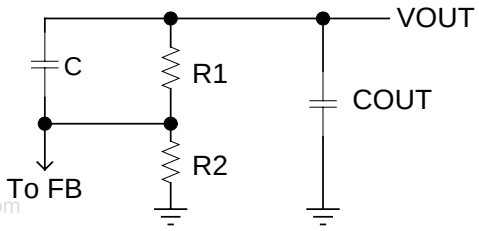


Figure 14

This capacitor should be left out until confirmation that double-pulsing exists. It is best to leave a spot on the PCB in case it is needed.

FB/VOUT Ripple

Because the constant on-time control method triggers a DH pulse whenever the FB waveform reaches the 750mV trip point, it is important that the VOUT and FB ripple waveforms are well shaped. This waveform will depend on the output capacitors.

The idealized case for the output filter has an inductor and a capacitor COUT with series ESR. The voltage ripple due to charging and discharging COUT is typically much smaller than the ripple voltage due to ESR, so the overall ripple waveform is generally determined by ESR only. The result is a well-defined sawtooth, see Figure 15.

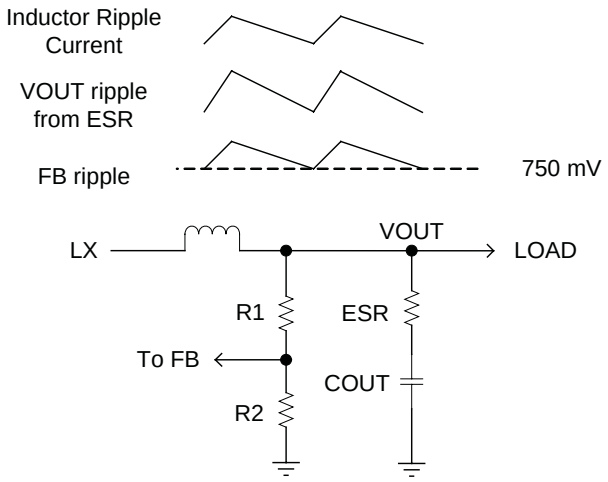


Figure15

In many applications, the output capacitor also has some series inductance (ESL), and this can have a large effect on ripple. The ripple current creates voltage across the ESL; this is a square wave similar to the LX waveform. The result is shown below. Note the fast rising and falling edges created by the ESL.

Applications Information (continued)

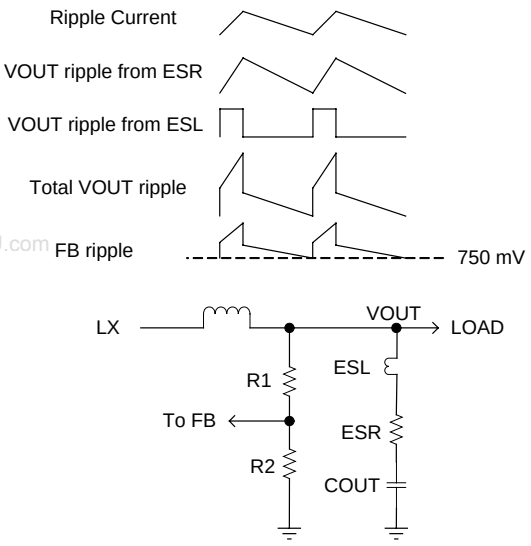


Figure 16

Note also that the effect of ESL becomes increasingly more noticeable with lower VOUT and higher VIN. The square wave due to ESL is basically the same square wave seen at the LX node, scaled down by the ratio of the output inductor and the ESL. As VOUT gets lower, the output inductor gets smaller, and this directly increases the ESL square wave. Moreover, lower output voltages have tighter ripple requirements, so there is generally less room available for pk-pk ripple.

In addition to the ESL, most applications also have a small capacitor in parallel with COUT; this is typically a small ceramic capacitor intended to absorb high frequency noise not filtered by the output capacitor, as shown by CB in Figure 17.

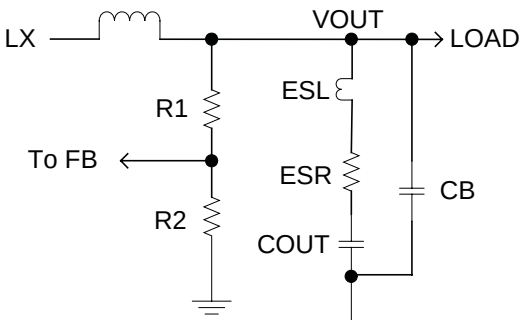


Figure 17

This capacitor CB can have a large effect on the ripple waveform. The switch transitions are fast, typically 10-30nsec. At this high speed, the output capacitor (COUT) impedance is dominated by ESL, which is in parallel with CB. The effective circuit is a parallel L-C filter. The choice of CB can have significant effect on the ripple waveform. This parallel LC circuit can lead to ringing at VOUT. Since the FB waveform goes below the 750mV threshold soon after the DH pulse is finished, there is the potential for double-pulsing; the ringing can cause the FB waveform to go below the trip point too early.

Applications Information (continued)

Figure 18 shows examples of this.

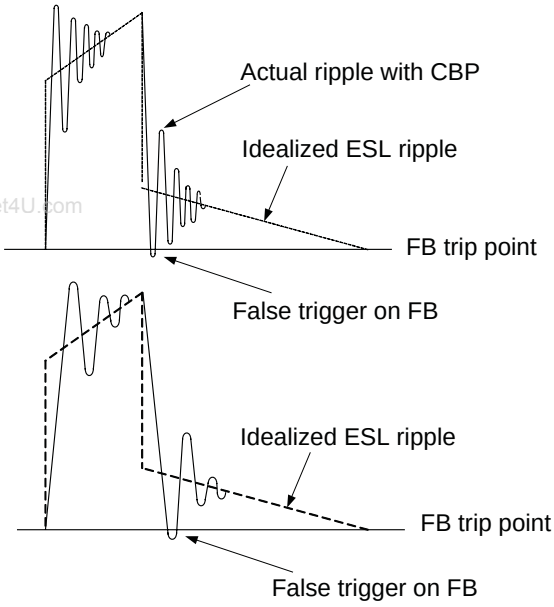


Figure 18

There are two ways to deal with this issue. One is to use a larger ceramic capacitor, typically 2.2–10µF, which significantly smooths the ripple waveform as shown in Figure 19.

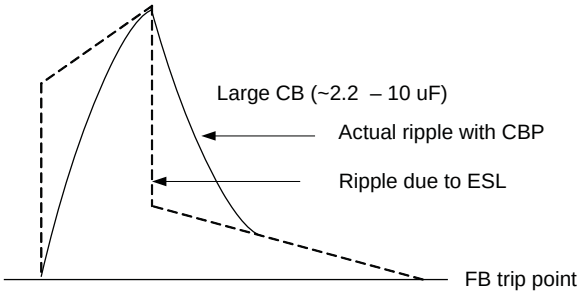


Figure 19

A second solution is to add a small RC filter in series with the FB resistors, shown by RF/CF in Figure 20. This RC filter is intended to remove the high-frequency noise but still allow the ripple to reach the FB pin. Recommended values are 10 ohms and 10nF.

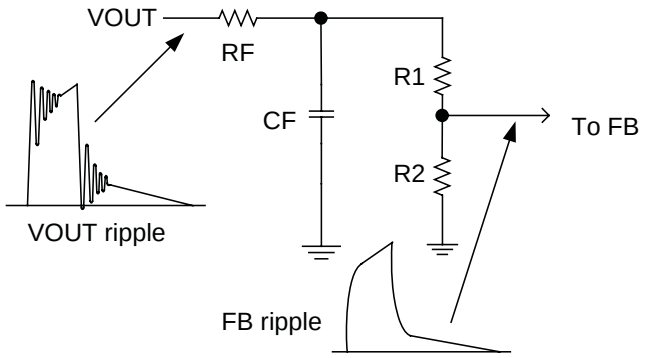


Figure 20

Dropout Performance

The VOUT adjust range for continuous-conduction operation is limited by the fixed 330nsec (typical) Minimum Off-time One-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The IC duty-factor limitation is given by:

$$DUTY = TON_{MIN} / (TON_{MIN} + TOFF_{MAX})$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case drop-out duty-factor calculations.

SC416 System DC Accuracy (VOUT Controller)

Three factors affect VOUT accuracy: the trip point of the FB error comparator, the switching frequency variation with line and load, and the external resistor tolerance. The error comparator is trimmed to trip when the FB pin is 750mV, +/-1% over the range of 0 to 85°C.

Applications Information (continued)

The on-time pulse is programmed using the RTON resistor to give a desired frequency. However, some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because constant on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, If the output ripple is 50mV with VIN = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with VIN = 25 volts, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation it is often desirable to use passive droop. Take the feedback directly from the output side of the inductor, placing a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced.

The use of 1% feedback resistors contributes typically 1% error. If tighter DC accuracy is required use 0.1% resistors. Note that for the internal preset voltages, the FB accuracy of 1.25% for 0 to 85°C already includes the tolerance of the internal resistors.

The output inductor value may change with current. This will change the output ripple and thus the DC output voltage. The output ESR also affects the ripple and thus the DC output voltage.

Switching Frequency Variation

The switching frequency will vary somewhat due to line and load conditions. The line variations are a result of a fixed offset in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As input voltage increases, these factors make the actual DH on-time slightly longer than the idealized on-time. The net effect is that frequency tends to fall slightly with increasing input voltage.

The frequency variation with load is due to losses in the power train from IR drop and switching losses. For a conventional PWM constant-frequency topology, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A constant on-time topology must also overcome the same losses by increasing the effective duty cycle (more time is spent drawing energy from VIN as losses increase). Since the on-time is constant for a given VOUT/VIN combination, the way to increase duty cycle is to gradually shorten the off-time. The net effect is that switching frequency increases slightly with increasing load.

Layout Guidelines

As with any switch-mode converter, and especially a dual-channel converter, a good pcb layout is essential for optimum performance. The following guidelines should be used for PCB layout.

Placement

Note that the pins on the IC are arranged in four groups, i.e. Side1 Power, Side2 Power, Side1 Analog, and Side2 Analog, as shown in Figure 21.

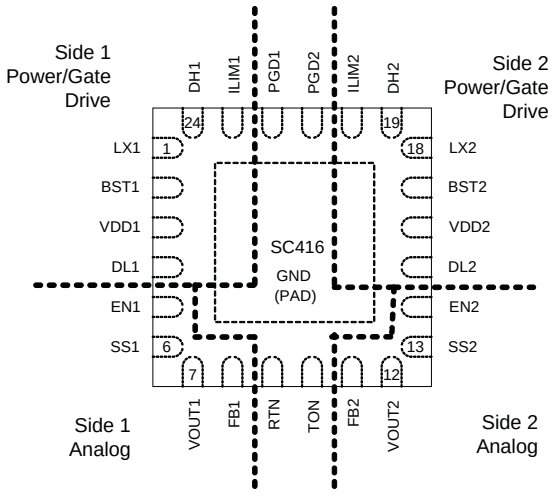


Figure 21

SEMTECH

Applications Information (continued)

For placement, power devices for side1 should be grouped together near the gate drive pins for side1 (pins 23-24 and 1-8). Power devices for side2 should be grouped together near the gate-drive pins for side2 (pins 15-20).

The feedback and VOUT sense components should be located near the FBx/VOUTx pins. This includes the feedback resistors and capacitors if used.

Ground Connections

When doing placement, be aware that there are four grounds to consider on the pcb. ‘

1. Power ground for Side1
2. Power ground for Side2
3. Analog ground for Side1
4. Analog ground for Side2

Note that grounds (1) and (2) are high-current and contain high noise. These grounds carry the DL gate drive current as well as the high switching current through the MOSFETs and low-side diode. It is important to note that the SC416 has only one power ground pin (PAD, pin 25), which must drive DL for both side1 and side2. As such, the low-side MOSFET and diode will need to be near the IC.

Grounds (3) and (4) are low-current and intended for low-noise VOUT/FB ripple sensing. Note that there is only one analog ground pin (RTN, pin 9) which shared between sides 1 and 2

Proper connection between the grounds is needed for good operation. Generally, all ground connections between the power components and the SC416 should be short and direct, without vias where possible. Each side has significant high-current switching in the ground path, moving between the input capacitors, the low-side MOSFET, the low-side diode if used, and the output capacitors. Moreover, each side has significant high-current pulses to/from the ground PAD, created by the DL drive to the low-side MOSFETs. The DL gate-drive current peaks can be 2 amps or more, with fast switching. As such the ground connection between the low-side MOSFETs and the ground PAD should be as short and wide as practical.

Note that the ground PAD, which is the return path for the high-noise DL drive current, is not accessible on the top layer of the pcb, due to the other pins. The ground PAD connection to the MOSFETs must therefore be done on an inner or bottom layer. For this reason, it is best to place the low-side MOSFET on the opposite side of the pcb, to allow a wide and direct connection to the ground PAD on the bottom layer. Otherwise an inner layer must be used for the ground PAD connection; if needed, this should be done with many vias to minimize the high-frequency impedance. This applies to both side1 and side2 MOSFETs.

The remaining power devices should then be placed with their ground pins near each other, and near the IC. That is, the ground connections between the IC, the low-side MOSFET, the low-side diode (if used), the input capacitors, and the output capacitor, should be short. The other non-ground power connections (from input cap to high-side MOSFET, from MOSFETs to inductor, and from inductor to output capacitor) should be short and wide as well, to minimize the loop length and area.

Use short, wide traces from the DL/DH pins to the MOSFETs to reduce parasitic impedance; the low-side MOSFET is most critical. Maintain a length to width ratio of <20:1 for gate drive signals. Use multiple vias as required for current handling (and to reduce parasitics) if routed on more than one layer.

When placing the power components, also be aware that the VOUT signal must route back to the analog components. It is important that this feedback signal not cross the DH/DL/BST or other high-noise power signals. Place and rotate the power components in a way that allows the VOUT trace to get from the output capacitor to the

Applications Information (continued)

analog components without crossing the high-noise power signals (DH/DL/BST, etc).

The analog components are those which connect to the FB and VOUT pins. The FB pins are sensitive so the copper area of these traces should be minimized. Components connected to FB should be placed directly near the IC and should not be placed over or near the gate drive or power signals (DL/DH/BST/ILIM/LX/VDD).

The connection between power ground (PAD) and analog ground (RTN) should be done at a single point directly at the IC. The analog components should be placed in their own ground island which connects to the PAD directly at the IC, and all analog components should connect directly to this island.

Overall placement should look similar to Figure 22.

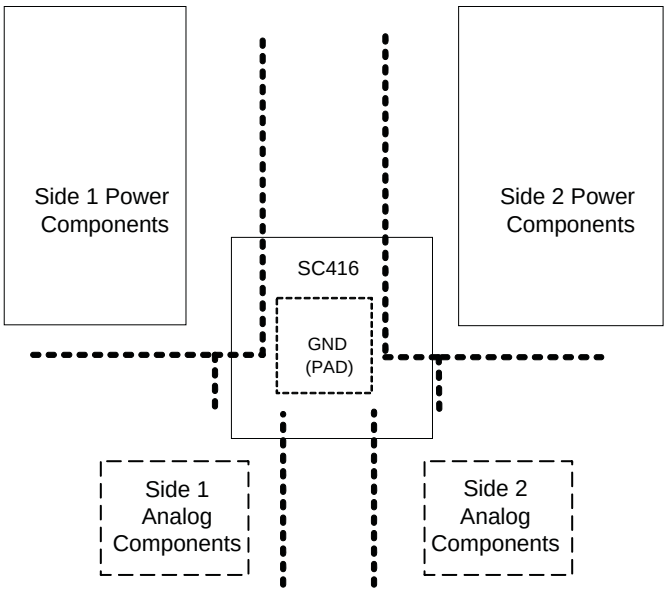


Figure 22

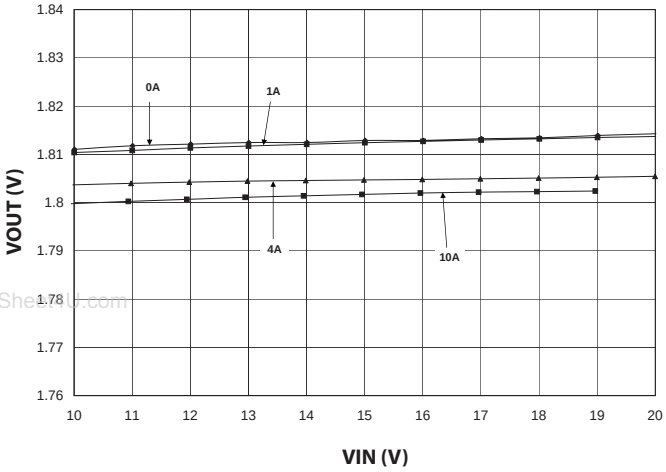
The VDD supply decoupling capacitors should connect to the IC with short traces, with multiple vias if needed.

Connect the ILIM traces to the low-side MOSFET directly at the drain pins, and route these traces over to the ILIM resistor on another layer if needed.

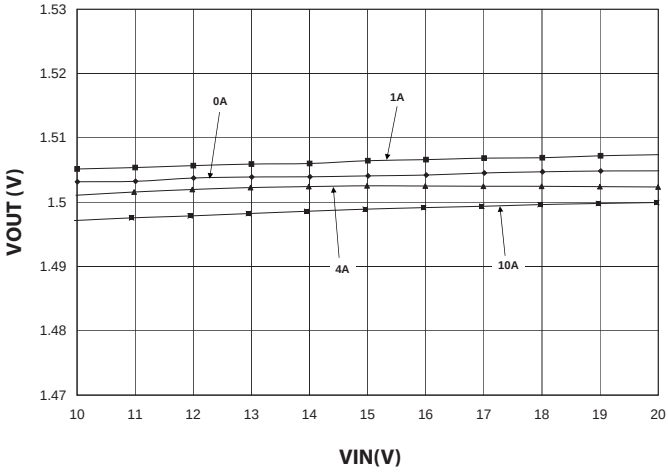
Route the VOUT/FB feedback traces in a “quiet” layer, away from noise sources. Avoid routing near any of the high-noise switching signals or other noise sources.

Typical Characteristics

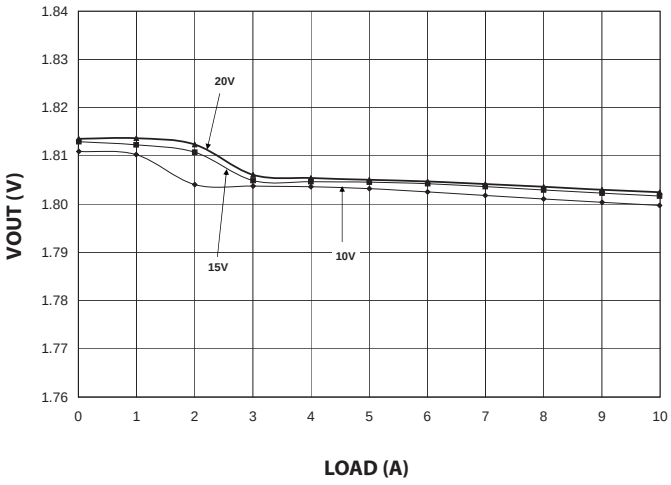
VOUT1 Line Regulation 1.8V PSAVE Enabled



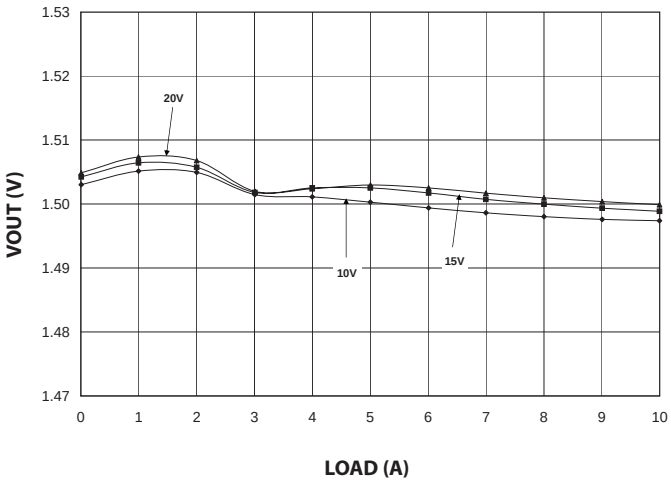
VOUT2 Line Regulation 1.5V PSAVE Enabled



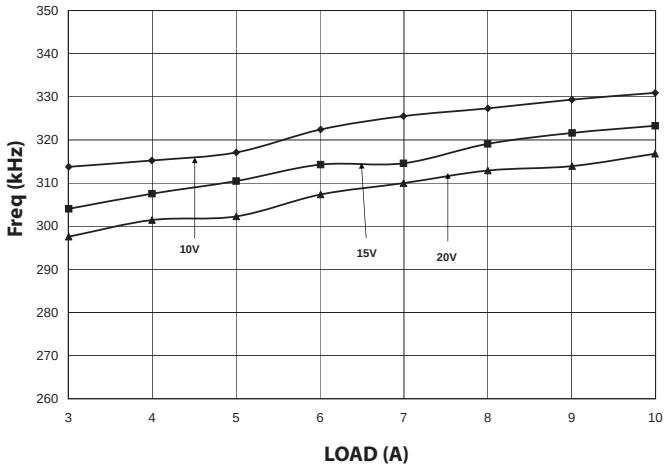
VOUT1 Load Regulation 1.8V PSAVE Enabled



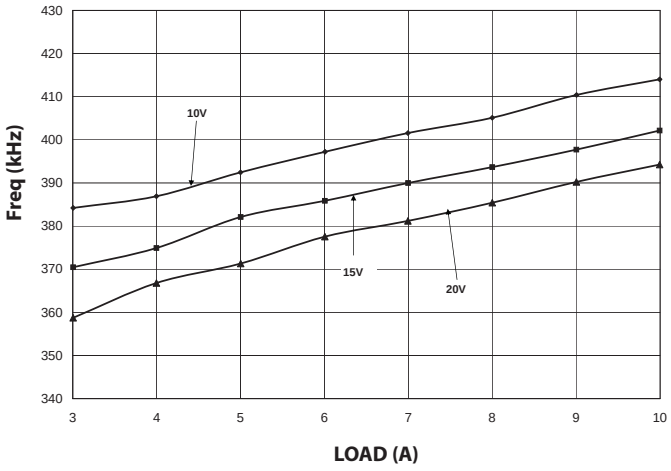
VOUT2 Load Regulation 1.5V PSAVE Enabled



Frequency vs. Load, VOUT1 at 1.8V

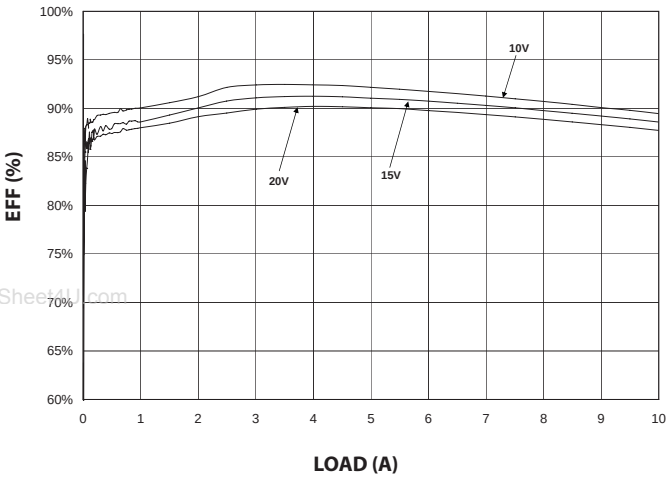


Frequency vs. Load, VOUT2 at 1.5V

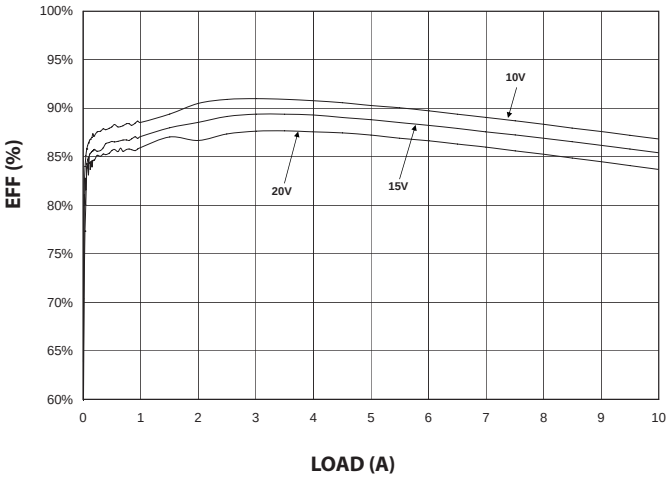


Typical Characteristics

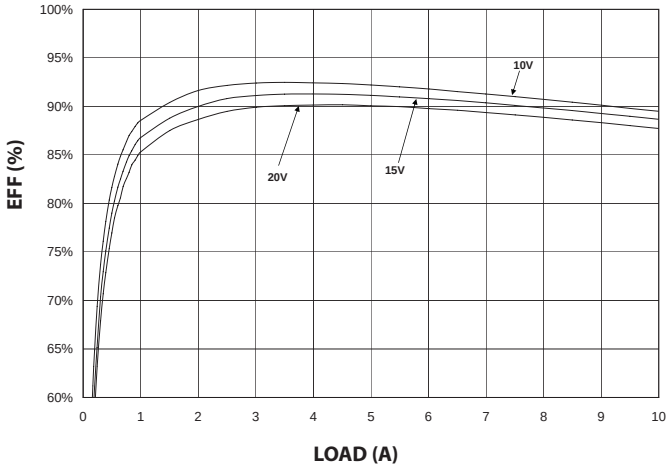
VOUT1 Efficiency, 1.8V PSave Enabled



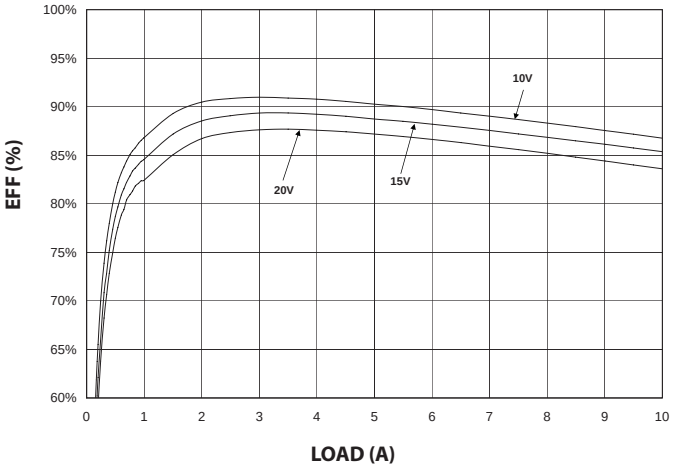
VOUT2 Efficiency, 1.5V PSave Enabled



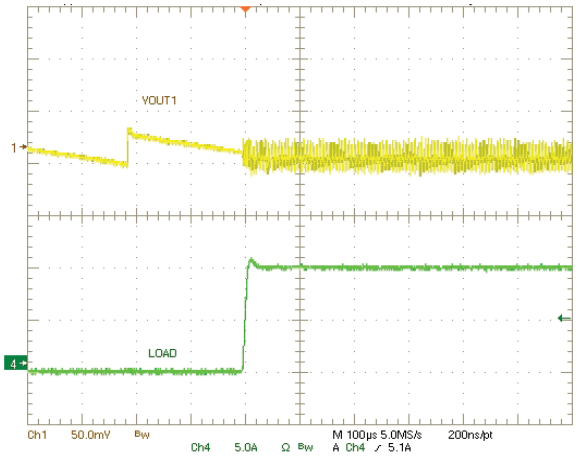
VOUT1 Efficiency, 1.8V PSave Disabled



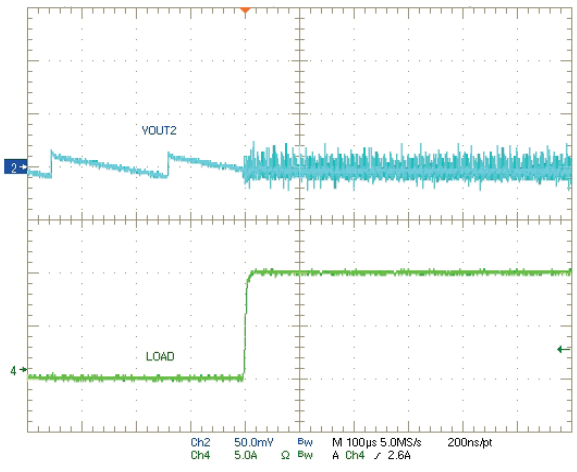
VOUT2 Efficiency, 1.5V PSave Disabled



Load Step VOUT1, 1.8V

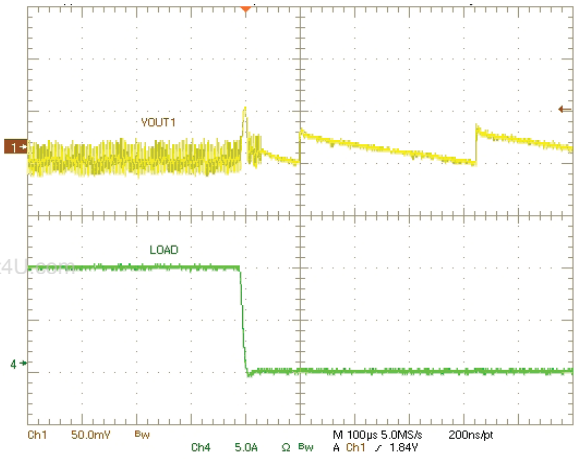


Load Step VOUT2, 1.5V

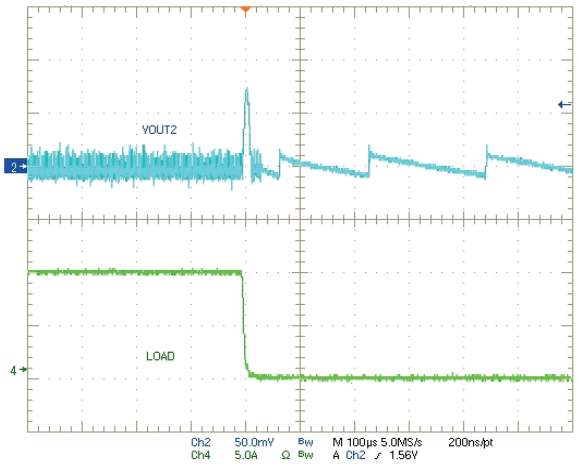


Typical Characteristics

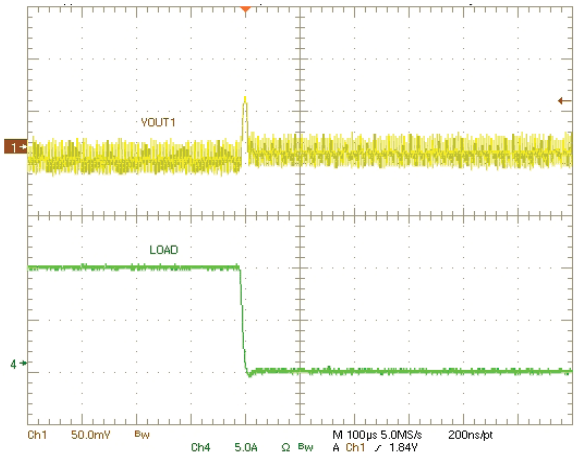
Load Release VOUT1, 1.8V PSAVE Enabled



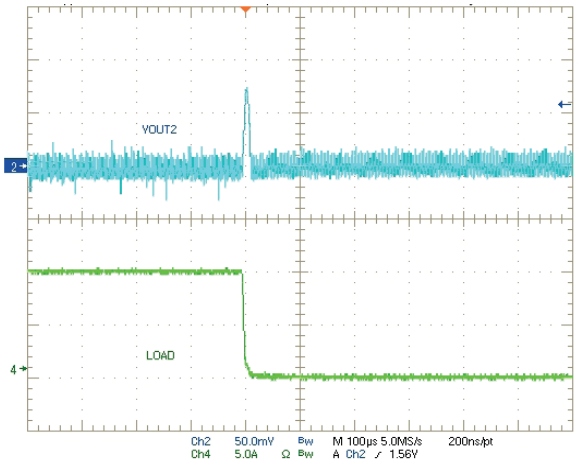
Load Release VOUT2, 1.5V PSAVE Enabled



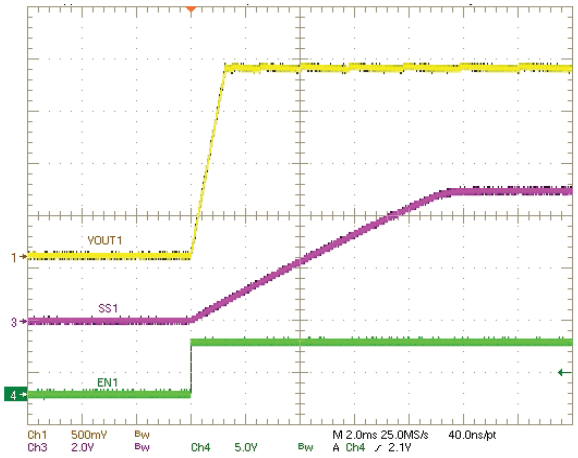
Load Release VOUT1, 1.8V PSAVE Disabled



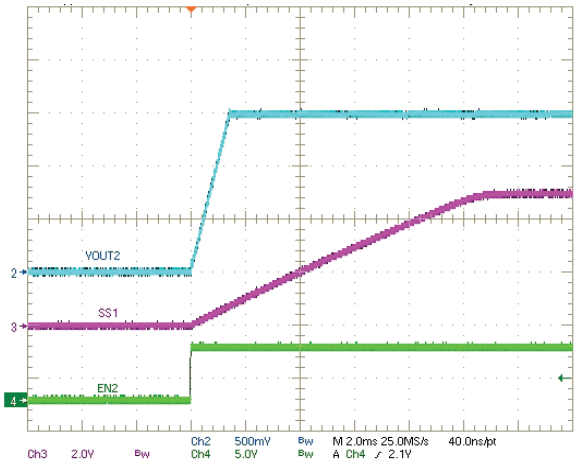
Load Release VOUT2, 1.5V PSAVE Disabled



Independent Startup VOUT1, 1.8V No Load

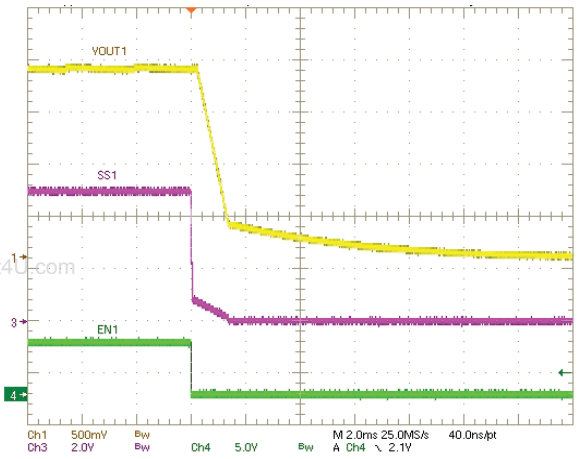


Independent Startup VOUT2, 1.5V No Load

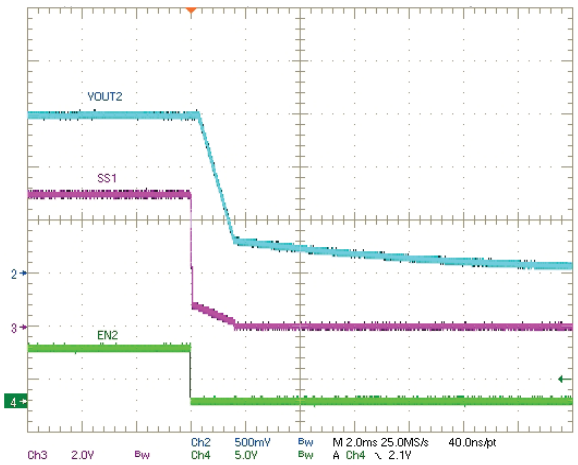


Typical Characteristics

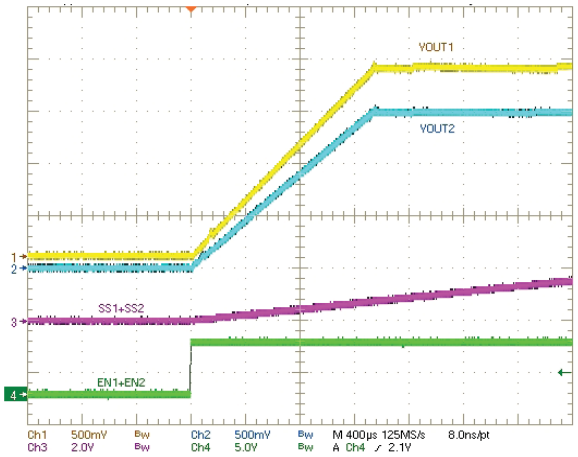
Independent Shutdown VOUT1, 1.8V No Load



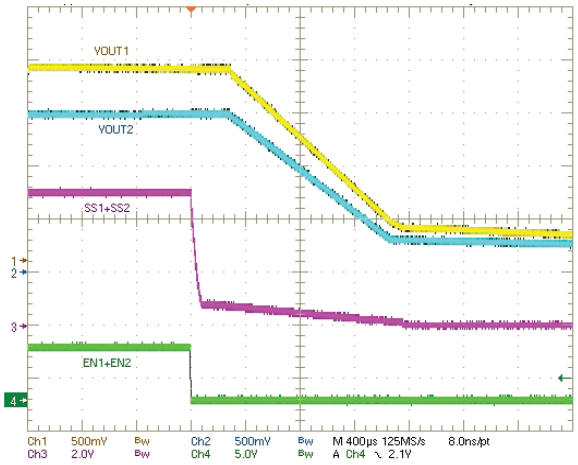
Independent Shutdown VOUT1, 1.8V No Load



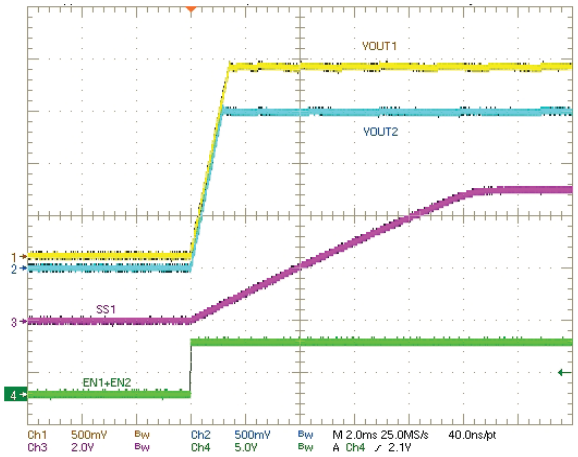
Proportional Tracking Startup



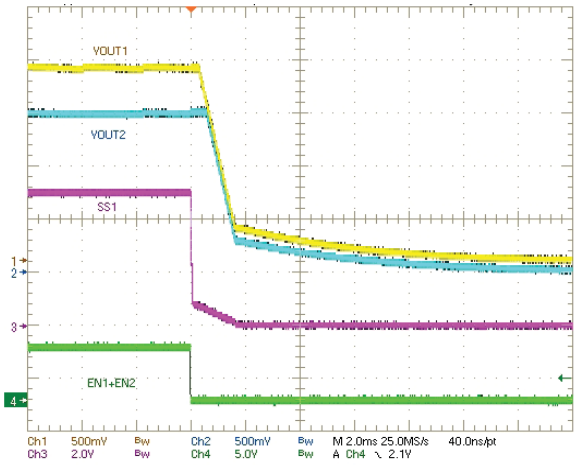
Proportional Tracking Shutdown



Coincident Tracking Startup

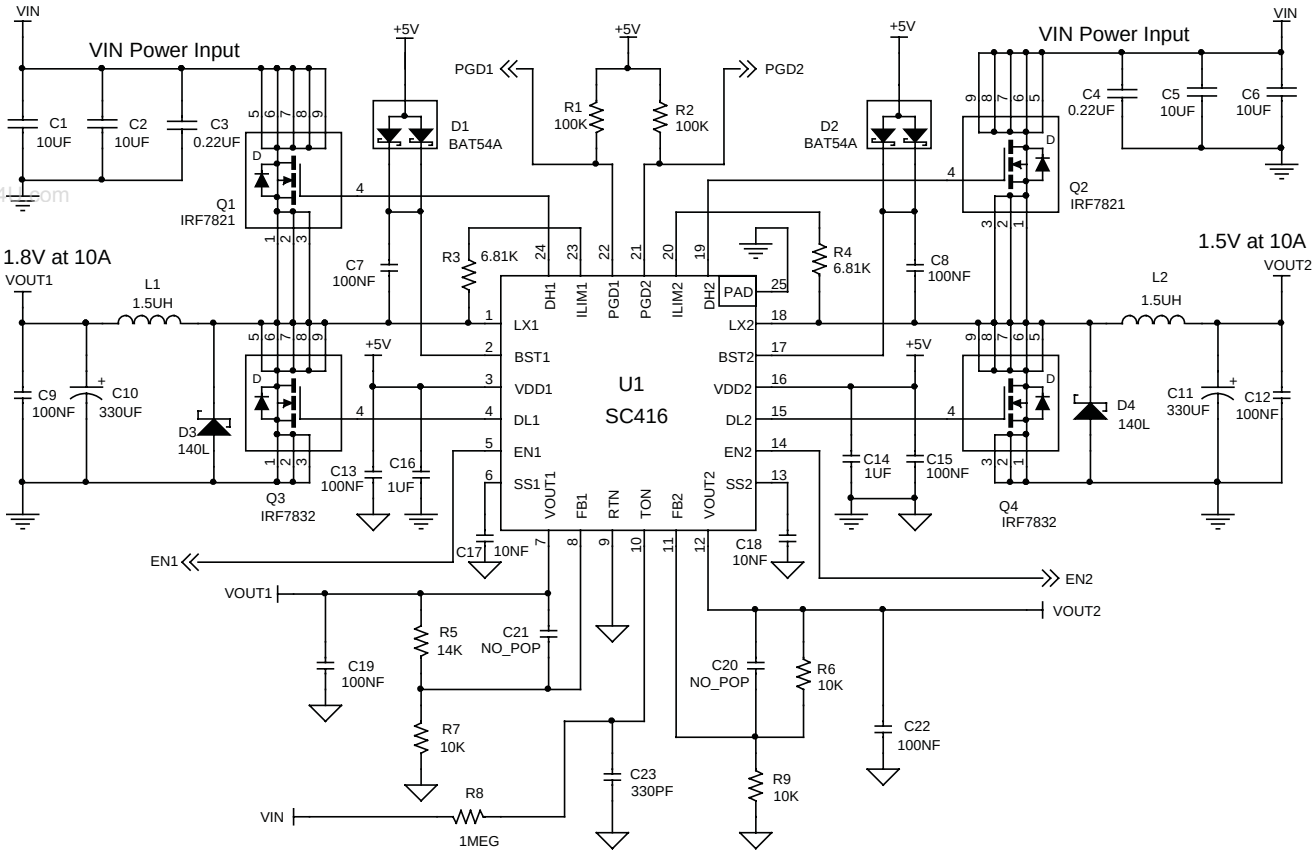


Coincident Tracking Shutdown



Applications Information (continued)

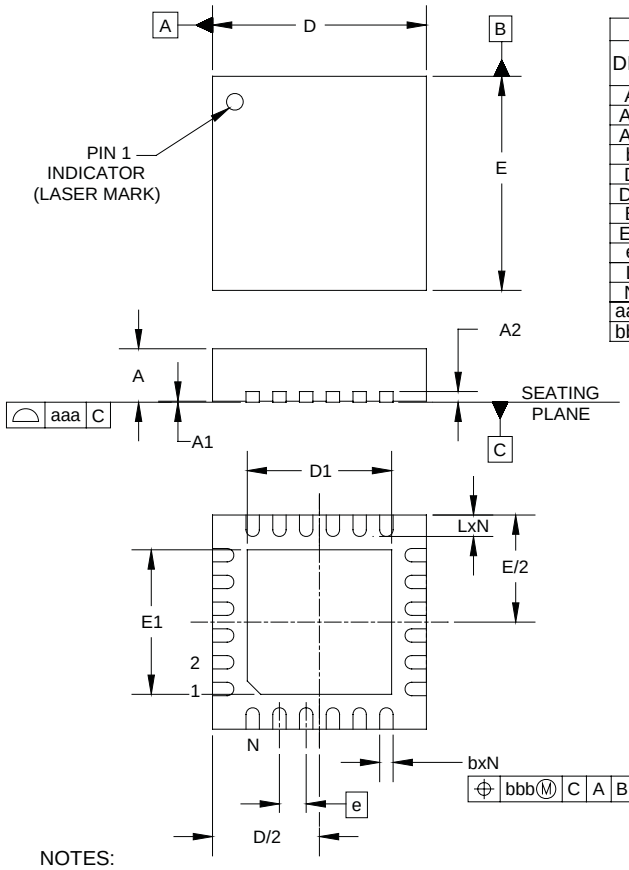
Reference Design



Bill of Materials

Component	Value	Manufacturer	Part Number	Web
C1,C2,C5,C6	10uF, 25V	Murata	GRM32DR71E106KA12L	www.murata.com
C10,C11	330uF/6mΩ/2V	Panasonic	EEFSX0D331XR	www.panasonic.com
D1,D2	200mA/30V	OnSemi	BAT54A	www.onsemi.com
D3,D4	1A/40V	OnSemi	MBSR140LT3	www.onsemi.com
L1,L2	1.5uH/19A	Vishay	IHLP5050CER1R5M01	www.vishay.com
Q1,Q2	30V/12.5mΩ	I.R.	IRF7821	www.irf.com
Q3,Q4	30V/12.5mΩ	I.R.	IRF7832	www.irf.com

Outline Drawing - MLPQ-24

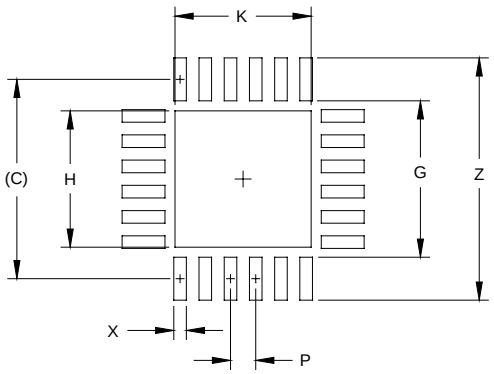


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.040	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.151	.157	.163	3.85	4.00	4.15
D1	.100	.106	.110	2.55	2.70	2.80
E	.151	.157	.163	3.85	4.00	4.15
E1	.100	.106	.110	2.55	2.70	2.80
e	.020 BSC			0.50 BSC		
L	.011	.016	.020	0.30	0.40	0.50
N	24			24		
aaa	.004			0.10		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLPQ-24



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.155)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.021	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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Phone: (805) 498-2111 Fax: (805) 498-3804

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