

POWER MANAGEMENT

PRELIMINARY

Description

The SC4210 Linear Regulator Controller includes all the features required for an extremely low dropout linear regulator that uses an external N-channel MOSFET as the pass transistor. The device can operate from input voltages as low as 4V and can provide high current levels, thus providing an efficient linear solution for custom processor voltages, bus termination voltages, and other logic level voltages down to 0.5V. The on board charge pump creates a gate drive voltage capable of driving an external N-MOSFET which is optimal for low dropout voltage and high efficiency. The wide versatility of this IC allows the user to optimize the setting of both current limit and output voltage for applications beyond or between standard 3-terminal linear regulator ranges.

The 8-pin controller IC features a duty ratio current limiting technique that provides peak transient loading capability while limiting the average power dissipation of the pass transistor during fault conditions.

The SC4210 is available in an MSOP-8 surface mount package.

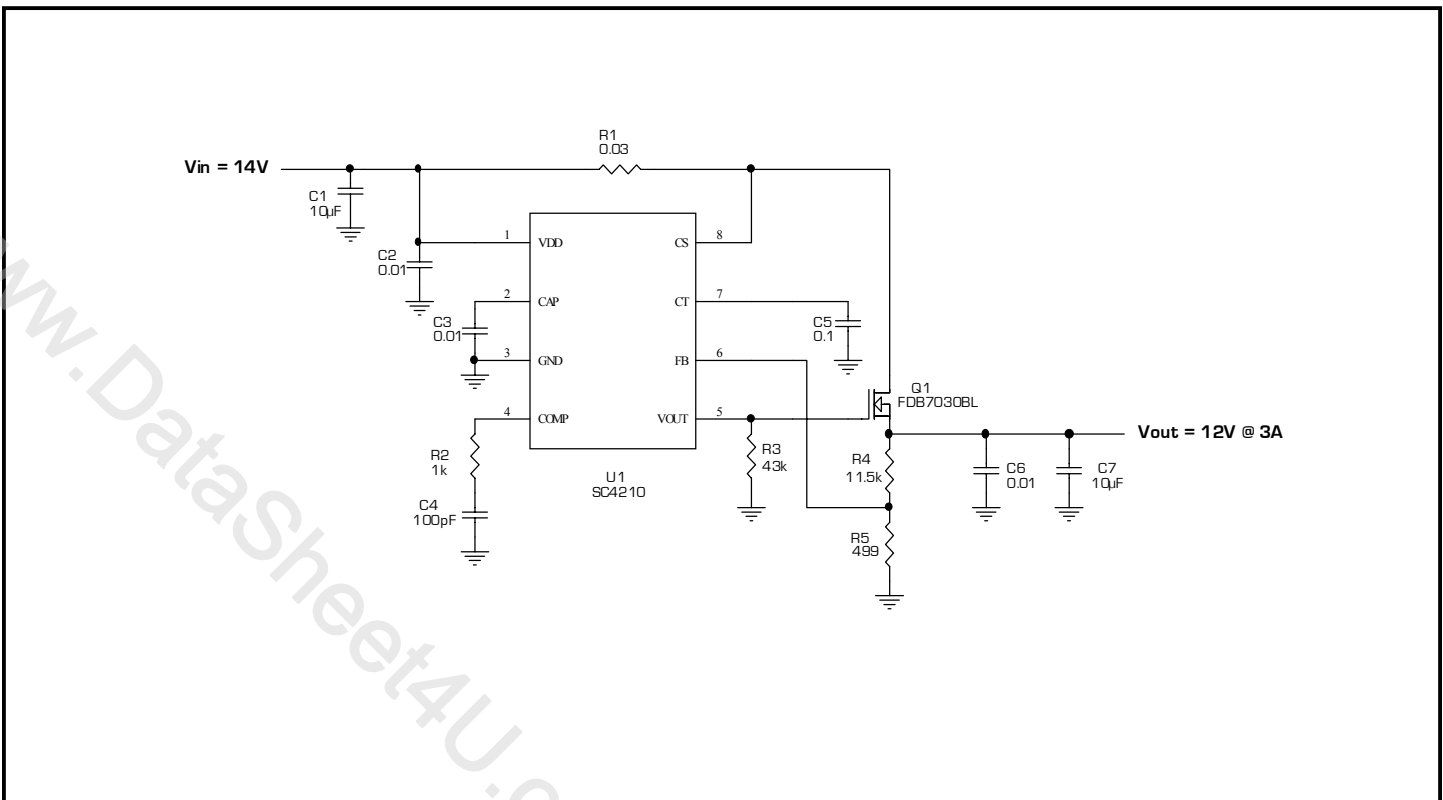
Features

- ◆ On-board charge pump to drive external N-MOSFET
- ◆ Input voltage as low as 4V, up to 15V
- ◆ Duty ratio mode over-current protection
- ◆ Extremely low dropout voltage
- ◆ Low external parts count
- ◆ Output voltages as low as 0.5V
- ◆ MSOP-8 package

Applications

- ◆ Telecom and networking cards
- ◆ Industrial applications
- ◆ Wireless infrastructure
- ◆ Set-top boxes
- ◆ Post regulated power supplies

Typical Application Circuit



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Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Limits	Units
CAP, COMP, VOUT, VDD, CS		-0.3 to +15	V
CT, FB		-0.3 to +6	V
Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C
Thermal Impedance Junction to Ambient	θ_{JA}	207	°C/W

Electrical Characteristics

Unless specified: $T_J = T_A = -40$ to 125°C , $V_{DD} = 4\text{V}$ to 14V , $C_T = 10\text{nF}$, $C_{CAP} = 100\text{nF}$.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Supply						
Supply Current		$V_{DD} = 5\text{V}$		2.3	3.3	mA
Under Voltage Lockout						
Minimum Voltage to Start				4.2		V
Hysteresis				200		mV
Reference						
V_{REF}		$V_{DD} = 5\text{V}, T_J = 25^\circ\text{C}$	495	500	505	mV
		$V_{DD} = 5\text{V}, T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	485		515	mV
Current Sense						
Comparator Threshold				120		mV
Amplifier Threshold				150		mV
Input Bias Current				0.35	0.7	μA

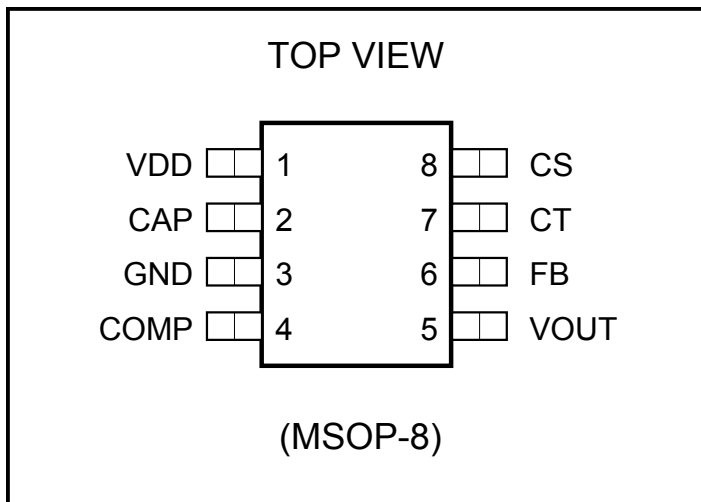
POWER MANAGEMENT
PRELIMINARY
Electrical Characteristics

 Unless specified: $T_J = T_A = -40$ to 125°C , $V_{DD} = 4\text{V}$ to 14V , $C_T = 10\text{nF}$, $C_{CAP} = 100\text{nF}$.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Current Fault Timer						
CT Charge Current		$V_{CT} = 1.3\text{V}$, $V_{DD} = 5\text{V}$	35	40	70	μA
CT Discharge Current		$V_{CT} = 1.3\text{V}$, $V_{DD} = 5\text{V}$	1.0	2.0	3.0	μA
CT Fault Low Threshold				0.3		V
CT Fault High Threshold				1.7		V
Fault Duty Cycle			2.5	3.2	4.0	%
Error Amplifier						
Input Bias Current				0.2	0.5	μA
Open Loop Gain				66		dB
Transconductance		$-10\mu\text{A}$ to $10\mu\text{A}$, $V_{DD} = 5\text{V}$	0.7	0.9		mS
Output Impedance				2.6		$\text{M}\Omega$
Unity Gain Crossover	GBW			5		MHz
Source Current		$V_{DD} = 5\text{V}$	30	55		μA
Sink Current		$V_{DD} = 5\text{V}$	45	70		μA
FET Driver						
Peak Output Current		$V_{CAP} = 10\text{V}$, $V_{OUT} = 1\text{V}$	1.3	2.5		mA
Average Output Current		$V_{OUT} = 1\text{V}$, $V_{DD} = 5\text{V}$	200	330		μA
Max Output Voltage		$V_{DD} = 4.5\text{V}$, $I_{CAP} = 10\mu\text{A}$	8	9.0		V
Charge Pump						
CAP Voltage		$V_{DD} = 4.5\text{V}$, $CS = 0\text{V}$	8.5	9.4		

Note:

(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

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Pin Configuration

Ordering Information

Part Number ⁽¹⁾	Package
SC4210IMSTR ⁽²⁾	MSOP-8
SC4210EVB	EVALUATION BOARD

Notes:

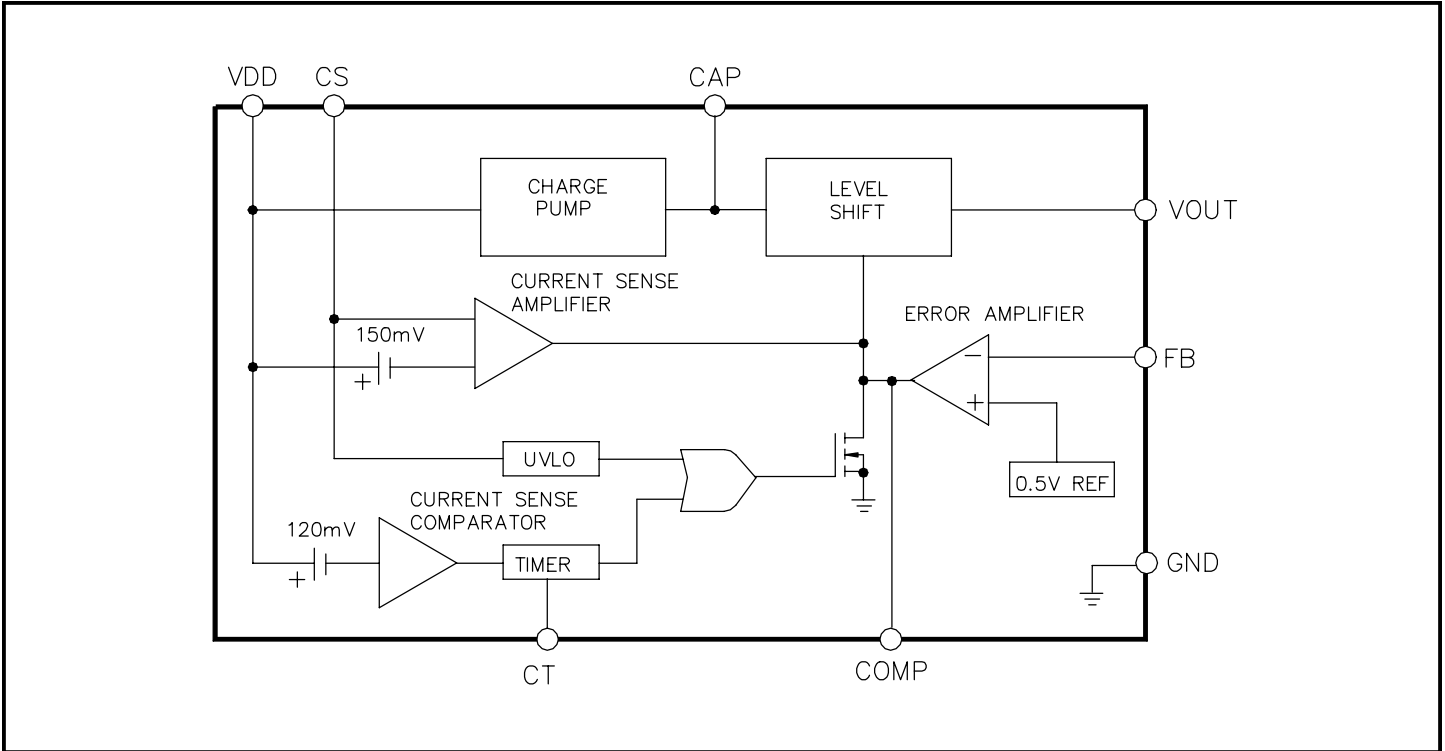
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin	Pin Name	Pin Function
1	VDD	The system input voltage is connected to this point. VDD must be above 4V. VDD also acts as one side of the current sense amplifier and comparator.
2	CAP	The output of the charge pump circuit. A capacitor is connected between this pin and GND to provide a floating bias voltage for an N-Channel MOSFET gate drive. A minimum of a 0.01 μ F ceramic capacitor is recommended. CAP can be directly connected to an external regulated source, in which case the external voltage will be the source for driving the N-Channel MOSFET.
3	GND	Ground reference for device.
4	COMP	The common output of the transconductance error amplifier and current sense amplifier. It is used for compensating the small signal characteristics of the voltage and current loop (when the current sense amplifier is active in over-current mode). Also, it can be utilized as an ON/OFF node; if pulled to GND the circuit will shutdown; if left floating, it will enable normal operation.
5	VOUT	This pin directly drives the gate of the external N-MOSFET pass element. The typical output impedance of this pin is 2.5k Ω
6	FB	The inverting terminal of the voltage error amplifier; used to feedback the output voltage for comparison with the internal reference voltage.
7	CT	The input to the duty cycle timer circuit. A capacitor is connected from this pin to GND, setting the maximum ON time of the over-current protection circuits.
8	CS	The negative current sense input signal. This pin should be connected through a low noise path to the low side of the current sense resistor.

Block Diagram



Control Loop Block Diagram

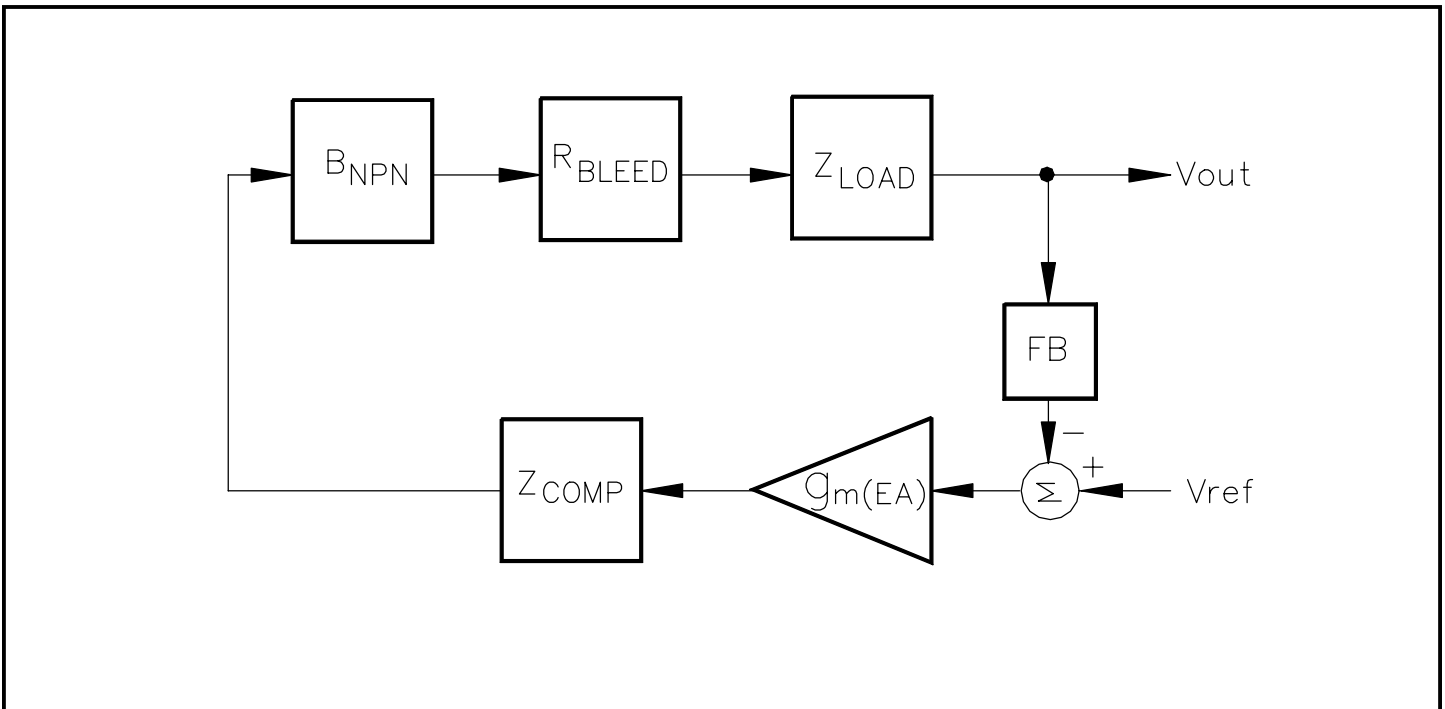


Figure 1.

Basic Operation
Topology

The SC4210 incorporates a charge pump which multiplies the input supply by a factor of approximately three. This charge pump output, or the CAP pin, should be bypassed to GND in order to reduce high frequency ripple – capacitor value isn't critical. The amplified voltage supplies power to both the output stage of the error amplifier and the bipolar buffer transistor which provides the gate potential to the external N-MOSFET.

The error amplifier is a transconductance type with a transconductance of around $0.8\text{mS}_{\text{TYP}}$. The open loop voltage gain is about 66dB. The output of the E/A is compensated externally through the COMP pin with an RC series network.

The OUT pin is a buffered version of the COMP pin with approximately $2.5\text{k}\Omega$ output drive impedance.

Overcurrent protection is accomplished by measuring the voltage potential between the input supply, pin V_{DD} , and the connection of the external sense resistor and drain terminal of the external N-MOSFET at pin CS.

If the potential difference between the CS and V_{DD} exceeds 120mV for a time greater than the value determined by formula (1) below, the device will enter a 4% maximum on-time until the overcurrent condition is removed.

$$T_{\text{delay}} = C_T \cdot 0.3\text{V} \div 36\mu\text{A} \quad (1)$$

where

C_T is the capacitor at the CT pin.

The above applies to the initial overcurrent condition, after which if the overcurrent condition remains in effect, the device will repeatedly cycle on and off according to the following formulas:

$$T_{\text{ON}} = C_T \cdot 1\text{V} \div 36\mu\text{A} \quad (2)$$

$$T_{\text{OFF}} = C_T \cdot 1\text{V} \div 1.6\mu\text{A} \quad (3)$$

During the Gate on-time, the maximum current the pass device may supply is limited to:

$$I_{\text{LIM}} = 150\text{mV} \div R_{\text{SENSE}}$$

The SC4210 incorporates a UVLO rising threshold of 1.9V_{TYP} with 100mV hysteresis.

Stability and Transient Performance

The SC4210 topology allows the device to be configured to have both a stable performance across a wide frequency range as well as react quickly to and recover from transients at the output load.

Experimental and simulated results have shown that the device performs well under the following setup conditions:

$R_{\text{comp}} = 1\text{k}\Omega$; $C_{\text{comp}} = 100\text{pF}$

$C_{\text{OUT}} = 10\mu\text{F}$, MLCC, ESR = 2-3m Ω

$R_{\text{bleed}} (R3) = 43\text{k}\Omega$

$V_{\text{DD}} = 14\text{V}$

$V_{\text{OUT}} = 12\text{V}$

$I_{\text{out}} = 100\text{mA}$ to 3A pulses at $S_r = 0.3\text{A}/\mu\text{s}$

External pass device - FDB7030BL, N-MOSFET

The measured ripple voltage is 89mV pk-pk or better than 0.1%; see Figure 2.

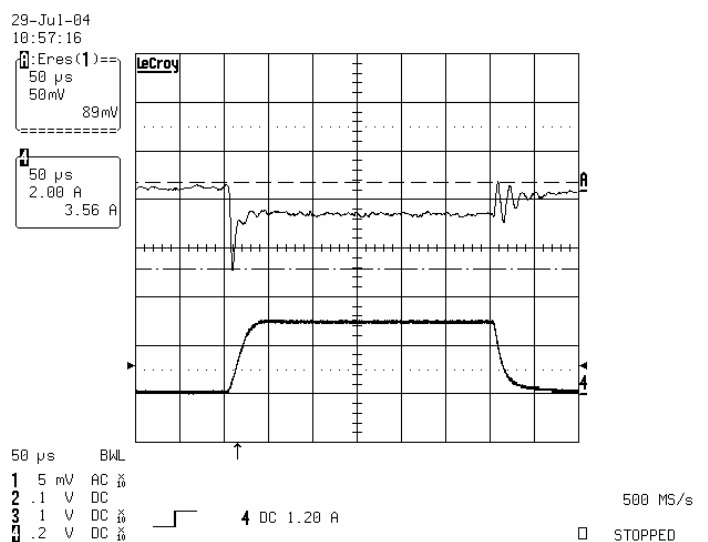


Figure 2.

Applications Information (Cont.)

In Figure 3, below is shown the Bode Plot taken with AP200 frequency response analyzer (Ridley Instruments).

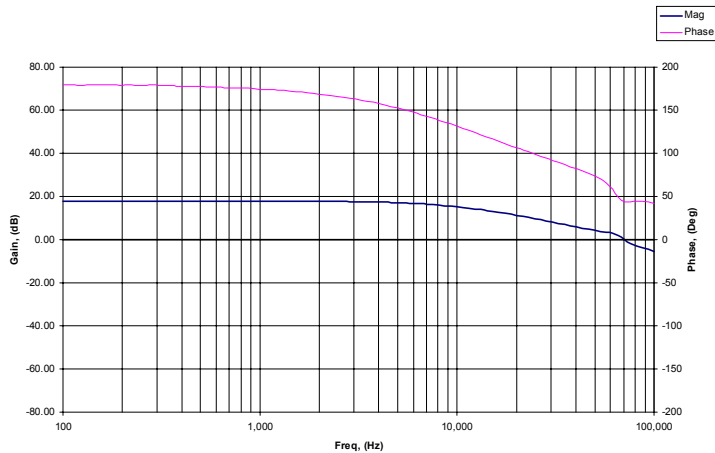


Figure 3.

Compensating the SC4210 can be done by modeling the device in a straight forward fashion using the Control Loop Block Diagram shown in Figure 1.

$$Z_c := \frac{R_c \left(s + \frac{1}{R_c \cdot C_c} \right)}{s}$$

$$R_o := 0.26 \cdot 10^7 \frac{\beta_{nnpn} \cdot R_3}{0.26 \cdot 10^7 + \beta_{nnpn} \cdot R_3}$$

$$F_s := \frac{g_m \cdot R_o \cdot Z_c}{R_o + Z_c}$$

$$g_m := 0.8 \frac{\text{mA}}{\text{V}}$$

$$FB := \frac{R_5}{R_4 + R_5}$$

$$Z_L := \frac{1}{s CL} + \text{Resr}$$

$$G_s := \frac{R_L \cdot Z_L}{R_L + Z_L}$$

$$G_s := \frac{R_L \left(\frac{1}{s CL} + \text{Resr} \right)}{\left(R_L + \frac{1}{s CL} + \text{Resr} \right)}$$

$$H_s := \frac{R_5}{(R_4 + R_5)} \cdot F_s \cdot G_s$$

The basic analysis yields a two pole, two zero system. However, considering a limited bandwidth of the NPN buffer stage and external N-MOSFET, the system eventually rolls off due to the third pole at very high frequencies (10-20MHz). The low ESR ceramic capacitors push the secondary zero to well above the unity gain frequency, requiring accurate placement of the dominant zero for stability.

An output capacitor is not required for stability. If one is used, compensation is required. Assuming there is no output cap present, only Ccomp will be used. Under this condition, the non-dominant pole and both zero's are pushed well above the unity gain frequency.

The pass transistor does add an additional pole to the transfer function. Generally speaking, this parasitic non-dominant pole is at frequencies well above the unity gain frequency but should be considered when various types of N-MOSFETs are available.

The purpose of the R_{BLEED} is to improve the transient response, reduce overshoot, and to remove an unwanted output ripple voltage if no load is applied to the output.

In a practical sense, it is chosen to bleed (drain) about 300µA. The optimum value depends on the input/output voltage ratio and the constraints on the output ripple voltage. Simulation analysis and real life circuit testing have shown very close correlation.

Applications Information (Cont.)

Following the procedure described, yields a stable operation and excellent transient response over a wide range of output capacitors: extra low-ESR “ceramics” and “organics”, mid-ESR “polymers” and “tantalums”, low-cost aluminum capacitors. Below in Table 1 are the summarized results of choosing R_{COMP} and C_{COMP} values for the typical application circuit shown on Page 1.

Test (#)	ESR (mΩ)	C_{OUT} (μF)	C_{COMP} (pF)	No Load		Transient Load*	
				V_{OUT} Ripple (mV)	R_{COMP} (kΩ)	dV_{OUT} p-p (mV)	R_{COMP} (kΩ)
1	3	0.1	100	13.7	1k - 25k	80	1k
2	3	0.1	500	13.2	1k - 25k	145	25k
3	3	0.1	1000	12.8	1k - 25k	178	25k
4	3	1	100	12.8	1k - 25k	74	1k
5	3	1	500	12.3	1k - 25k	129	25k
6	3	1	1000	12.3	1k - 25k	163	25k
7	2	10	100	10.9	1k - 25k	89	1k
8	2	10	500	10.9	1k - 25k	150	25k
9	2	10	1000	10.9	1k - 25k	172	25k
10	350	100	100	9.1	1k - 25k	65	1k
11	350	100	500	11.4	1k - 25k	129	25k
12	350	100	1000	10	1k - 25k	156	25k

Table 1.

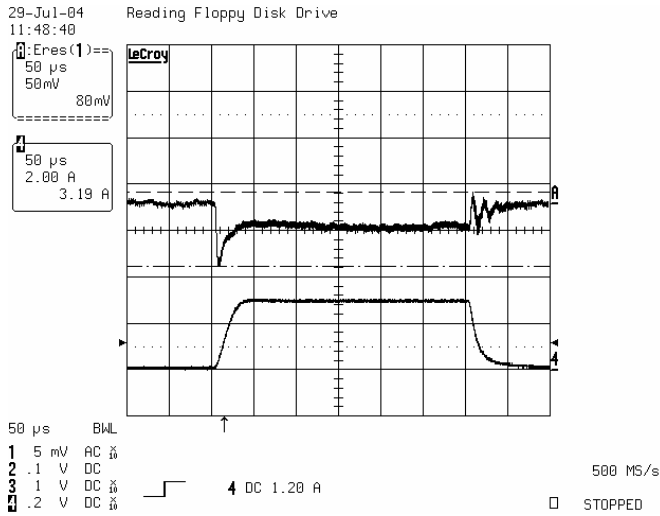
*Transient load conditions:

$$V_{IN} = 14V, V_{OUT} = 12V, I_{OUT} = 3A/0.1A, S_r = 0.3A/\mu s.$$

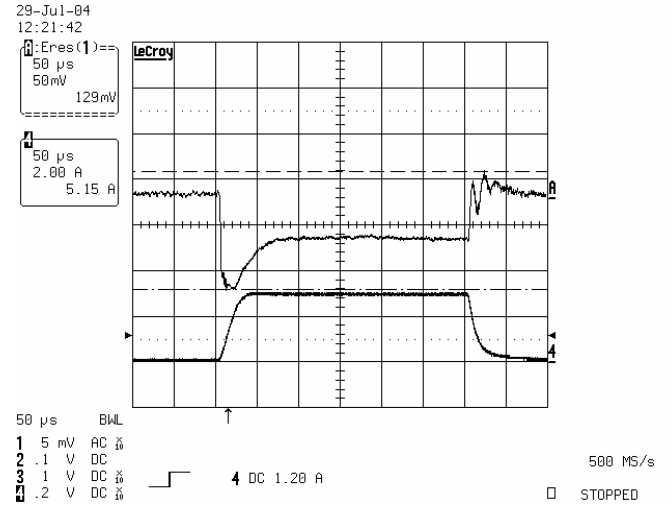
Waveforms show transient tests #1 through #12.

Typical Characteristics

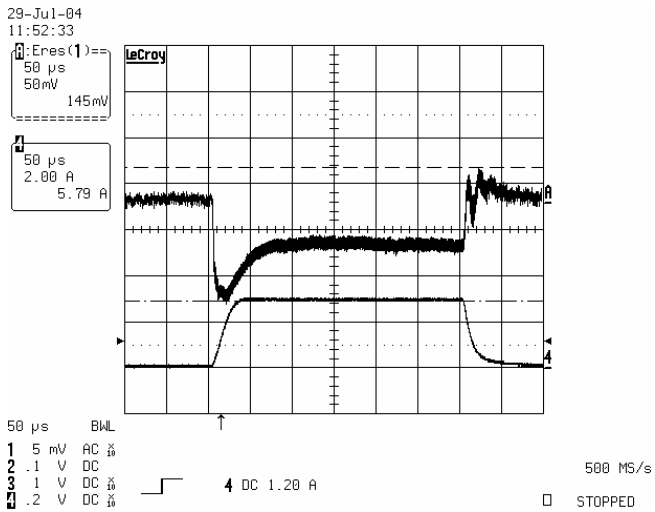
Test #1.



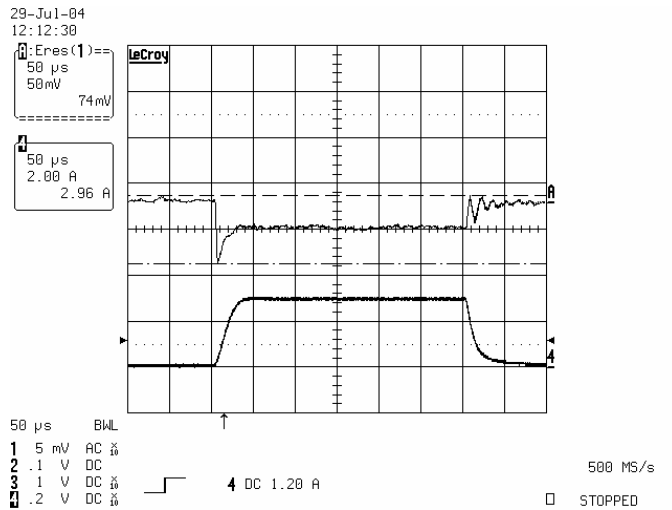
Test #4.



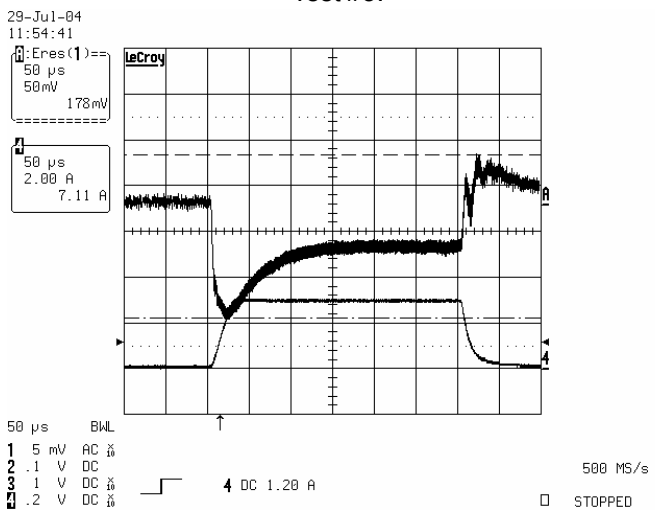
Test #2.



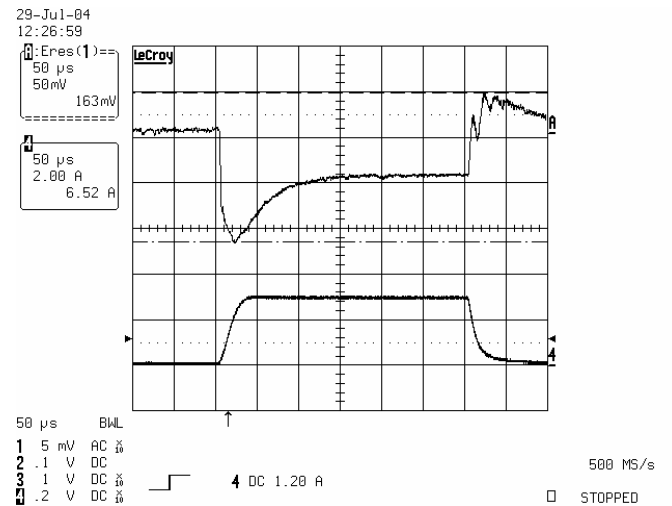
Test #5.



Test #3.

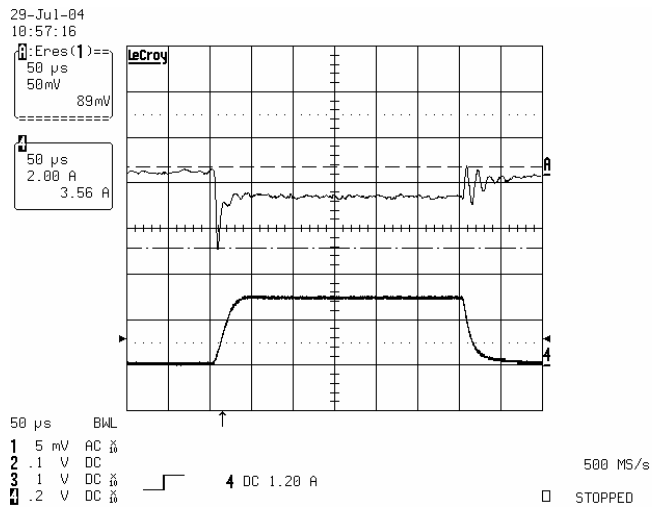


Test #6.

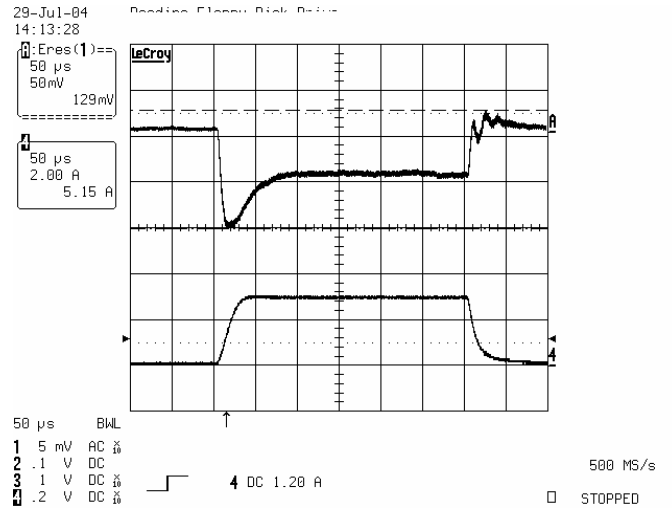


Typical Characteristics (Cont.)

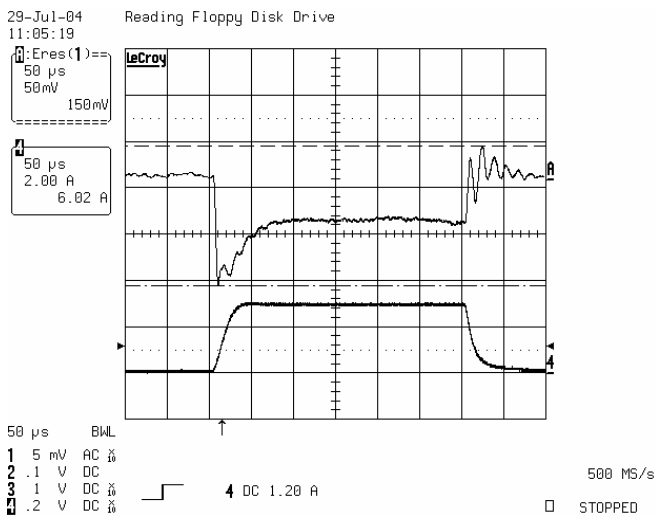
Test #7.



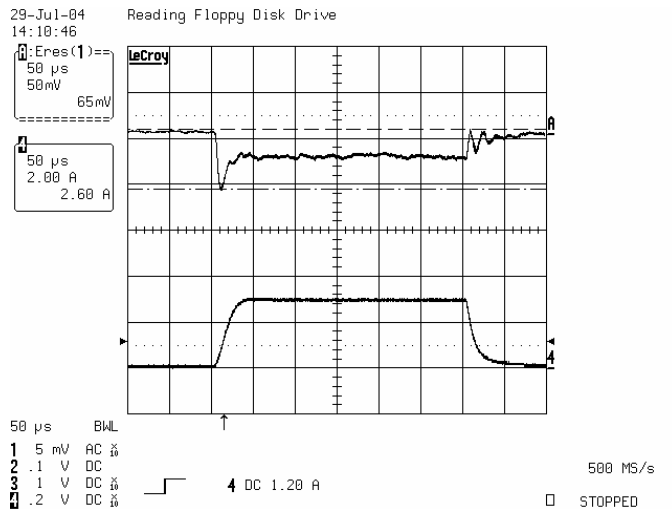
Test #10.



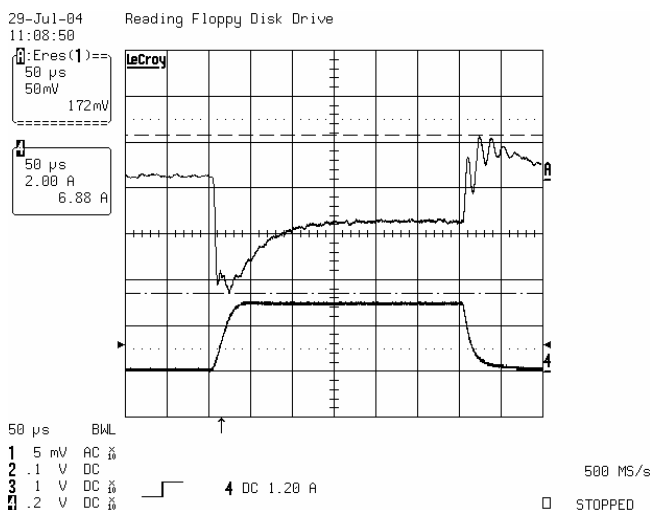
Test #8.



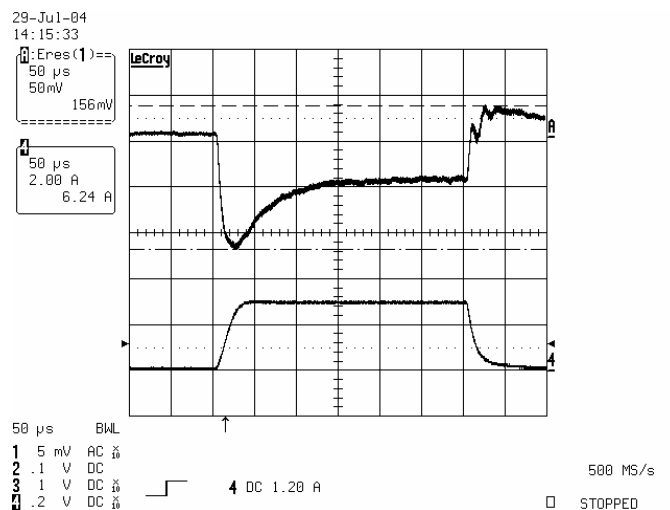
Test #11.



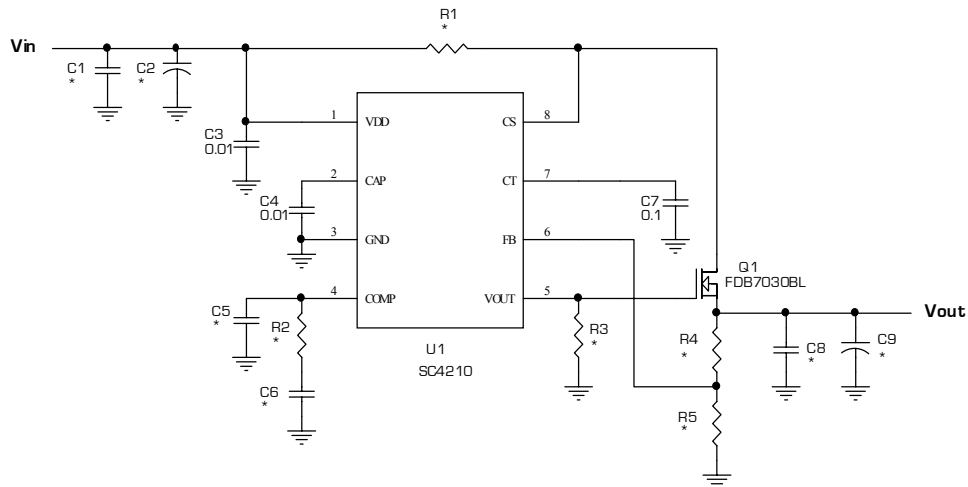
Test #9.



Test #12.

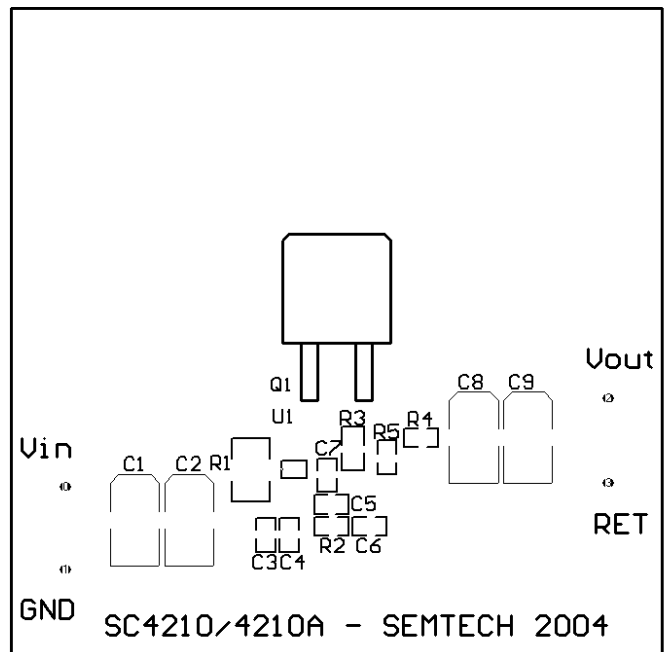
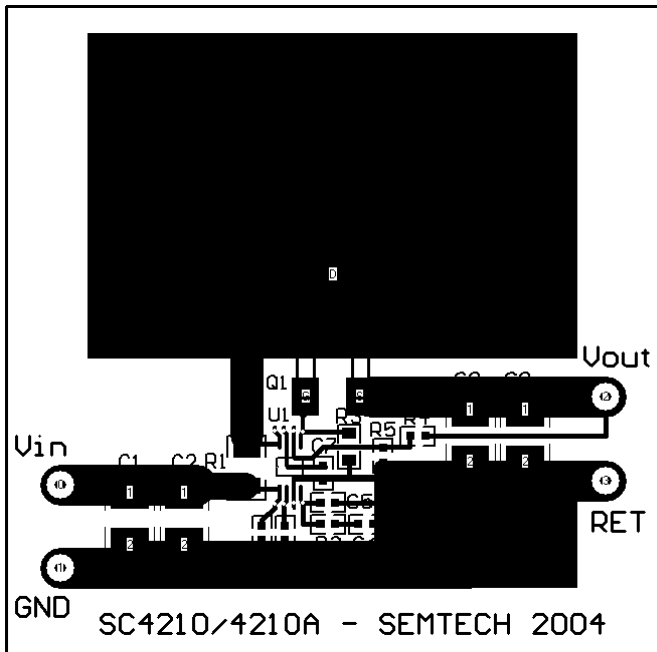


Evaluation Board Circuit

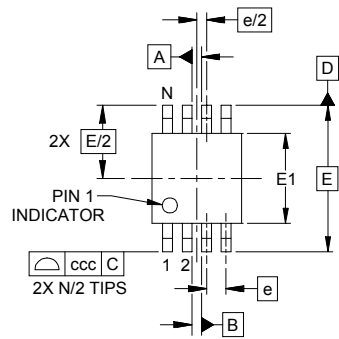


* Denotes variable components

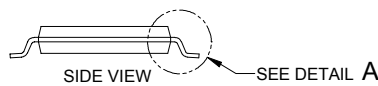
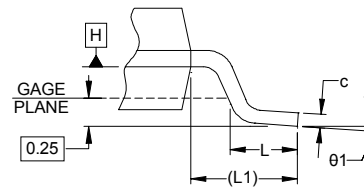
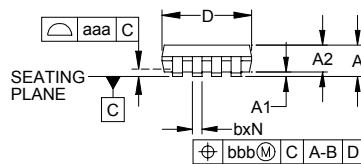
Evaluation Board Layout and Components Placement



Outline Drawing - MSOP-8



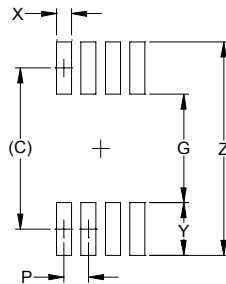
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.009	-	.015	0.22	-	0.38
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.026 BSC			0.65 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.005			0.13		
ccc	.010			0.25		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS [-A-] AND [-B-] TO BE DETERMINED AT DATUM PLANE [-H-]
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION AA.

Land Pattern - MSOP-8



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.026	0.65
X	.016	0.40
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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