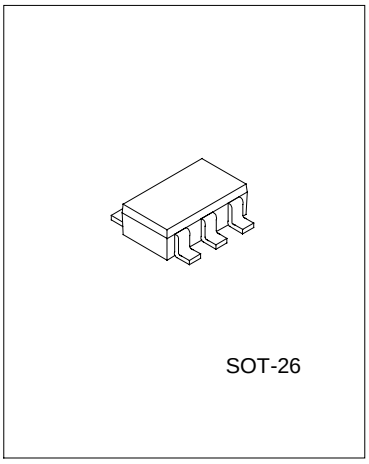
LI-ION BATTERY PROTECTOR



DESCRIPTION

The SC451XX series are protection ICs for over-charge /discharge of rechargeable one-cell Lithium-ion (Li+) batteries by CMOS process.

The SC451XX series can detect over-charge/discharge of Li+ one-cell and excess load current, further include a short circuit protector for preventing large external short circuit current.

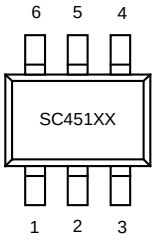
FEATURES

* Low supply current.
* High withstand voltage.
* High accuracy detector threshold.
* Variety of detector threshold.
* Built-in protection circuit.
* Output delay of over-charge.
* Ultra small package: SOT-26

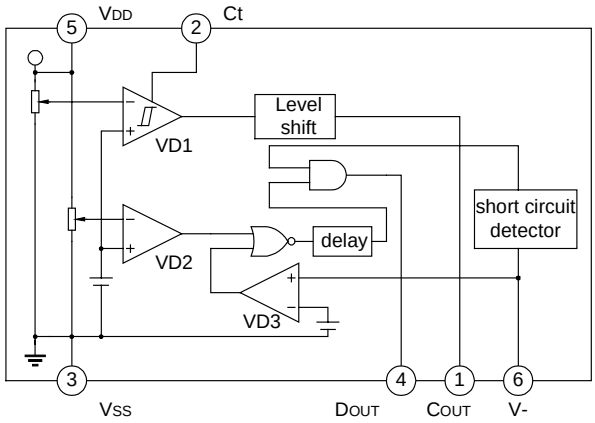
APPLICATIONS

* Over-charge/over-discharge protection for Li+ one-cell pack
* High precision protectors for cell-phones and any other gadgets using on board Li+ one-cell battery.

PIN ASSIGNMENT



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	0.3 ~ 12	V
Input Voltage	V-	V_{DD}-18~V_{DD}+0.3	V
	V_{CT}	Vss-0.3 ~ V_{DD}+0.3	V
Output Voltage	V_{COUT}	V_{DD}-18~V_{DD}+0.3	V
	V_{DOUT}	Vss-0.3 ~ V_{DD}+0.3	V
Power Dissipation	P_D	150	mW
Storage Temperature	T_{STG}	-55 ~ +125	°C
Operating Temperature	T_{OPR}	-40 ~ + 85	°C

ELECTRICAL CHARACTERISTICS (Tamb=25°C, unless otherwise specified)

Sc451XX-01

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD1}	Voltage defined as V_{DD}-V_{SS}	1.5		10	V
Min Operating Voltage for 0V Charging	V_{st}	Voltage defined as V_{DD}-V-, V_{DD}-V_{SS}=0V			1.2	V
Over-charge Threshold Voltage	V_{DET1}	Detect rising edge of supply voltage	4.20	4.25	4.30	V
Over-charge Threshold Hysteresis Range	V_{HYS1}		0.15	0.2	0.25	V
Output Delay Time of Over-charge	T_{VDET1}	C3=0.01μF,V_{DD}=3.6V→4.3V	50	75	100	ms
Over-discharge Threshold Voltage	V_{DET2}	Detect falling edge of supply voltage	2.437	2.500	2.563	V
Output Delay Time of Over-Discharge	T_{VDET2}	V_{DD}=3.6V→2.4V	7	10	13	ms
Excess Current Threshold Voltage	V_{DET3}	Detect rising edge of "V-" pin voltage	0.17	0.20	0.23	V
Output Delay Time of Excess Current	T_{VDET3}	V_{DD}=3.0V	9	13	17	ms
Short Detection Voltage	Vshort	V_{DD}=3.0V	V_{DD}-1.1	V_{DD}-0.8	V_{DD}-0.5	V
Output Delay Time of Short Detection	Tshort	V_{DD}=3.0V		5	50	μs
Reset Resistance for Excess Current Protection	Rshort	V_{DD}=3.6V, V- =1.0	50	100	150	kΩ
Nch ON Voltage of COUT	V_{OL1}	I_{OL}=50μA,V_{DD}=4.4V		0.2	0.5	V
Pch ON Voltage of COUT	V_{OH1}	I_{OH}= -50μA,V_{DD}=3.9V	3.4	3.8		V
Nch ON Voltage of DOUT	V_{OL2}	I_{OL}=50μA,V_{DD}=2.4V		0.2	0.5	V
Pch ON voltage of DOUT	V_{OH2}	I_{OH}= -50μA,V_{DD}=3.9V	3.4	3.7		V
Supply Current	I_{DD}	V_{DD}=3.9V,V- =0V		3.0	6.0	μA
Standby Current	Istandby	V_{DD}=2.0V		0.3	0.6	μA

SC451XX-02

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD1}	Voltage defined as V_{DD}-V_{SS}	1.5		10	V
Min Operating Voltage for 0V Charging	V_{st}	Voltage defined as V_{DD}-V-, V_{DD}-V_{SS}=0V			1.2	V
Over-charge Threshold Voltage	V_{DET1}	Detect rising edge of supply voltage	4.30	4.35	4.40	V
Over-charge Threshold Hysteresis Range	V_{HYS1}		0.15	0.2	0.25	V
Output Delay Time of Over-charge	T_{VDET1}	C3=0.01μF,V_{DD}=3.6V→4.3V	55	80	105	ms
Over-discharge Threshold Voltage	V_{DET2}	Detect falling edge of supply voltage	2.437	2.500	2.563	V
Output Delay Time of Over-discharge	T_{VDET2}	V_{DD}=3.6V→2.4V	7	10	13	ms
Excess Current Threshold Voltage	V_{DET3}	Detect rising edge of "V-" pin voltage	0.17	0.20	0.23	V
Output Delay Time of Excess Current	T_{VDET3}	V_{DD}=3.0V	9	13	17	ms
Short Detection Voltage	Vshort	V_{DD}=3.0V	V_{DD}-1.1	V_{DD}-0.8	V_{DD}-0.5	V
Output Delay Time of Short Detection	Tshort	V_{DD}=3.0V		5	50	μs
Reset Resistance for Excess Current Protection	Rshort	V_{DD}=3.6V, V- =1.0	50	100	150	kΩ
Nch ON Voltage of C_{OUT}	V_{OL1}	I_{OL}=50μA, V_{DD}=4.4V		0.2	0.5	V
Pch ON Voltage of C_{OUT}	V_{OH1}	I_{OH}= -50μA, V_{DD}=3.9V	3.4	3.8		V
Nch ON Voltage of D_{OUT}	V_{OL2}	I_{OL}=50μA, V_{DD}=2.4V		0.2	0.5	V
Pch ON Voltage of D_{OUT}	V_{OH2}	I_{OH}= -50μA, V_{DD}=3.9V	3.4	3.7		V
Supply Current	I_{DD}	V_{DD}=3.9V, V- =0V		3.0	6.0	μA
Standby Current	Istandby	V_{DD}=2.0V		0.3	0.6	μA

PIN DESCRIPTION

PIN No.	Symbol	Description
1	C_{OUT}	Output of over-charge detection, CMOS output
2	C_T	Pin for external capacitor setting output delay of VD1
3	V_{SS}	Ground
4	D_{OUT}	Output of over-discharge detection, CMOS output
5	V_{DD}	Power supply
6	V-	Pin for charger negative input

FUNCTIONAL DESCRIPTION

• VD1/OVER-CHARGE DETECTOR

The VD1 monitors V_{DD} pin voltage. When the V_{DD} voltage crosses over-charge detector threshold V_{DET1} from a low value to a value higher than the V_{DET1}, the VD1 can sense over-charging and an external charge control Nch-MOS-FET turns to "off" with C_{OUT} pin being at "L".

An output delay time for over-charges detection can be set by an external capacitor C3 connecting the V_{SS} pin and Ct pin. The external capacitor can make a delay time form a moment detecting over-charge to a time output a signal which enables charge control Nch-MOS-FET for turning to "off". Though the V_{DD} voltage would be going up to a higher level than V_{DET1} if it is within a time period of the output delay time, VD1 would not output a signal for turning "off" of charge control Nch-MOS-FET. The output delay time can be calculated as below:

$$t_{VDET1} = \frac{C3 \times (VDD - 0.7)}{0.48 \times 10^{-6}}$$

A level shifter incorporated in a buffer driver for the C_{OUT} pin makes the "L" of C_{OUT} pin to the V-pin voltage and the "H" of C_{OUT} pin is set to V_{DD} voltage with CMOS buffer.

• RESET CONDITIONS FROM OVERCHARGING OF SC451XX-01

There can be two cases to reset the VD1 making the C_{OUT} pin level to "H" again after detecting over-charge. Resetting the V_{D1} makes the charging system ready for resumption of charging process.

The first case is in such condition that a time when the V_{DD} voltage is coming down to a level lower than "V_{DET1}-V_{HYS1}". While in the second case, disconnecting a charger from the battery pack can make the VD1 resetting when the V_{DD} level is within hysteresis width (V_{DET1}-$V_{HYS1} \le V_{DD} \le V_{DET1}$).

After detecting over-charge with the V_{DD} voltage of higher than V_{DET1}, connecting system load to the battery pack makes load current allowable through parasitic diode of external charge control Nch-MOS-FET. The C_{OUT} level would be "H" when the V_{DD} level is coming down to a level below the V_{DET1} by continuous drawing of load current.

• RESET CONDITIONS FROM OVERCHARGING OF SC451XX-02

After detecting over-charge, the V_{D1} would not be release and C_{OUT} level would not switch to "H" again with the exception that a cell voltage reaches to a lower value than "V_{DET1}-V_{HYS1}" by self discharge of cell or else. After detecting over-charge, when the V_{DD} level stays at a value higher than "V_{DET1}-V_{HYS1}", to connect battery pack to a system load makes battery pack being disable at for charging or discharging because of excess current detector operated being D_{OUT} "L".

• VD2/OVER-DISCHARGE DETECTOR

The V_{D2} monitors a V_{DD} pin voltage. When the V_{DD} voltage crosses the over-discharge detector threshold V_{DET2} from a high value to a value lower than the V_{DET2}, the V_{D2} can sense an over-discharging and the external discharge control Nch-MOS-FET turns to "off" with the D_{OUT} pin being at "L".

Resetting the V_{D2} with the D_{OUT} pin level being "H" again after detecting over-discharge is only possible by connecting a charger to the battery pack. When the V_{DD} voltage stays under over-discharge detector threshold V_{DET2} charge current can flow through parasitic diode of external discharge control Nch-MOS-FET, then after the V_{DD} voltage comes up to a value larger than V_{DET2} discharging process would be advanced through "on" state discharge control Nch-MOS-FET. Connecting a charger to the battery pack makes the D_{OUT} level being "H" instantaneously when the V_{DD} voltage is higher than V_{DET2}.

When a cell voltage equals to zero, connecting charger to the battery pack makes the system allowable for charge with higher charge voltage than Vst, 1.2V Max.

An output delay time of the over-discharge detection is fixed internally. Though the V_{DD} voltage would be going down to a lower level than V_{DET2} if it is within a time period of the output delay time, V_{D2} would not output a signal for turning "off" of discharge control Nch-MOS-FET.

After detection of an over-discharge by V_{D2}, supply current would be reduced to 0.3μATYP. at V_{DD}=2.0V and into standby, only the charger detector is operating.

The output type of D_{OUT} pin is CMOS having "H" level of V_{DD} and "L" level of V_{SS}.

• VD3/EXCESS CURRENT DETECTOR, SHORT CIRCUIT PROTECTOR

*Both of the excess current detector and short circuit protector can work when both control Nch-MOS-FETs are in "on" state.

When the V-pin voltage is going up to a value between the short protection voltage Vshort and excess current threshold V_{DET3}, the excess current detector operates and further soaring of V-pin voltage higher than Vshort makes the short circuit protector enabled. As a result the external discharge control Nch-MOS-FET turns to "off" with the D_{OUT} pin being at "L".

*An output delay time for the excess current detector is internally fixed, 13ms TYP. at V_{DD}=3.0V. A quick recovery of V-pin level from a value between Vshort and V_{DET3} within the delay time keeps the discharge control FET staying "ON" state.

When the short circuit protector is enabled, the D_{OUT} would be "L" and its delay time would be 5μs TYP.

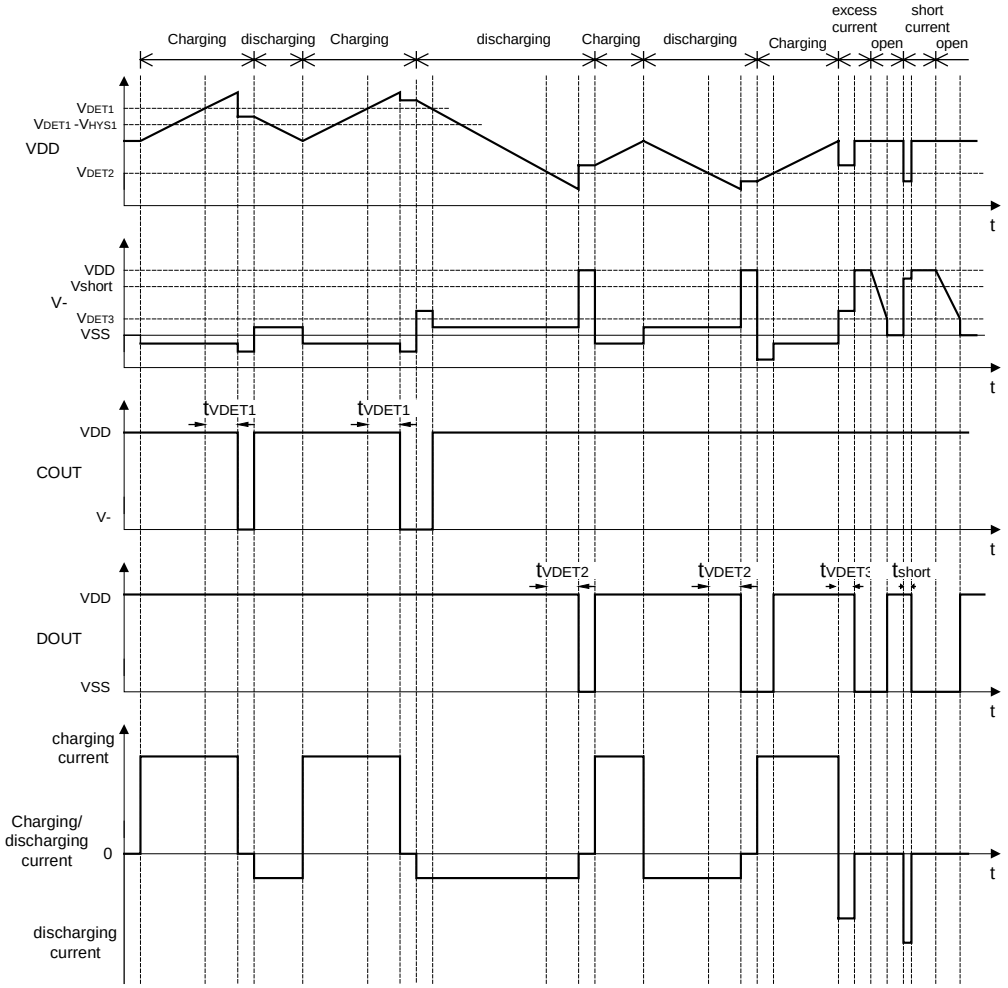
*The V-pin has a built-in pull down resistor, TYP.100KΩ, connected to the V_{SS} pin.

After an excess current or short circuit protection is detected, removing a cause of excess current or external short circuit makes an external discharge control Nch-MOS-FET to an "on" state automatically with the V-pin level being down to the V_{SS} level through the built-in pull down resistor.

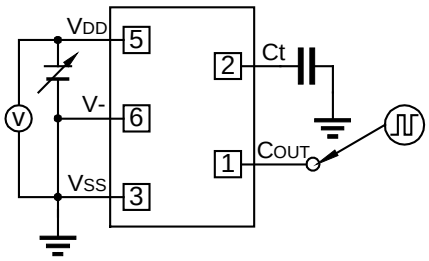
* When V_{DD} voltage is higher than V_{DET2} at a time when the excess current is detected the SC451XX does not enter a standby mode, while V_{DD} voltage is lower than V_{DET2} the SC451XX enters a standby mode.

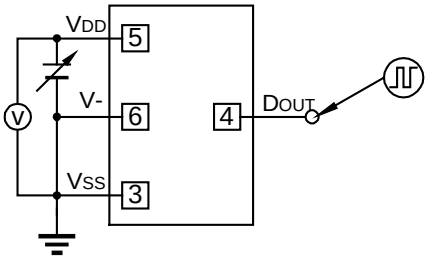
After detecting short circuit the SC451XX will not enter a standby mode.

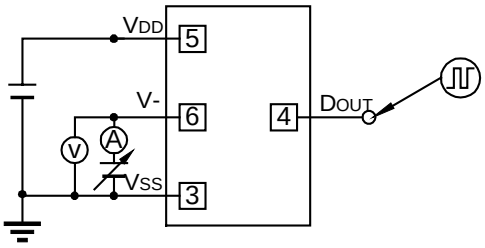
TIMING DIAGRAM

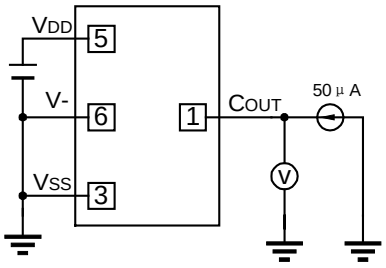


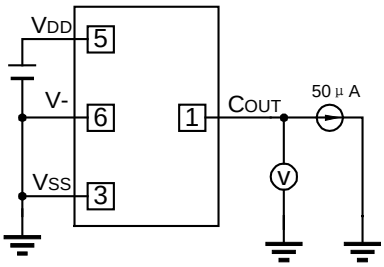
TEST CIRCUITS

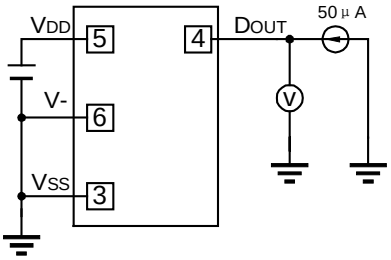












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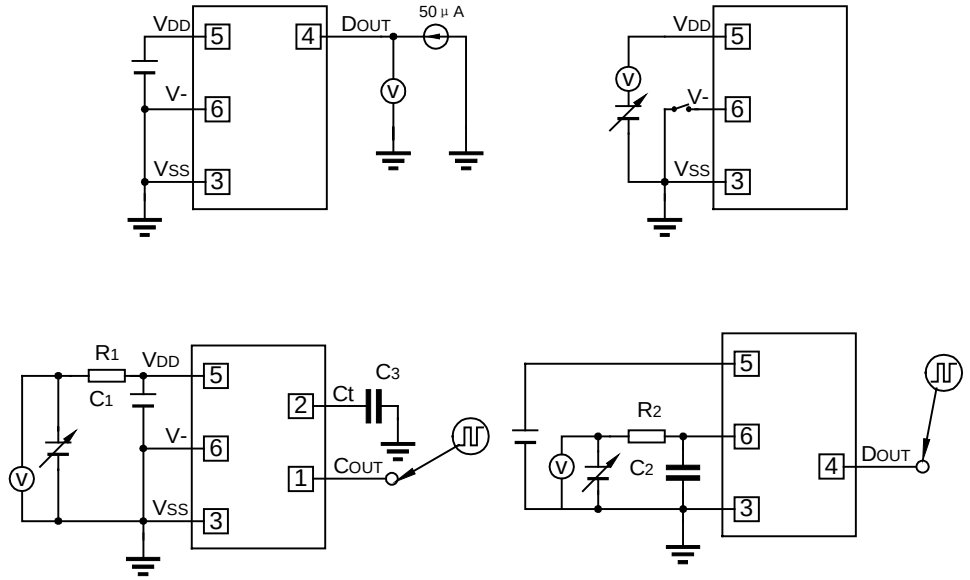
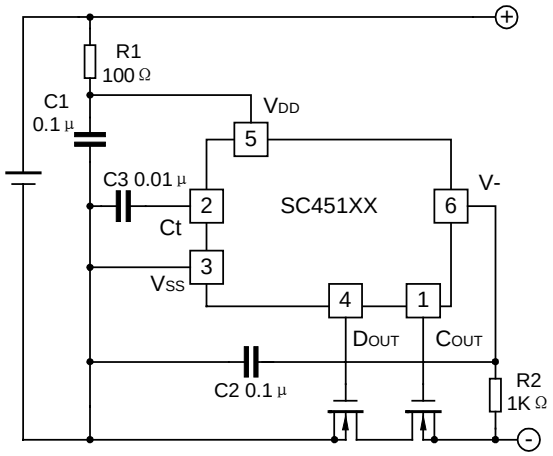
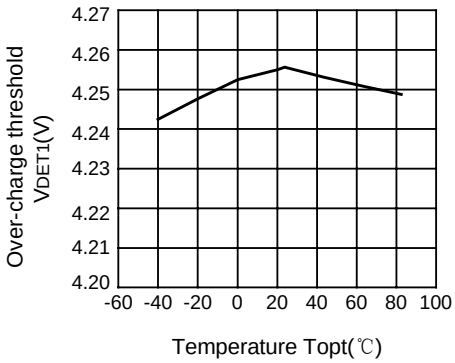
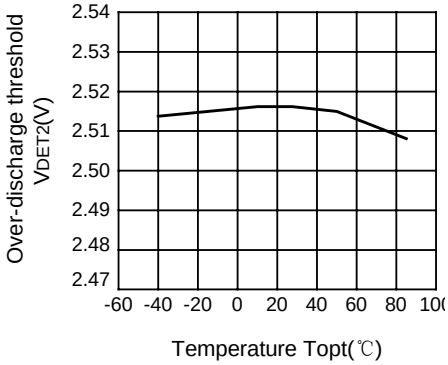


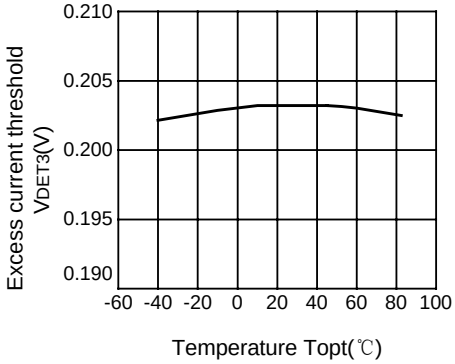
TYPICAL APPLICATION CIRCUITS

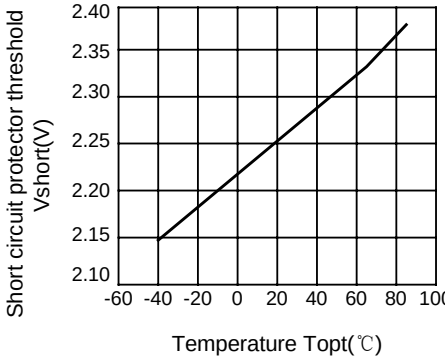


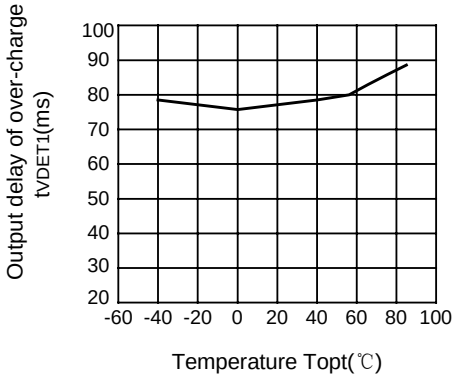
TYPICAL PERFORMANCE CHARACTERISTICS

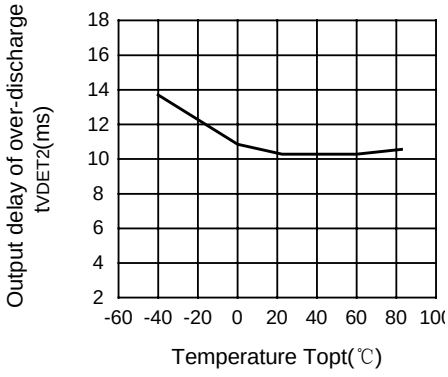




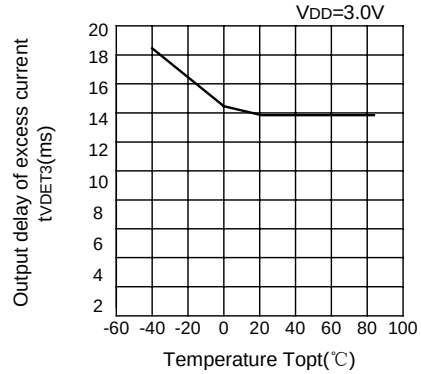


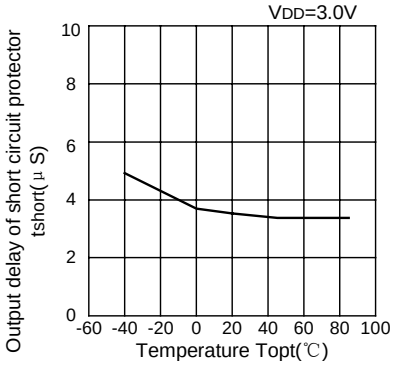


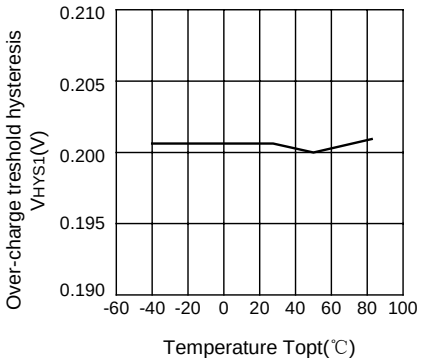


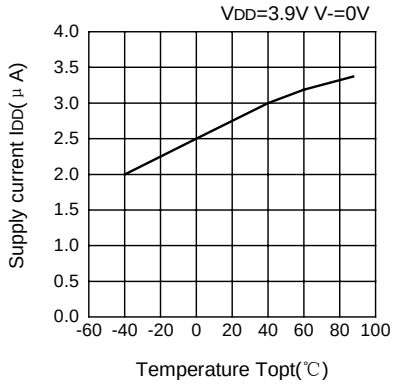


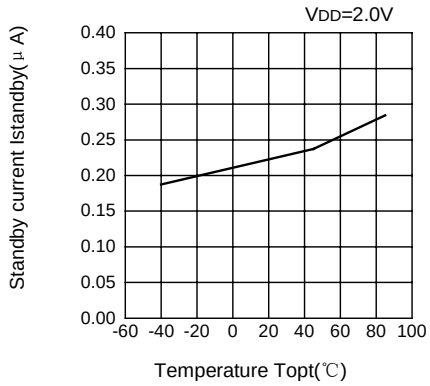
TYPICAL PERFORMANCE CHARACTERISTICS (continued)











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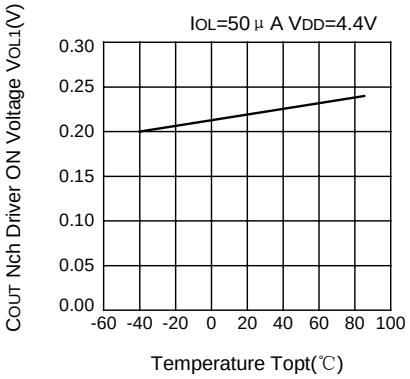
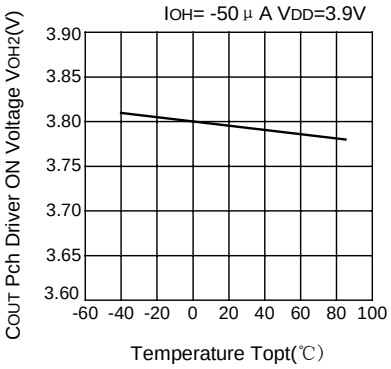
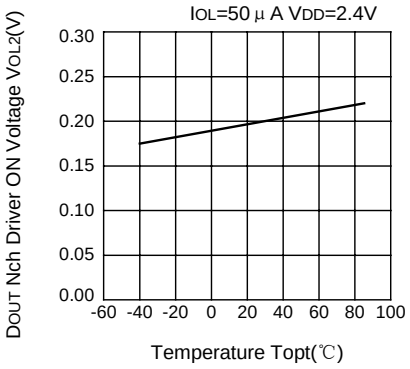
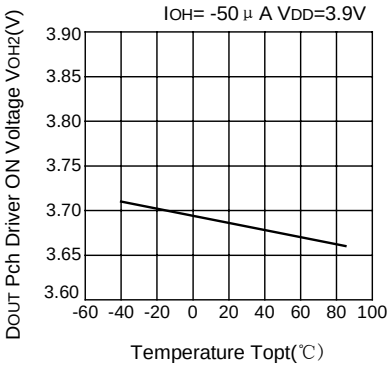
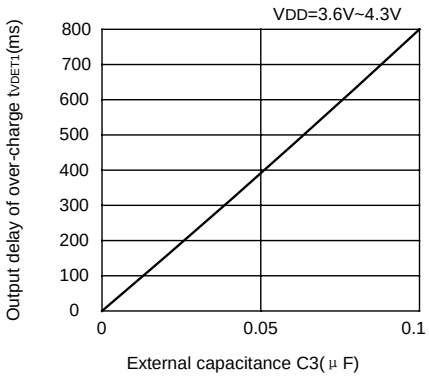


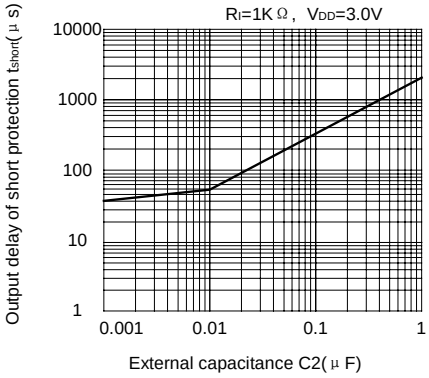


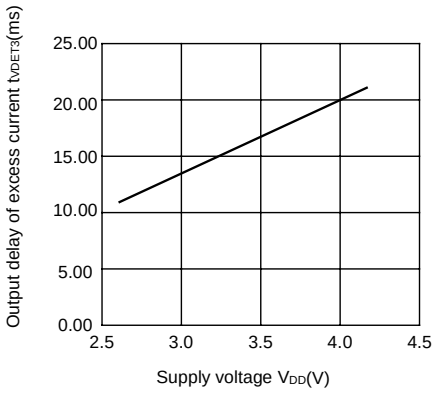


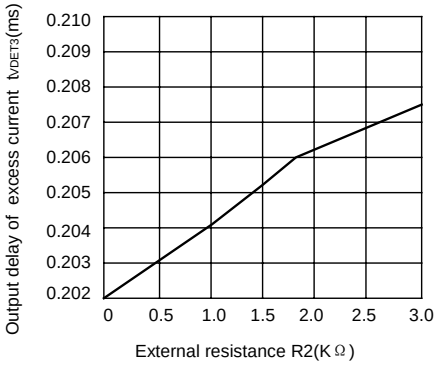


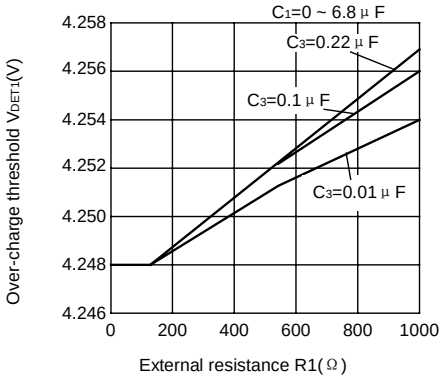
TYPICAL PERFORMANCE CHARACTERISTICS (continued)











PACKAGE OUTLINE

SOT-26 UNIT: mm