SEMTECH INTERNATIONAL AG

SC452
Dual-Phase Single Chip IMVP-6 Vcore Power Supply

POWER MANAGEMENT

Description

The SC452 is a single chip high-performance PWM controller designed to power advanced IMVP-6™ processors. On-chip support is provided for all of the IMVP-6 requirements, including Active Voltage Positioning, Geyserville-3 VID transitions, VID-controlled Deeper Sleep voltage setting, PSI# and DPRSL control, fast/slow C4 exit, and default Boot voltage.

The SC452 implements hysteretic control technology which provides the fastest possible transient response while avoiding the stability issues inherent to classical PWM controllers. Semtech's proprietary Combi-Sense® technology provides a loss-less current sensing scheme which is extremely robust and easy to lay out. Eliminating the sense resistors reduces costs and PCB area, plus increases system efficiency. Integrated SmartDriver™ technology initially turns on the high side driver with 'soft' drive to reduce ringing, EMI, and capacitive turn-on of the low side MOSFET, while also increasing overall efficiency.

Hysteretic operation adaptively reduces the SC452 switching frequency at light loads. Combined with an automatic "power-save" mode which prevents negative current flow in the low-side FET, system efficiency is significantly enhanced during light loading conditions. The SC452 changes from dual-phase to single-phase operation whenever PSI# asserts, providing optimal efficiency across the entire power range.

A 7-bit DAC, accurate to 0.85%, sets the output voltage reference, and implements the 0.300V to 1.500V range required by the processor. The DAC slew rate is externally programmed to minimize transient currents and audible noise. True differential remote sensing provides accurate point-of-load regulation at the processor die. Other features include programmable soft-start, open-drain IMVP6_PWRGD and CLKEN# outputs, dynamic current sharing, over-voltage and programmable over-current protection. The SC452 is available in a space-saving 44 pin MLP package.

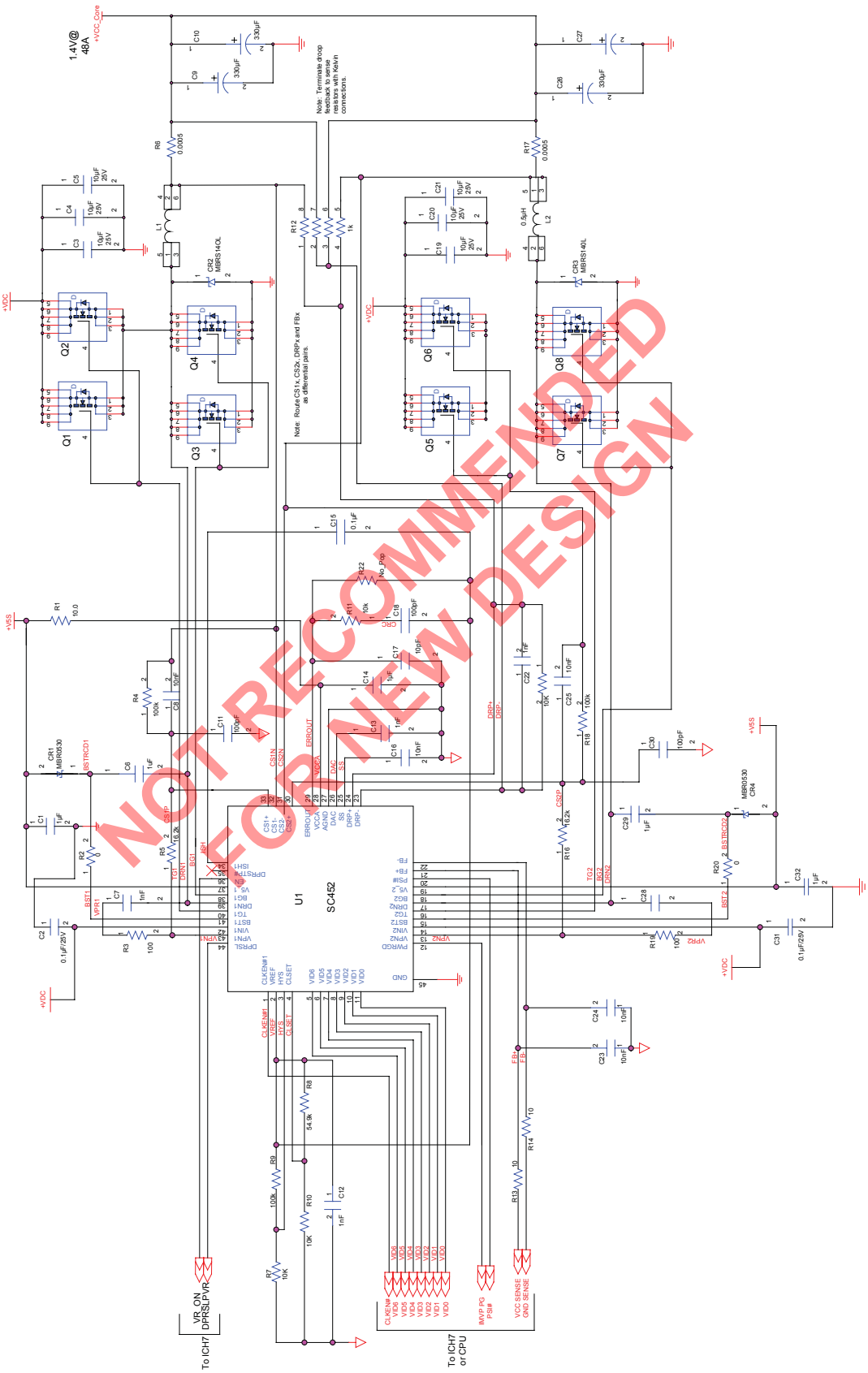
Features

- Dual-Phase Solution with Integrated Drivers
- Hysteretic Control for Fast Transient Response
- Combi-Sense Provides Loss-Less Current Sensing
- Dynamic Current Sharing
- Active Voltage Positioning
- True Differential Remote (die) Sensing
- On-Chip Support for all IMVP-6 Power Management Features
- VID Programmed Deeper Sleep Voltage
- Fast/Slow C4E Break-Event Support
- Clock Enable (CLKEN#) Output
- Delayed Power Good Signal with Blanking
- Programmable Soft-Start and DAC Slew Control
- Programmable OCP Threshold
- Supports all Ceramic Decoupling Solutions
- 44 pin MLP (7x7)
- Lead-free Package

Applications

- IMVP-6/6+ Notebook PCs
- Embedded Applications
- Graphics and Other Processor Cores

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Condition	Min	Max	Units
Supply Voltages VCCA V5_1, V5_2		-0.3	6.5	V
BST1, BST2 to PGND	Static	-0.3	30	V
	Transient <100ns	-0.3	34	V
BST1, BST2 to DRN1, DRN2		-0.3	6	V
DRN1, DRN2 to PGND	Static	-2	25	V
	Transient <100ns	-5	29	V
TG1, TG2 to PGND		DRN 1, 2-0.3	BST1, 2+0.3	V
BG1, BG2 to PGND		-0.3	V5_1, 2+0.3	V
VIN1, VIN2 to PGND		-0.3	25	V
VPN1, VPN2 to PGND		-0.3	VIN1, 2+0.3	V
PGND to AGND		-0.3	0.3	V
All other pins to AGND		-0.3	VCCA+0.3	V
Thermal Resistance Junction to Ambient	θ_{JA}		21	°C/W
Operating Junction Temperature Range	T_J	-40	125	°C
Storage Temperature Range	T_{STG}	-65	150	°C
Peak IR Reflow (10-40sec)	$T_{IRreflow}$		260	°C
ESD Rating (Human Body Model)	V_{ESD}		2	kV

Electrical Characteristics

Unless otherwise specified, VccA = V5_1 = V5_2 =5 V. -40<T_J<+125°C.

Parameter	Condition	Min	Typ	Max	Units
Supplies (VccA, V5_1, V5_2)					
VccA,V5_1, V5_2 Operating Range		4.5	5.0	5.5	V
V_{BAT} Operating Range		4.5		24	V
VccA, V5_2 UVLO	Rising	4.25	4.4	4.5	V
	Hysteresis Falling	50	150	250	mV
VccA Current	Disabled			10	µA
	In UVLO		0.6	1.0	mA
	Operating (Static)	5	10	15	mA

Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
Supplies (VccA, V5_1, V5_2) (Cont.)					
VccA Operating Current	Operating (Deeper Sleep)		8	12	mA
V5_1 Current	Disabled			10	µA
	In UVLO			10	µA
	Operating, Static, TG1 Low	0.3	0.9	1.2	mA
V5_2 Current	Disabled			10	µA
	In ULVO		120	200	µA
	Operating, Static, TG2 Low	0.3	0.9	1.2	mA
Vin1 and Vin2 Current	Static TG when respective TG Low		500		µA
	Static TG when respective TG High		900		µA
	When in Powersave		0		µA
Logic Inputs (EN, VID[6:0], DPRSLP, DPRSTP#, PSI#)					
Enable Threshold		0.8		2.0	V
VID[6:0], DRPSLP, DPRSTP, PSI# Threshold		0.45		0.65	V
Input Impedance			40		kΩ
Reference (DAC, SS, VREF), (0 < T_J <85°C)					
DAC Error + Internal Offset	1.5000V - 0.7625V	-0.85		+0.85	%
	0.75V - 0.50V	-7		7	mV
	0.4875 - 0.30V	-14		14	mV
DAC Sink/Source Ability	0.3V < DAC <1.5V	|50|			µA
SS Slew Current	Start-Up	8	12	16	µA
	Operating	102	120	138	µA
	Slow DPRSLP Exit (x = operating ISS)	x/6	x/5	x/4	
	Discharge (SS = 0.5V)	15			mA
SS Discharge Threshold			50	100	mV
Boot Voltage		1.176	1.2	1.224	V
Boot Delay(1)		10	30	100	us
VREF Accuracy		1.97	2.00	2.03	V
VREF Sink/Source Ability		|1.5|			mA

Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Units
Remote Sense (FB+, FB-)					
Input Impedance			14		kΩ
Bandwidth(1)		2			MHz
Droop (DRP+, DRP-)					
Input Bias Current				±1	µA
Gain	DRP+ = 1.5V, DRP- = 1.48V	9.5	10	10.5	V/V
Droop Input Offset	(25°C only)	-0.4	0	0.4	mV
	0 to 85°C	-0.5	0	0.5	mV
Maximum Input Signal(1)		20			mV
Bandwidth(1)		0.8			MHz
Error Amplifier (ERROUT)					
Gain			19		
Bandwidth(1)		2			MHz
Current Sensing (CS1+, CS1-, CS2+, CS2-, ISH)					
CS1, 2 + CS1, 2 Bias Currents	CS+ = CS- = 1.5V			±1	µA
CS Gain for Switching		5.4	6.0	6.6	V/V
Maximum Input Signal(1)		450			mV
CS Bandwidth(1)		2			MHz
Zero-Crossing Detector Offset		-6		6	mV
Low Pass Filter Corner Frequency(1)		50	80	125	kHz

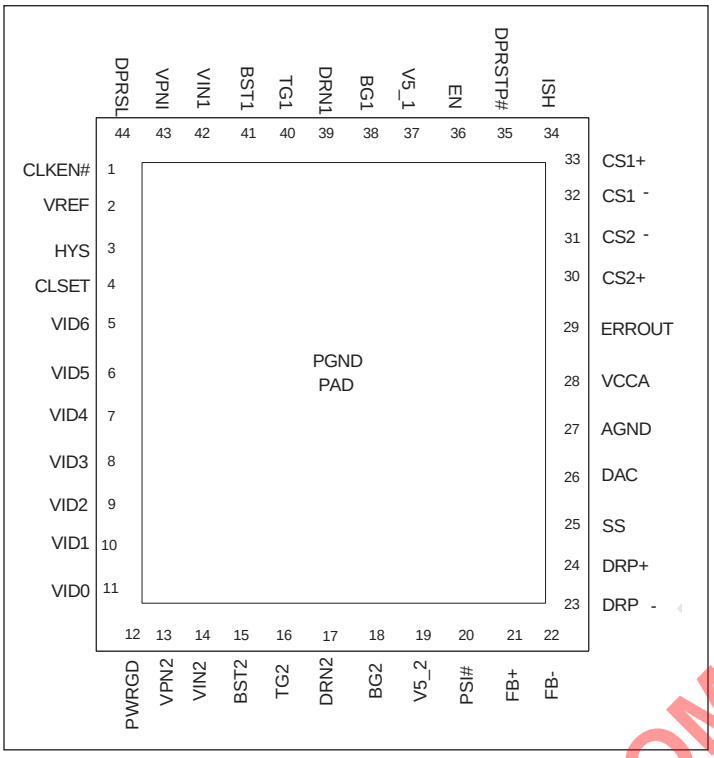
Electrical Characteristics (Cont.)

Parameter	Condition		Min	Typ	Max	Units
Current Sensing (CS1+, CS1-, CS2+, CS2-, ISH) (Cont.)						
Current Sharing Open Loop Gain			40	60	90	
Current Sharing Range (% relative to VHYS)			52	80	108	%
Current Sharing Offset			-3.0		+3.0	mV
Current Sharing Disable Threshold Relative to VccA	Voltage on ISH pin		-0.9		-0.35	V
Hysteresis Setting (HYS, CLSET)						
HYS, CLSET Input Bias Current					±1	µA
HYS Error (internal HYS difference from TG Hi to TG lo as a percentage of voltage applied at HYS pin)	HYS = 1V	Dual Phase	-24	-20	-16	%
		Single Phase	±36	±40	±44	%
CLSET Voltage (internal hysteresis setting relative to voltage applied at CLSET pin) CLSET = 1.2V	TG High		160	200	240	mV
	TG Low		128	160	192	mV
	Single Phase TG Low		90	120	150	mV
Powergood (CLKEN#, PWRGD)						
Leakage	CLKEN#, PWRGD High Impedance				1	µA
On Resistance	CLKEN#, PWRGD = 0.1V				100	Ω
PWRGD Start-Up Delay			3	6.5	10	ms
Fixed Over-Voltage Protection Threshold			1.75	1.8	1.85	V
Power Good Window Upper Threshold	FB Rising Relative DAC		+160	+200	+240	mV
Power Good Window Lower Threshold	FB Falling Relative DAC		-360	-300	-240	mV
Power Good Window Lower Hysteresis	FB Rising Relative DAC		30	50	90	mV

Electrical Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Unit
High-Side Driver (TG1, TG2, BST1, BST2, DRN1, DRN2)					
Peak Current(1,2)		1.75	2.0	2.25	A
On Resistance	R_{TG_UP}, DRN < 0.5V, 25°C	4.1	5.8	7.5	Ω
	R_{TG_UP}, DRN < 0.5V, -40 to 125°C	3.48	5.8	9.24	Ω
	R_{TG_UP}, DRN > 0.5V, 25°C	0.9	1.3	1.7	Ω
	R_{TG_UP}, DRN > 0.5V, -40 to 125°C	0.76	1.3	2.1	Ω
	R_{TG_DN}, 25°C	0.42	0.6	0.78	Ω
	R_{TG_DN}, -40 to 125°C	0.34	0.6	1.01	Ω
Rise Time (1,2)	CTG = 3nF	17	22	27	ns
Fall Time (1,2)	CTG = 3nF	9	12	15	ns
Propagation Delay (1,2)	From Hysteretic Comparator Inputs to Driver Output	30	45	60	ns
Shoot-Thru Protection Delay (1)		10	20	30	ns
Low-Side Driver (BG1, BG2, V5_1, V5_2, PGND1, PGND2)					
Peak Current(1, 2)		3.5	4.0	4.5	A
On Resistance	R_{BG_UP} at 25°C	0.9	1.3	1.7	Ω
	R_{BG_UP} at -40 to 125°C	0.76	1.3	2.1	Ω
	R_{BG_DN} at 25°C	0.35	0.5	0.65	Ω
	R_{BG_DN} at -40 to 125°C	0.28	0.5	0.86	Ω
Rise Time(1, 2)	C_{BG} = 3nF	5	7	9	ns
Fall Time(1, 2)	C_{BG} = 3nF	2.5	3.5	4.5	ns
VPN (VPN1, VPN2, VIN1, VIN2)					
Tri-State Leakage		-600		600	nA
On Resistance	Source	100	200	400	Ω
	Sink	100	200	400	Ω
Propagation Delay(1, 2)	From Hysteretic Comparator Inputs to Driver Output	30	45	60	ns

Pin Configuration



Ordering Information

Device[2]	Package[1]	Temp Range (T_J)[3]
SC452IMLTRT	MLP-44	-40°C to +125°C
SC452EVB	Evaluation Board	

Notes:
1) Only available in tape and reel packaging. A reel contains 3000 devices.

2) This device is ESD sensitive. Use of standard ESD handling precautions is required.

3) Lead-free package compliant with J-STD-020B. Qualified to support maximum IR Reflow temperature of 260°C for 30 seconds. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Description
1	CLKEN#	Start Clock Indicator - open drain output. Active low.
2	VREF	Internal reference voltage (2V). Bypass to AGND with a 1nF capacitor.
3	HYS	Core comparator hysteresis. A resistor divider on this pin sets the hysteresis voltage.
4	CLSET	Current Limit Set. A resistor divider on this pin sets the OCP threshold.
5	VID6	VID MSB.
6	VID5	
7	VID4	
8	VID3	
9	VID2	
10	VID1	
11	VID0	VID LSB.
12	IMVP6_PWRGD	IMVP6 Power Good - open drain output.

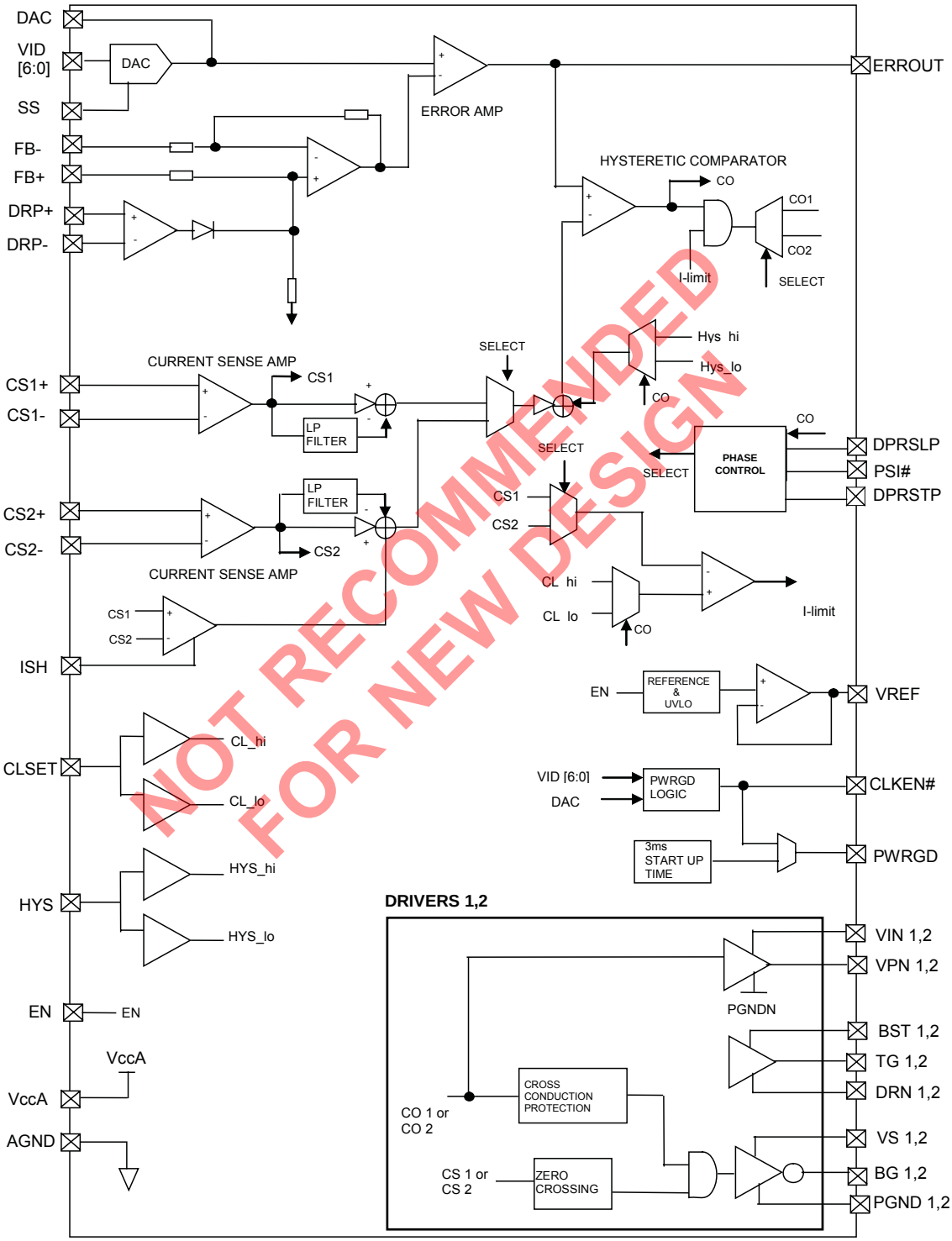
Pin Descriptions (Cont.)

Pin #	Pin Name	Pin Description
13	VPN2	Virtual Phase Node for Phase 2. Connect an RC between this pin and the output sense point to enable Combi-Sense operation.
14	VIN2	Input power to the DC-DC converter. Used as supply reference for internal Phase 2 Combi-Sense circuitry.
15	BST2	Phase 2 Bootstrap pin. A capacitor is connected between BST and DRN to develop the floating voltage for the high-side MOSFET.
16	TG2	Phase 2 output drive for the top (switching) MOSFET.
17	DRN2	This pin connects to the junction of the Phase 2 switching and synchronous MOSFETs . This pin can be subjected to a -2V minimum relative to PGND without affecting operation.
18	BG2	Phase 2 output drive signal for the bottom (synchronous) MOSFET.
19	V5_2	Input supply for Phase 2 low-side gate drive. Connect to 5V.
20	PSI#	Platform PSI-2 control signal.
21	FB+	Remote die sense of core voltage. Connect to V_{CC_SENSE} at the CPU socket.
22	FB-	Remote GND sense. Connect to V_{SS_SENSE} at the CPU socket.
23	DRP-	Inverting input to droop amplifier.
24	DRP+	Non-inverting input to droop amplifier.
25	SS	Soft-start. An external cap at this pin defines the soft-start ramp.
26	DAC	DAC output. An external cap at this pin defines VID transition timing.
27	AGND	Analog ground.
28	VCCA	IC supply. Connect to 5V.
29	ERROUT	Error Amplifier Compensation Pin.
30	CS2+	Non-inverting input to Phase 2 Combi-Sense amplifier.
31	CS2-	Inverting input to Phase 2 Combi-Sense amplifier.
32	CS1-	Inverting input to Phase 1 Combi-Sense amplifier.
33	CS1+	Non-inverting input to Phase 1 Combi-Sense amplifier.
34	ISH	Used for compensation of the ISHARE amplifier.
35	DPRSTP#	DPRSTP# control pin for fast/slow C4E event. Active high.
36	EN	Enable control. Active High.
37	V5_1	Input supply for Phase 1 low-side gate drive. Connect to 5V.

Pin Descriptions (Cont.)

Pin #	Pin Name	Pin Description
38	BG1	Phase 1 output drive signal for the bottom (synchronous) MOSFET.
39	DRN1	This pin connects to the junction of the Phase 1 switching and synchronous MOSFETs . This pin can be subjected to a -2V minimum relative to PGND without affecting operation.
40	TG1	Phase 1 output drive for the top (switching) MOSFET.
41	BST1	Phase 1 Bootstrap pin. A capacitor is connected between BST and DRN to develop the floating voltage for the high-side MOSFET.
42	VIN1	Input power to the DC-DC converter. Used as supply reference for internal Phase 1 Combi-Sense circuitry.
43	VPN1	Virtual Phase Node for Phase 1. Connect an RC between this pin and the output sense point to enable Combi-Sense operation.
44	DPRSL	Deeper Sleep control pin. Active high.
PAD	PGND	Power Ground for Drivers 1 and 2. Pad must be soldered to Power Ground plane.

Block Diagram



Applications Information

INTRODUCTION:

The SC452 is a new generation of hysteretic converter which combines the best features of Semtech's hysteretic converter technology with the benefits of Semtech's patented Combi-Sense technology. The SC452 provides a complete solution to Intel's IMVP-6 requirements.

In the SC452, the ripple for the hysteretic switching control is provided by Combi-Sense current feedback. This provides several advantages over plain voltage-mode hysteretic converters, and other topologies such as constant on-time which switch on voltage ripple.

• No minimum amount of output ripple is required so there are no controller-induced limits on capacitor value or ESR.

• No current sense resistors are required, resulting in higher converter efficiency.

• The large signal magnitude afforded by Combi-Sense (4-5 times that of inductor DCR current sensing) makes the layout much less sensitive to noise.

• Full differential feedback of the output voltage from the CPU die is enabled.

Because the basic control is hysteretic, the SC452 provides the fastest possible transient response without switching at very high frequencies. This results in higher efficiency with less expensive parts because switching losses are reduced. Only the Combi-Sense ripple is used for the regulation loop, so the load-line accuracy is not affected by tolerances in RDS(ON) or inductor DCR. However, because of the large signal magnitude, the DC is kept for the current limiting and current sharing functions.

Load-line control is provided by a dedicated droop amplifier with uncommitted inputs. This provides users with maximum flexibility, as the droop source can be any of the following:

- PCB copper trace
- Inductor DCR
- Sense resistor

Thus, customers can choose the amount of cost and performance they need for any given design.

The SC452 also provides a full range of features.

All IMVP-6/6+ functions are implemented:

- ¨ EN
- ¨ CLKEN#
- ¨ IMVP-6 PWRGD
- ¨ DPRSLPVR
- ¨ DPRSTP#
- ¨ PSI#
- ¨ Geyserville-3 VID changes
- ¨ Fast-C4 Exit
- ¨ All '1s' soft-OFF state

- A 2.00V voltage reference is provided
- Separate hysteresis and current limit settings
- A full suite of protection features is provided:
  - ¨ Over-current protection (OCP)
  - ¨ Fixed and DAC-referenced over-voltage protection (OVP)
  - ¨ Over-temperature protection (OTP)
  - ¨ Undervoltage detection via PWRGD

All protection features are latching, and are either reset by recycling power or toggling the EN signal.

THEORY OF OPERATION

Voltage Regulation:

Referring to the block diagram on the preceding page, the hysteretic comparator is the heart of the converter. The "+" input corresponds roughly to the CMPREF node of our older generations of IC; the "-" input is similar to CMP. In order to regulate, the hysteretic comparator needs the following information:

- DAC (reference) voltage
- Droop voltage proportional to IOUT
- Feedback voltage
- Hysteresis voltage
- Hysteresis ripple

Applications Information (Cont.)

CMPREF receives the reference, voltage feedback and droop information. The reference is produced by the integrated seven-bit DAC. The feedback voltage is received by the full differential amplifier from the CPU socket. The droop amplifier reduces the voltage at the "+" node of the differential amplifier as the output current increases to produce the required linear load line. A third amplifier, labeled the "Error Amplifier", multiplies the difference between the "ideal" voltage (DAC minus droop) and the actual voltage (FB+ minus FB-) for faster response. This signal is the reference for the hysteretic comparator.

CMP has the ripple signal derived from the Combi-Sense inputs plus the hysteresis signal. The DC is stripped from the ripple signals by the combination of low-pass filter and summing amplifiers. Phase 2 has a current sharing input derived from an averaged difference between the two phases. The ripple inputs are fed to a summing block via a multiplexer which is synchronized to the active phase with the select output. The hysteresis signal is added at the summing block. The hysteresis voltage is set directly by the resistor divider from the 2V REF output.

The figure on Page 14 illustrates the basic switching control. Starting with the Select line (top plot, green trace) on Phase 2, and both CO signals low. Accordingly, both bottom gate (BG) signals are on and the inductor currents in both phases are discharging as shown by the Phase 1 (orange) and Phase 2 (blue) ripple signals in the lower plot.

When CMP discharges to CMPREF, the select line toggles, CO1 turns on, and subtracts V(hys_hi) from CMP. CO1 remains high until CMP again charges to CMPREF. Then, CO1 switches low, adding V(hys_lo) to CMP. This state is held until CMP again discharges to CMPREF. Then, the select line toggles, CO2 turns on, and the cycle repeats.

In Dual Phase mode, V(hys_lo) is zero; CO of the initial phase remains low while the alternate phase is in control, so BG of the initial phase remains on through the alternate cycle and, as a result, the second phase will terminate at approximately -V(hys). During single phase operation, V(hys_lo) = -V(hys).

Current Limit Regulation:

In Current Limit, the voltage hysteretic converter is overridden by the current limit hysteretic comparator, and the TG pulse is terminated when the output of the current sense amplifier reaches the CL_hi threshold and BG is terminated at the CL_lo threshold. These thresholds are set from the CLSET resistor divider:

CL_hi = 0.33 * V(clset)
CL_lo = 0.20 * V(clset)

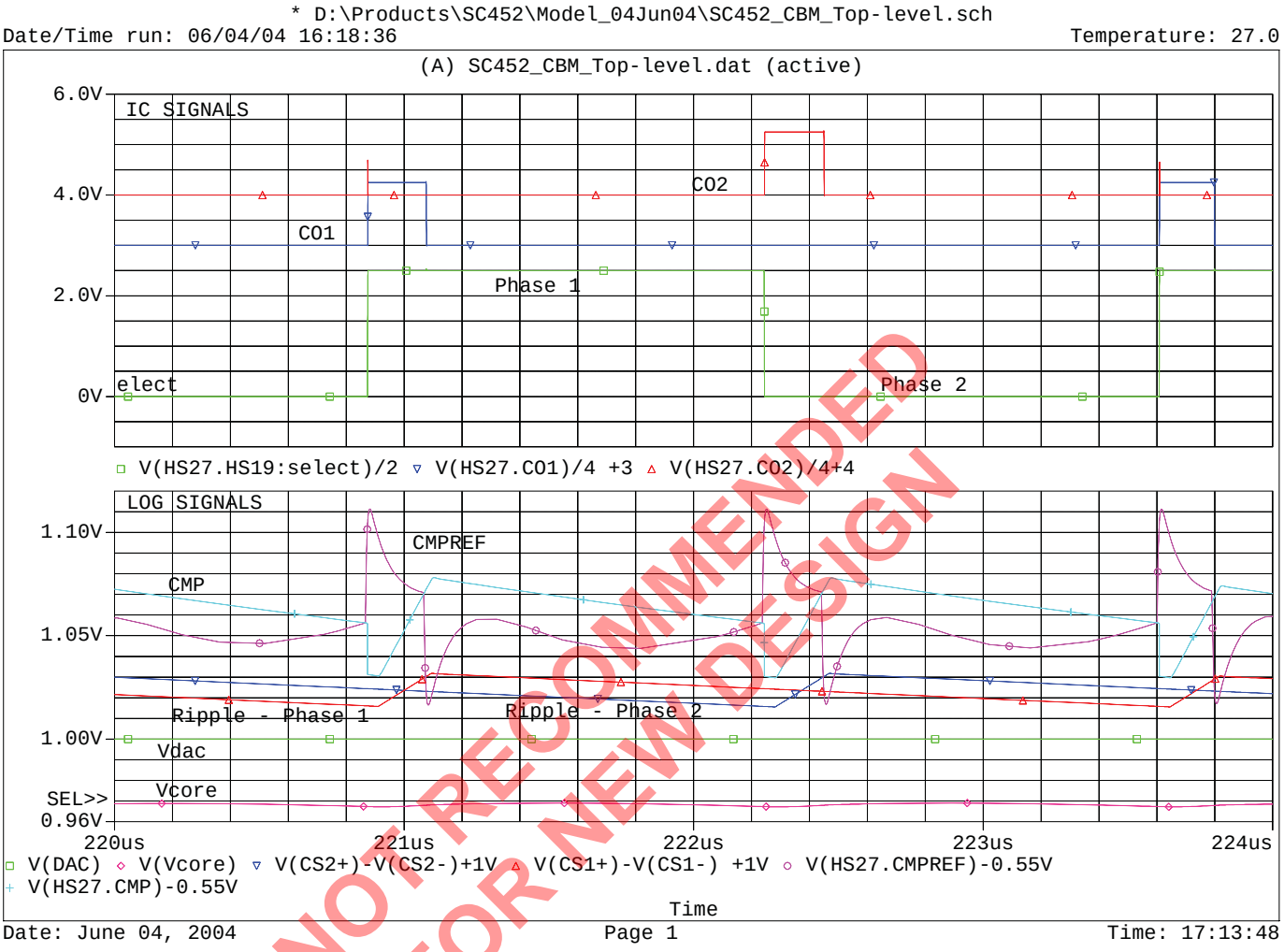
Current limit pulses continue until 32 pulses after the voltage droops to the PWRGD low threshold; then the controller latches off. This current limit algorithm has been used in several generations of IMVP controllers and have been proven to be extremely robust.

Start-Up and Shut-Down Sequences:

For the SC452 to start up, VCCA, V5_1, and V5_2 must reach their under-voltage lockout (UVLO) thresholds (4.4V typ.) then the EN signal goes high. The DAC drives 12µA (typ.) into the soft-start capacitor on the SS pin. The SS and DAC pins rise slowly until the BOOT voltage (1.2V, fixed internally) is reached. The controller remains at BOOT voltage for ~30µs. At the end of the BOOT interval, the VID(6:0) lines are considered valid and CLKEN# is driven low. The controller will slew at a 120µA rate to the VID-defined value. Approximately 6ms after the voltage hits the PWRGD threshold, IMVP-6_PWRGD goes high, and start-up is complete.

In a normal shutdown, the EN signal is driven low, the TG and BG signals are driven low, tri-stating the power chains. An approximately 100Ω resistor on the FB+ signal discharges Vcore slowly and prevents normal amounts of leakage from pulling Vcore high. The DAC and other internal circuitry is shut down, entering a very low power (<10µA typical) state. A UVLO will also result in this type of shutdown.

Applications Information (Cont.)



Applications Information (Cont.)

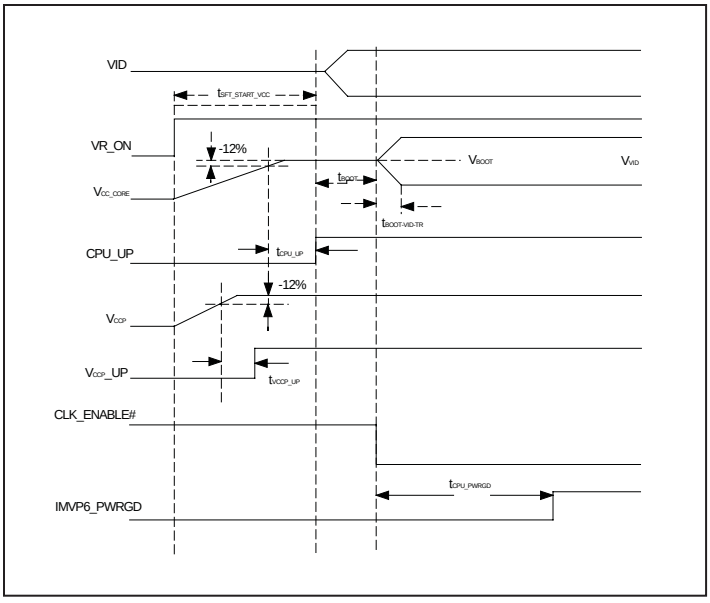


Figure A - Power On Sequencing Timing Diagram

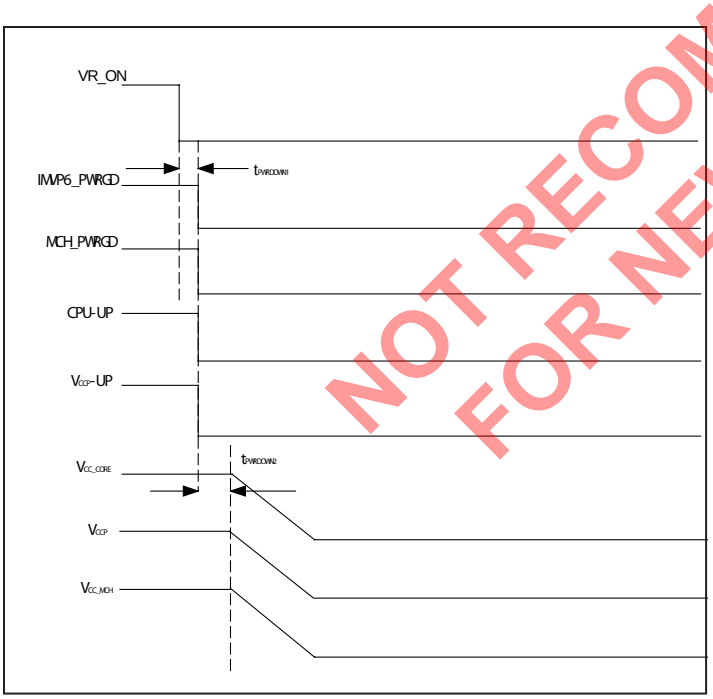


Figure B - Power Off Sequencing Timing Diagram

DPRSL	PSI#	Status	Load	SC452 Mode
1	0	Deeper Sleep	Icc < 3A	1-phase
1	1	Deeper Sleep	Icc > 3A	1-phase
0	0	Active; Med. Power Potential	9A < Icc <16A	1-phase
0	1	Active; Full Power Potential	Icc > 15A	2-phase

Response to Power Control Inputs:

Besides the EN signal, described on Page 13, the SC452 reacts to the other control signals in the following manner:

The SC452 always operates with discontinuous mode power saving enabled, always saving power at light load regardless of the status of DPRSL or PSI#. PSI# signal is used to indicate the expected max level of currents demanded from IMVP6. In essence, as DPRSTP# (DPRSLPVR) indicates a voltage demand, PSI# indicates a current demand. PSI# signal can be asserted during active (LFM to HFM) execution. The purpose is to command the voltage regulator to maximize its efficiency through the widest range of current loads, (i.e., DeeperSleep to HFM).

PSI# transitions no longer occurs during Deeper Sleep mode. While in active mode, it is expected that PSI# signal toggle occurs at the same Vcc-core voltage level VID. The reason to have same VID voltage requirement is that the superimposed charge current required to charge the output decoupling to a new level of voltage can overcome single phase mode of operation (if used), during positive dv/dt events (such as Enhanced Intel SpeedStep® or Deeper Sleep exit).

Applications Information (Cont.)

In active mode, enhanced Intel SpeedStep transitions can occur. SC452 can recognize a step-up in voltage transition and revert operation to full power mode to supply the bulk capacitor charge currents superimposed on the processor active mode current. During Deeper Sleep, PSI# indicates a very low current state. Regulator can enter asynchronous mode of operation. In rare occasions, if the PSI# is deasserted during Deeper Sleep, this is an indication of a high leakage component that may not benefit from asynchronous operation.

In the Deeper Sleep state, SC452 recognizes Deeper Sleep exit state and its associated voltage transitions and reverts operation to full power mode to allow for the bulk capacitor charge currents to superimpose with the processor active mode current.

A +/-0.85% 7-bit digital-to-analog converter (DAC) serves as the programmable reference source of the Core Comparator. Programming is accomplished by logic voltage levels applied to the DAC inputs. The VID code vs. The DAC output is shown in the tables below. There are 7 voltage identification pins on mobile processor. These signals can be used to support automatic selection of Vcc_core voltages.

They are needed to cleanly support voltage specification variations on current and future processors. VID [6:0] are defined in the table below. The VID [6:0] signals are 0V to Vccp CMOS level inputs. These signals are not to be pulled up externally as this will damage the processor.

Applications Information (Cont.)

Table 1.
VID vs. VCC_CORE Voltage (Active Mode)

VID							V_{DAC}	VID							V_{DAC}
6	5	4	3	2	1	0	V	6	5	4	3	2	1	0	V
0	0	0	0	0	0	0	1.5000	0	0	1	0	1	0	0	1.2500
0	0	0	0	0	0	1	1.4875	0	0	1	0	1	0	1	1.2375
0	0	0	0	0	1	0	1.4750	0	0	1	0	1	1	0	1.2250
0	0	0	0	0	1	1	1.4625	0	0	1	0	1	1	1	1.2125
0	0	0	0	1	0	0	1.4500	0	0	1	1	0	0	0	1.2000
0	0	0	0	1	0	1	1.4375	0	0	1	1	0	0	1	1.1875
0	0	0	0	1	1	0	1.4250	0	0	1	1	0	1	0	1.1750
0	0	0	0	1	1	1	1.4125	0	0	1	1	0	1	1	1.1625
0	0	0	1	0	0	0	1.4000	0	0	1	1	1	0	0	1.1500
0	0	0	1	0	0	1	1.3875	0	0	1	1	1	0	1	1.1375
0	0	0	1	0	1	0	1.3750	0	0	1	1	1	1	0	1.1250
0	0	0	1	0	1	1	1.3625	0	0	1	1	1	1	1	1.1125
0	0	0	1	1	0	0	1.3500	0	1	0	0	0	0	0	1.1100
0	0	0	1	1	0	1	1.3375	0	1	0	0	0	0	1	1.0875
0	0	0	1	1	1	0	1.3250	0	1	0	0	0	1	0	1.0750
0	0	0	1	1	1	1	1.3125	0	1	0	0	0	1	1	1.0625
0	0	1	0	0	0	0	1.3000	0	1	0	0	1	0	0	1.0500
0	0	1	0	0	0	1	1.2875	0	1	0	0	1	0	1	1.0375
0	0	1	0	0	1	0	1.2750	0	1	0	0	1	1	0	1.0250
0	0	1	0	0	1	1	1.2625	0	1	0	0	1	1	1	1.0125

Table 1 - reflects VID codes to be used in Active state. The voltages represented cover HFM through LFM.

Table 2.
VID vs. VCC_CORE Voltage
(Active Mode/Deeper Sleep Dual Mode Region)

VID							V_{DAC}	VID							V_{DAC}
6	5	4	3	2	1	0	V	6	5	4	3	2	1	0	V
0	1	0	1	0	0	0	1.0000	0	1	1	1	1	0	0	0.7500
0	1	0	1	0	0	1	0.9875	0	1	1	1	1	0	1	0.7375
0	1	0	1	0	1	0	0.9750	0	1	1	1	1	1	0	0.7250
0	1	0	1	0	1	1	0.9625	0	1	1	1	1	1	1	0.7125
0	1	0	1	1	0	0	0.9500	1	0	0	0	0	0	0	0.7000
0	1	0	1	1	0	1	0.9375	1	0	0	0	0	0	1	0.6875
0	1	0	1	1	1	0	0.9250	1	0	0	0	0	1	0	0.6750
0	1	0	1	1	1	1	0.9125	1	0	0	0	0	1	1	0.6625
0	1	1	0	0	0	0	0.9000	1	0	0	0	1	0	0	0.6500
0	1	1	0	0	0	1	0.8875	1	0	0	0	1	0	1	0.6375
0	1	1	0	0	1	0	0.8750	1	0	0	0	1	1	0	0.6250
0	1	1	0	0	1	1	0.8625	1	0	0	0	1	1	1	0.6125
0	1	1	0	1	0	0	0.8500	1	0	0	1	0	0	0	0.6000
0	1	1	0	1	0	1	0.8375	1	0	0	1	0	0	1	0.5875
0	1	1	0	1	1	0	0.8250	1	0	0	1	0	1	0	0.5750
0	1	1	0	1	1	1	0.8125	1	0	0	1	0	1	1	0.5625
0	1	1	1	0	0	0	0.8000	1	0	0	1	1	0	0	0.5500
0	1	1	1	0	0	1	0.7875	1	0	0	1	1	0	1	0.5375
0	1	1	1	0	1	0	0.7750	1	0	0	1	1	1	0	0.5250
0	1	1	1	0	1	1	0.7625	1	0	0	1	1	1	1	0.5125
								1	0	1	0	0	0	0	0.5000

Table 2 - reflects VID codes to be used for both Active and Deeper Sleep states.

Applications Information (Cont.)

Table 3.
VID vs. VCC_CORE Voltage (Deeper Sleep/ Extended Deeper Sleep Dual Mode Region)

VID							V_{DAC}	VID							V_{DAC}
6	5	4	3	2	1	0	V	6	5	4	3	2	1	0	V
1	0	1	0	0	0	1	0.4875	1	0	1	1	0	1	0	0.3750
1	0	1	0	0	1	0	0.4750	1	0	1	1	0	1	1	0.3625
1	0	1	0	0	1	1	0.4625	1	0	1	1	1	0	0	0.3500
1	0	1	0	1	0	0	0.4500	1	0	1	1	1	0	1	0.3375
1	0	1	0	1	0	1	0.4375	1	0	1	1	1	1	0	0.3250
1	0	1	0	1	1	0	0.4250	1	0	1	1	1	1	1	0.3125
1	0	1	0	1	1	1	0.4125	1	1	0	0	0	0	0	0.3000
1	0	1	1	0	0	0	0.4000	1	1	1	1	1	1	1	OFF
1	0	1	1	0	0	1	0.3875								

Table 3 - reflects VID codes likely to represent Deeper Sleep and extended versions of Deeper Sleep State.

DAC Operation Below 0.3000V:

The SC452 responds to DAC codes corresponding to voltage values below 0.3V by producing voltages less than 0.3V; however, the tolerance of these signals is not specified or guaranteed. In the case of the '111 1111' VID code, the SC452 holds BGx and TGx low, preventing switching from occurring. In addition, a ~50Ω FET connected from VCORE to GND is turned on to prevent system leakage from charging up the VCORE rail.

DAC Slew Rate Control:

The DAC has integrated slew-rate control with multiple current settings to charge and discharge the soft-start capacitor. The slowest setting is used for soft-start, a medium setting for slow C4-exit (DPRSLVR='1', DPRSTP#='1') and a fast setting for all other VID transitions.

Power Supply Protection:

A UVLO circuit consists of a comparator that monitors the input supply voltage level, 5V. The SC452 is in UVLO mode when its supply voltage has not ramped above the upper threshold or has dropped below the lower threshold. The output of the UVLO comparator, gated with the ENABLE signal, turns on or off the internal bias, enables or disable the SC452 output, and initiates or resets the soft-start timer. If an UVLO occurs, a fault is set and SC452 is disabled until the system has shut down (and reapplied power), or the enable input signal to the SC452 has toggled states.

The OVP circuit of SC452 monitors the processor core VCC_CORE voltage for an over-voltage condition. If the FB voltage is 200mV greater than the DAC-Droop (i.e., out of the power good window), the SC452 will latch off and hold the low-side driver on permanently. Either the Power or EN must be recycled to clear the latch. The latch is disabled during soft-start and VID/DeeperSleep transitions. For safety, the latch is enabled if the FB voltage exceeds 1.8V even during VID/DeeperSleep transitions.

The device will be disabled and latched off when the internal junction temperature reaches approximately 160°C. Either the Power or EN must be recycled to clear the latch.

Applications Information (Cont.)

Design Procedure

(Based on SC452 R2 calculation with DCR Droop and R-Droop Method. In this design procedure, we are going to use the specifications required by the Intel's IMVP VI Napa Platform T&L (Yonah) Processor):

Important requirements and design constants are defined below:

$\Pi := 3.1415926$, $k := 10^{3}$, $M := 10^{6}$, $mil := 10^{-3}$

$p := 10^{-12}$, $n := 10^{-9}$, $\mu := 10^{-6}$

$V_{INMAX} := 20 \cdot V$

$V_{INMIN} := 10\ V$

$V_{INNOM} := 19 \cdot V$

$V_{HFM\_NL} := 1.2875\ V$

$I_{LKGMAX} := 1.6\ A$

$I_{HFM\_FL} := 36\ A$

$R_{IMVP} := -2.1 \frac{mV}{A}$

$V_{HFM\_FL} := V_{HFM\_NL} + R_{IMVP} \cdot I_{HFM\_FL}$

The required droop per phase at full load is:

$V_{DP} := \left| R_{IMVP} \right| \cdot I_{HFM\_FL}$

STEP 1: Output Inductor and Capacitor Selection

Output capacitance and ESR values are a function of transient requirements and output inductor value. Figure 1 illustrates the response of a hysteretic converter to a positive transient: In a hysteretic converter with adaptive voltage positioning, like the SC452, two conditions determine if you meet the positive transient requirements since there are no transient specifications in IMVP IV:

A: $ESR_{MAX} \le R_{IMVP}$

B: $V_{IMVP} \ge deltaV(C_{OUT})$

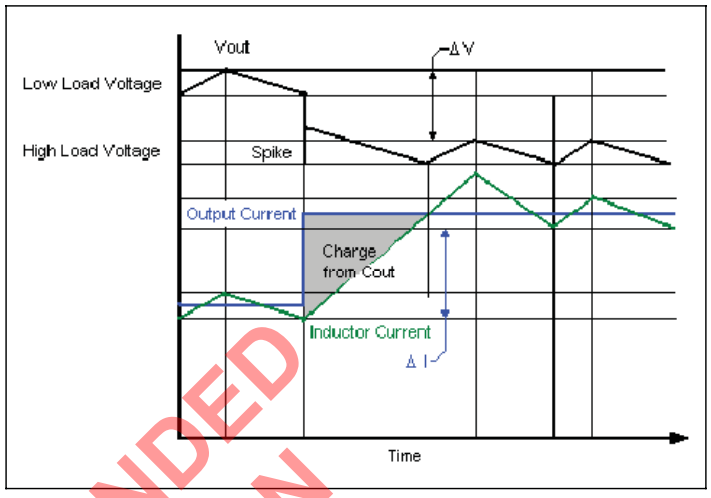


Figure 1 - Hysteretic Converter Response to a Positive Transient

The first condition is easy to see; if the ESR is too high, the transient response will fail.

In the second condition, because the hysteretic converter responds in < 100ns, the capacitor does not droop very far before the inductor current starts ramping up. (This is not true of control schemes where time constants in the error amplifier cause delays.) Once the inductor current starts to rise, the increasing DV of the capacitor is offset by reduced DV from the ESR, so DV is constant. If the DV due to the charge taken from the capacitor before the inductor current reaches the load current (see the shaded area above) is less than VIMVP, then the transient response will pass.

Since HFM (High Frequency Mode) has the most severe requirements, the other modes will be satisfied by a design optimized for HFM. The maximum ESR requirement to meet the transient requirement is:

C: $ESR_{MAX} := \left| R_{IMVP} \right|$

$ESR_{MAX} = 2.1000 \times 10^{-3}\ \Omega$

Applications Information (Cont.)

For the second condition, we need to know the inductor value, which is a function of the highest desired switching frequency. The maximum frequency occurs at the highest input voltage. As a reasonable compromise between efficiency and component size, a maximum switching frequency of 300kHz or less per phase is desired. Since we are analyzing the minimum inductance for one phase, the ripple voltage will actually be twice the amount of the specified output ripple, since the ripple voltage from each phase will tend to cancel. Please consult the data for your specific processor. *Note: The desired ripple amount comes from Intel's IMVP-6 Rev 0.5 specs.*

$$d_{MIN} := \frac{V_{HFM\_NL}}{V_{INMAX}}$$

$$F_S := 250kHz$$

$$V_{RIPPLE} := 10m\ V$$

The current share accuracy is achieved by Semtech's proprietary Combi-Sense technology and no longer a function of the current sense resistor values.

D. $$L_{MIN} := d_{MIN} \cdot \frac{(V_{INMAX} - V_{HFM\_NL}) \cdot (ESR_{MAX})}{F_S \cdot 2V_{RIPPLE}}$$

$$ESR_{MAX} = 2.1000 \times 10^{-3}\ \Omega$$

$$L_{MIN} = 361.3852 \times 10^{-9}\ H$$

Selected L = 470nH as the next closest value.

Load Step:

$$L_1 := 0.47 \cdot \mu H$$

$$L_2 := 0.47 \cdot \mu H$$

This value of inductance is required up to maximum load. Inductors with a "swinging choke" characteristic, where the zero current value of inductance is much less than the full load current inductance can be used, as long as the above restriction is met. Then, the worst-case (low input voltage) response time (the time for the current to reach the new transient value) is:

$$dT := \frac{L_1 \cdot (I_{HFM\_FL} - I_{LKGMAX}) \cdot \frac{1}{2}}{V_{INMIN} - V_{HFM\_NL}}$$

$$dT = 927.8623 \times 10^{-9}\ s$$

Add ~200ns for the propagation delay from a change at the output to the MOSFET switch turning on in reaction due to the minimum on time requirement of the IC. Since the shaded area is triangular, the total charge taken out of the capacitor = (dI / dt) / 2. Q = C / dV = (dI / dt) / 2, therefore;

F. $$C_{MINP} := \frac{(I_{HFM\_FL} - I_{LKGMAX}) \cdot (dT + 2 \cdot 10^{-7} \cdot sec)}{2 \cdot V_{DP}}$$

$$C_{MINP} = 256.6036 \times 10^{-6}\ F$$

Selected C_{OUT} = 330µF x 6 to meet transient requirements. This condition applies only to the positive transient.

Load Release:

The worst-case for the transient load release to happen is when one phase has just reached the maximum hysteresis, (i.e., it has just turned off the high-side switch). At this point, the second phase will be declining (approximately) through the nominal voltage, (i.e., its low-side switch will be on).

Applications Information (Cont.)

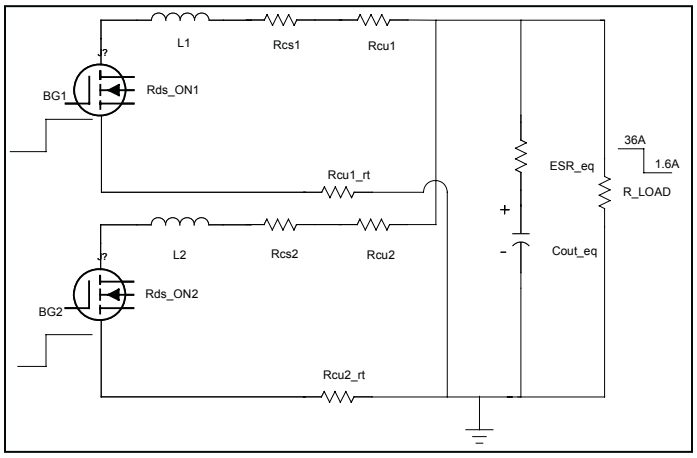


Figure 2 - Load Release Behavior of Dual Phase Buck Converter

Load is stepping from 36A to 1.6A:

$$V_{TRANS\_MIN} := -R_{IMVP} \cdot \left(I_{HFM\_FL} - I_{LKGMAX}\right) + 10 \cdot m \cdot V$$

$$V_{TRANS\_MIN} = 0.082\,V$$

The diagram below shows the response of the converter. The control circuit quickly turns off TG and turns on both bottom gates to discharge the inductors as quickly as possible. The stored energy, once losses in the ESR and FET RDS is subtracted, is transferred into the output capacitors.

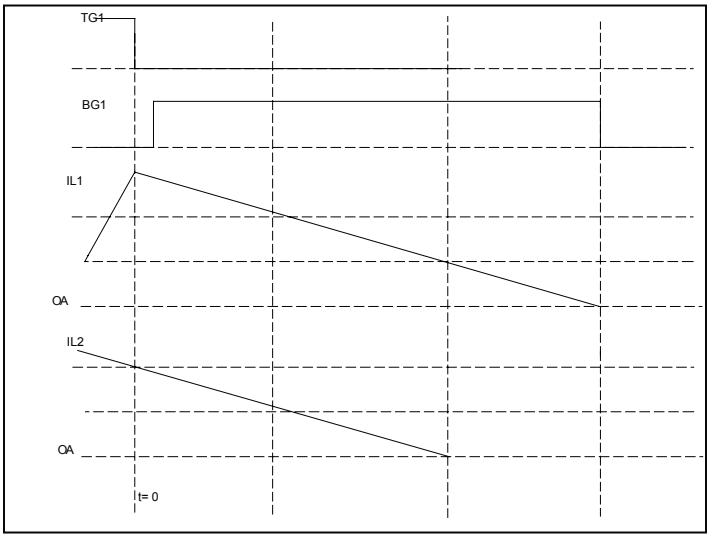


Figure 3 - Waveforms of Figure 2

$$I_{RIPPLE} := 13A$$

See STEP 6 for how to derive the ripple current.

$$I_{t0\_1} := \frac{I_{HFM\_FL}}{2} + \frac{I_{RIPPLE}}{2}$$

$$I_{t0\_2} := \frac{I_{HFM\_FL}}{2}$$

$$I_{t0\_1} = 24.5000 \times 10^{0}\,A$$

$$I_{t0\_2} = 18.0000 \times 10^{0}\,A$$

$$C_{OUT} := 330 \cdot 10^{-6}\,F$$

$$R_{ESR} := 6 \cdot m \cdot \Omega$$

We assume for the worst-case condition, at t = 0, one inductor is sitting at its maximum, while the other is sitting at its nominal. After t = 0, both inductors discharge at a rate equal to V_{FL} / L. (without the consideration of the secondary order effect, such as, Rds_on drop, current sense resistor and miscellaneous trace drop).

What happens in terms of energy: The energy released from both inductors during load step down will be dissipated through the following means:

$$I_{L1}(t) := \left(I_{t0\_1} - \frac{V_{HFM\_FL} \cdot t}{L_1}\right)$$

$$I_{L2}(t) := \left(I_{t0\_2} - \frac{V_{HFM\_FL} \cdot t}{L_2}\right)$$

$$t := 0, 50n \cdot s \,..\, 10\mu \cdot s$$

$$I_{CAP}(t) := I_{L1}(t) + I_{L2}(t) - I_{LKGMAX}$$

Applications Information (Cont.)

Since both inductors are discharging at the same time and the same rate, there are two terms contributing to the increase of the voltage on the output capacitors. First is due to the ESR of the output capacitor. Second is due to the added charge contributed by the inductor currents.

G: $$V_{ESR}(t,N) := I_{CAP}(t)\cdot\frac{R_{ESR}}{N} \quad --(1)$$

H: $$dV_{CAP}(t,N) := \frac{I_{CAP}(t)\cdot t}{C_{OUT}\cdot N} \quad --(2)$$

I: $$V_{TOTAL}(t,N) := V_{ESR}(t,N) + dV_{CAP}(t,N)$$

The goal here is to use minimum amount of N x C_{OUT} to meet the transient requirement, with some headroom to allow for component tolerance.

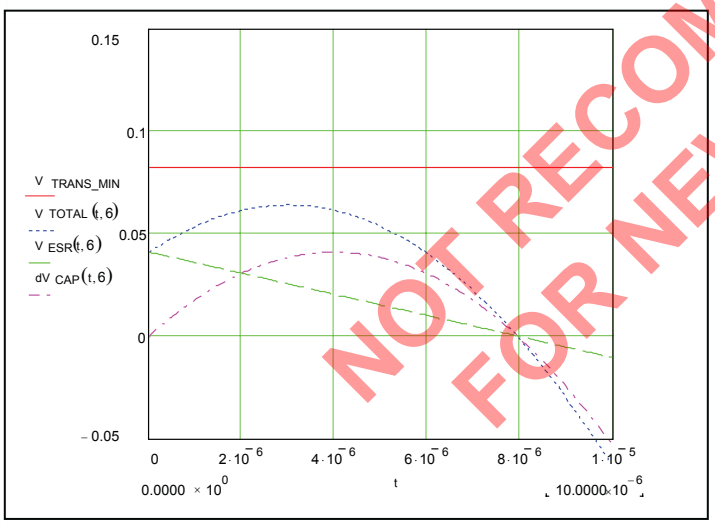


Figure 4 - Simulated (Load Release) Transient Response

Using Panasonic SPCAP, specified as 330µF at 2.0V with 6mΩ ESR, we see that 6 caps are sufficient for the ESR requirements, and also meet the capacitance requirement.

STEP 2: Droop Calculation

SC452 offers 2 droop methods: Method I — Current Sense Resistor Droop, Method II — DCR Resistive Droop.

Method I: Current Sense Resistor Droop

In an SC452 design, setting the IMVP gain is through the use of the droop amplifier. This IMVP gain is used to meet the IMVP load line specification.

The IMVP load line is defined as the High Frequency Mode at no-load voltage, minus the High Frequency Mode at full-load voltage, divided by the maximum (High Frequency Mode) load current. Since SC452 provides remote sensing for the core voltage, we no longer need to adjust for the trace loss at full load (such adjustment was needed for IMVP4 and 4+ core controllers, such as SC450 and SC451).

$$V_{HFM\_FL} = 1.195V$$

$$R_{CS1} := 0.5m\cdot\Omega$$

$$R_{CS2} := 0.5m\cdot\Omega$$

In order to provide the droop required by IMVP VI application, we will use the Block Diagram on Page 11 to determine the component values. The reference designators that are used in this worksheet are from the SC452 evaluation board schematic.

Applications Information (Cont.)

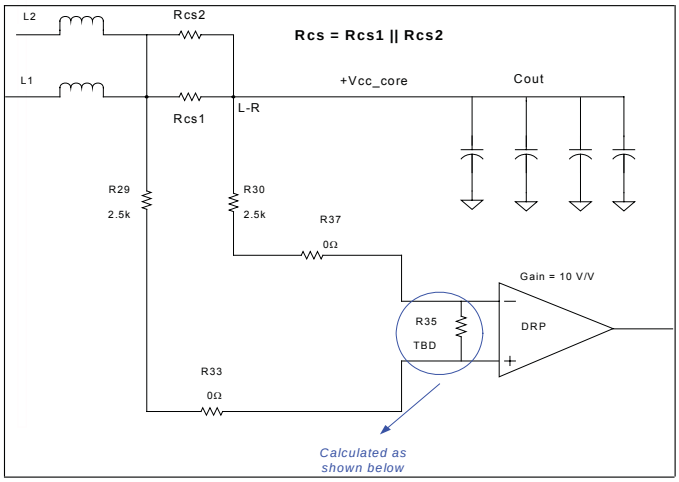


Figure 5 - Current Sense Resistive Droop Method

Since Rsense, R29, R30, R37 and R33 are pre-determined to the values shown on the above diagram, we will need to calculate the value of R35 to give us the correct droop.

According to the IMVP-VI droop requirement:

$$R_{IMVP} := -2.1 \cdot \frac{m \cdot V}{A}$$

the required droop at full load is therefore,

$$V_{DP} = 92.4000 \times 10^{-3}\ V$$

Since the droop amplifier has a gain of 10V/V, the actual voltage appears across R35 is only VDP_R35:

$$G_{DP\_AMP} := 10\frac{V}{V}$$

$$V_{DP\_R35} := \frac{V_{DP}}{G_{DP\_AMP}}$$

Since at full load, the voltage drop across the current sense resistor is VDP_CS.

$$R_{CS} := \frac{R_{CS1} \cdot R_{CS2}}{R_{CS1} + R_{CS2}}$$

$$V_{DP\_CS} := R_{CS} \cdot I_{HFM\_FL}$$

$$R_{29} := 2.5 \cdot k \cdot \Omega \qquad R_{30} := 2.5 \cdot k \cdot \Omega$$

We can calculate the value of R35 by using the equation as follows:

$$R_{35} := (R_{29} + R_{30}) \frac{V_{DP\_R35}}{V_{DP\_CS} - V_{DP\_R35}}$$

$$R_{35} = 26.2500 \times 10^{3}\ \Omega$$

Selected R35 = 26.5kΩ as the next closest value.

METHOD II: DCR Droop Method

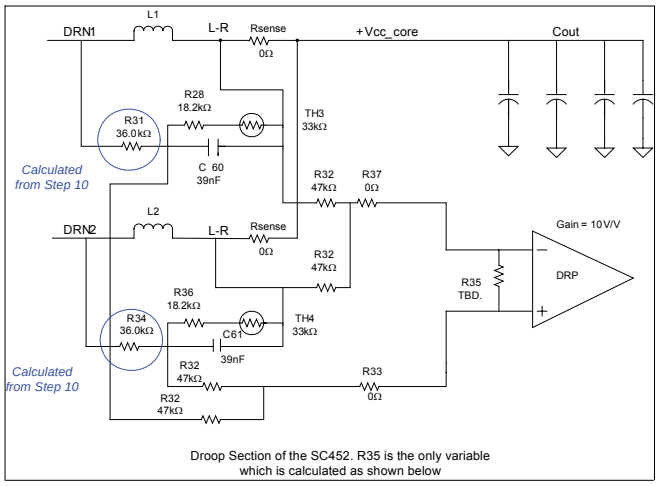


Figure 6 - Inductive DCR Droop Method

Applications Information (Cont.)

Using Inductive DCR droop method will also require the external compensation for the temperature coefficient of the DCR resistance. We will cover the entire thermal design in STEP 10. Here we are only interested in deriving the correct value of the droop resistor R35.

To simplify the design process, here we will use the nominal DCR resistance value published in the inductor vendor's datasheet.

As shown in Figure 6 (Page 23), by moving the regulation point before the output inductor (at the DRN1 and DRN2 node), droop becomes equal to the average voltage drop across the output inductor's DCR as well as any distributed resistance. The DCR droop is simply a RC low-pass filter placed across the output inductor. This filter must have the same time constant that the output inductor and its DCR have. If the DCR value of the inductor is very low, then care must be given to include any distributed/parasitic impedances on the board.

In the SC452 evaluation design, this low pass filter is represented by combination of R31, R28, TH3, C60, R32 and R35 (for phase 1) and R34, R36, TH4, C61, R32 and R35 (for phase 2). For phase 1, resistor combination R28, TH3 and R32, R35 are used to scale the magnitude of the droop. The output of this low pass filter is summed together with that of the phase 2 and then fed directly into the droop amplifier. The effects of this filter on the frequency response is minimal and can be ignored.

From Step 1 we have the inductor and DCR value as:

$$L_1 = 470.0000 \times 10^{-9}\ \text{H}$$

$$L_2 = 470.0000 \times 10^{-9}\ \text{H}$$

DCR: = 1.2 • m • Ω

The time constant of the output inductor is given by,

$$\tau := \frac{L_1}{DCR}$$

$$\tau = 391.6667 \times 10^{-6}\ \text{s}$$

The RC filter time constant is set by C60 and parallel combination of R31 and R28, TH3, R32 and R35.

In order to calculate R35 and C60, use the following simplified diagram for Phase 1,

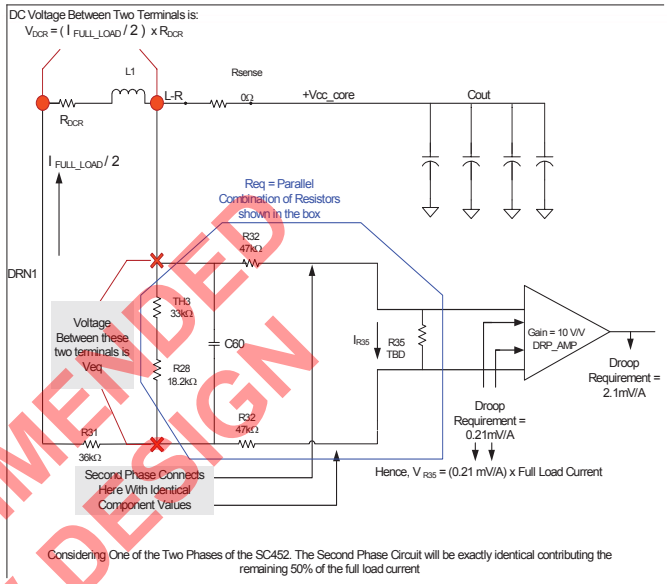


Figure 7 - Inductive DCR Droop Method (Simplifed Diagram)

According to the IMVP VI droop requirement,:

$$R_{IMVP} := -2.1 \cdot \frac{m \cdot V}{A}$$

$$V_{DP} = 92.4000 \times 10^{-3}\ \text{V}$$

Since the droop amplifier has a gain of 10V/V, the actual voltage appears across R35 is only VR35

$$V_{R35} := \frac{V_{DP}}{G_{DP\_AMP}}$$

$$G_{DP\_AMP} = 10.0000 \times 10^{0}$$

Applications Information (Cont.)

Consider Phase 1

Since at full load, the voltage drop across the DCR is VDCR,

$$V_{DCR} := DCR \cdot \frac{I_{HFM\_FL}}{2}$$

We can calculate the value of R35 as follows:

R_{31}: 16 • k • Ω

$R_{28} := 18.2 \cdot k \cdot \Omega$

$TH3 := 33 \cdot k \cdot \Omega$

$R_{32} := 47 \cdot k \cdot \Omega$

$$R_{eq} := \frac{(TH3 + R_{28})(R_{35} + 2R_{32})}{(TH3 + R_{28} + R_{35} + 2R_{32})}$$

So,

$$V_{eq} := V_{DCR} \cdot \frac{R_{eq}}{R_{eq} + R_{31}}$$

Now,

$$I_{R35} := \frac{V_{eq}}{2 \cdot R_{32} + R_{35}}$$

$$V_{R35\_1} := I_{R35\_1} \cdot R_{35}$$

Consider Phase 2

Since the components and current are identical for phase 2 we get the same expression for voltage across R35,

$$V_{R35\_2} := I_{R35\_2} \cdot R_{35}$$

$I_{R35\_1} := I_{R35\_2}$ equal to I_{R35}

Total voltage across R35 is given as:

$$V_{R35} := V_{R35\_1} + V_{R35\_2}$$

Substituting equations A,B,C, D, E, F, G into H and simplifying we get the following final expression for R35:

$$R_{35\_DCR} := \frac{(TH3 + R_{28}) \cdot 2R_{32} + (TH3 + R_{28}) \cdot R_{31} + 2 \cdot R_{32} \cdot R_{31}}{\frac{2 \cdot V_{DCR} \cdot (TH3 + R_{28})}{V_{R35}} - (TH3 + R_{28} + R_{31})}$$

$$R_{35\_DCR} = 31.6633 \times 10^{3}\ \Omega$$

$$R_{combination} := \left(\frac{1}{R_{32} + R_{32} + R_{35\_DCR}} + \frac{1}{R_{31}} + \frac{1}{R_{28} + TH3} \right)^{-1}$$

$$R_{combination} = 11.1125 \times 10^{3}\ \Omega$$

$$C_{60} := \frac{\tau}{R_{combination}}$$

$$C_{60} = 35.2457 \times 10^{-9}\ F$$

Applications Information (Cont.)

We use the standard resistor value of 32K for R35 in the case of DCR droop method. For C60 and C61, we use standard capacitor value of 7nF.

STEP 3: Calculate Input RMS Current (for input capacitor selection)

In order to calculate the worst case input RMS current, the layout is important. If the input capacitors for both phases are very close together, the following formula is accurate and provides the lowest input capacitance.

$n := 2$

$$D := \frac{V_{HFM\_FL}}{V_{INMIN}}$$

$$P_{OUT} := I_{HFM\_FL} \cdot V_{HFM\_FL}$$

$$P_{OUT} = 43.6284 \times 10^{0}\ W$$

The simplified expression is given as:

$$I_{RMS1} := \sqrt{(D)\cdot\left(\frac{1}{n} - D\right)\cdot I_{HFM\_FL}^{2} + \frac{n^{2}}{12\cdot n\cdot D^{2}}\cdot I_{RIPPLE}^{2}\cdot (D)^{3}}$$

$$I_{RMS1} = 7.93\,A$$

In this case, 6 x 22µF/25V POSCaps (1.5A ripple current rating) are marginal. A seventh POScap is required if full load must be sustained indefinitely at V_{INMIN}. Five 10µF/25V/1210 (2A ripple current rating) ceramic capacitors will work down to V_{INMIN}.

If the input capacitors and high side FETs are separated by a very short distance, the input capacitors and the board inductance will form an LC filter. Surprisingly, little inductance is required for the pole to be lower than the switching frequency. In the case of using 6 x 22µF POSCaps, three near each phase:

$C_{input} := 66\cdot\mu F$

$$L_{in} := \frac{1}{(2\cdot\Pi\cdot F_S)^{2}\cdot C_{input}}$$

$$L_{in} = 6.14\times 10^{-9}\ H$$

So effective is this that it takes less than 7nH to separate the phases from each other. This is about 1.5/inch of 250 mil wide trace. If the phases are separated, the following formula is more accurate:

$$P_{IN} := \frac{P_{OUT}}{85\%} \qquad I_{IN\_DC} := \frac{P_{IN}}{V_{INMIN}}$$

$$I_{IN\_DC} = 5.1328 \times 10^{0}\ A$$

$$I_{RMS2} := \sqrt{n\cdot\left[\left(\frac{I_{HFM\_FL}}{n}\right) - I_{IN\_DC}\right]^{2}\cdot D + \left[n\cdot I_{IN\_DC}^{2}\cdot(1-D)\right]}$$

$$I_{RMS2} = 9.2970\times 10^{0}\ A$$

Selection:

$C_{I\_RMS\_POSCAP} := 1.5A$ --> 8 X 22µF/25V POSCaps (1.5A ripple current rating) (4 per phase).

$C_{I\_RMS\_MLCC} := 2A$ --> 6 X 10µF/25V MLCC (2A ripple current rating) (3 per phase).

Applications Information (Cont.)

STEP 4: Combi-Sense Component Values Calculation

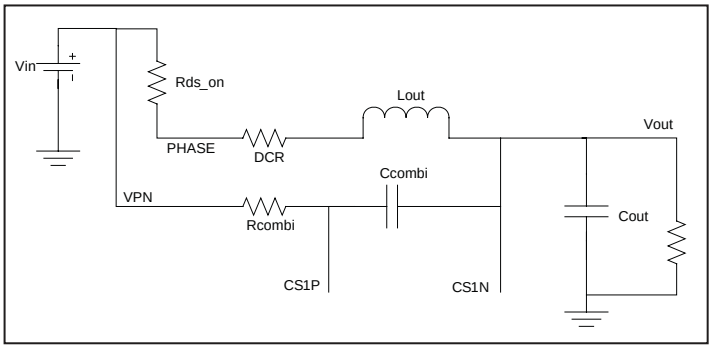


Figure 8 - The Equivalent Circuit of Combi-Sense During On-Time

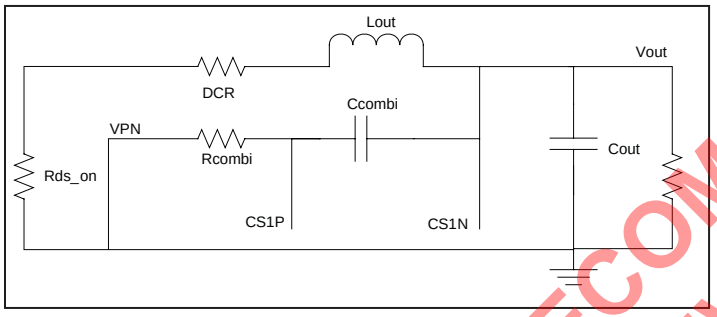


Figure 9 - The Equivalent Circuit of Combi-Sense During Off-Time

The equivalent Comb-Sense resistance is then given by the following equations:

$R_{HS\_FET} := \frac{0.008}{2} \cdot 1.25\Omega$ ---> 2 X IRF7821 per phase @ 75°C, per datasheet effective Rds-on at 75°C is 1.25 x 8mΩ.

$R_{LS\_FET} := \frac{0.004}{2} 1.2\cdot\Omega$ --->2 X IRF7832 per phase @ 75°C, per datasheet effective Rds-on at 75°C is 1.2 x 4mΩ.

$R_{IND} := 0.0012\Omega$

$d_{NOM} := \frac{V_{HFM\_NL} - \left|R_{IMVP}\right| \cdot I_{HFM\_FL}}{V_{INNOM}}$

$R_{SENSE} := d_{NOM} \cdot R_{HS\_FET} + \left(1 - d_{NOM}\right) R_{LS\_FET} + R_{IND}$

$R_{SENSE} = 3.7658 \times 10^{-3}\,\Omega$

$\frac{L_1}{R_{SENSE}} = 1.2481 \times 10^{-4}\,s$

In Figures 8 and 9 R_{COMBI} is the parallel combination of R4 and R7. R4 is the gain setting resistor and R7 with R4 sets R_{COMBI}.

$R_7 := 7.5 \times 10^3 \cdot \Omega$

$R_4 := 100 \cdot 10^3 \cdot \Omega$

Note: We assume R7 and R4 to be 7.5k and 100k respectively. One can vary R4 to have desired gain and the signal for combi-sense. If thermal compensation is required please refer Step 10.

$R_{COMBI} := \frac{1}{\frac{1}{R_7} + \frac{1}{R_4}}$

$R_{COMBI} = 6.9767 \times 10^3\,\Omega$

$C_{COMBI} := \frac{L_1}{R_{SENSE} \cdot R_7}$

$C_{COMBI} = 16.6408 \times 10^{-9}\,F$

From the above calculation, we determined the values for the Combi-Sense components: R7, R4, R23, R20, C8 and C17 ----> where R7 = R23 = 7.5kΩ, 11.5KΩ, R4 = R20 = 100KΩ, C8 = C17 = 12nF.

Applications Information (Cont.)

STEP 5: Hysteresis (Frequency) Setting

The next step is to calculate the desired hysteresis voltage level for a fixed switching frequency. Since SC452 is a hysteretic converter with the benefits of Combi-Sense technology, the ripple for the hysteretic switching control is provided by the Combi-Sense current feedback.

The ripple inputs are fed to a summer via a multiplexer which is synchronized to the active phase with the select ouput. The hysteresis signal is added at the summer. The hystersisis voltage is set directly by the resistor divider from the 2V REF output.

From the circuit in Figure 8 on Page 27, we can write the following equation for Combi-Sense operation during on time (high side MOSFETs are on),

$$Vin - Vout := Vcombi(t) + Rcombi \cdot Ccombi \cdot \frac{dVcombi(t)}{dt}$$

We can simplify the above equation as follows:

$$\int \frac{1}{Rcombi \cdot Ccombi} dt = \int \frac{1}{Vin - Vout - Vcombi(t(t))} dVcombi$$

Since we are interested in the end point for this waveform we simplify the equation with $t = t_{ON}$.

Hence, the solution for the above equation is:

$$\frac{Ton}{Rcombi \cdot Ccombi} := -\ln[(Vin - Vout) - Vcombi(t)] + Vini$$

In the above equation Vini is the initial value of voltage across the capacitor. Let us assume it to be equal to Vhys_low voltage. This is a fair assumption because of the architecture of the hysteretic comparator. We can rewrite the above equation as follows:

$$\frac{Ton}{Rcombi \cdot Ccombi} := -\ln[(Vin - Vout) - Vcombi(t)] + Vhys\_low$$

Using the Taylor Series we can expand the right hand side.

If we consider only the first term of the Taylor series the equation is greatly simplified with about a 20% error in the final value. If first 3 terms are considered the equation will give virtually zero error,

$$\frac{Ton}{Rcombi \cdot Ccombi} := \frac{Vcombi(Ton)}{Vin - Vout} + Vhys\_low$$

$$Vcombi(Ton) := (Vin - Vout)\left(\frac{Ton}{Rcombi \cdot Ccombi} - Vhys\_low\right)$$

For more accuracy we have to consider more than the first term of the Taylor series for the hysteretic frequency prediction.

The Feedback

The feedback voltage essentially contains two components, the voltage across the output capacitor and the voltage across the ESR of the output capacitor,

$$Vfb(t) := \Delta i \cdot esr + \int \frac{1}{Cout} \cdot \Delta i \, dt$$

In the above equation, Δi is the output inductor current ripple defined by the equation below for on-time,

$$\Delta i(t) := \frac{Vin - Vout}{2Lout} \cdot t$$

Again we are interested in the end point where $t = t_{ON}$, so the above equation simplifies to,

$$Vfb(Ton) := \frac{Vin - Vout}{2 \cdot Lout}\left(Ton \cdot esr + \frac{1}{Cout} \cdot \frac{Ton^2}{2}\right)$$

The Droop

The droop circuit is the simple inductor sense feedback for the SC452 with a gain of 0.00021.

$$Vdrp(Ton) := \frac{Vin - Vout}{2 \cdot Lout} \cdot Ton \cdot 0.00021$$

Equations 1, 2 and 3 can be used to obtain the final expression for the on-time for SC452 architechture.

Final Expresssion

$$2 \cdot Vcombi(Ton) := (10 \cdot Vdrp(Ton) + Vfb(Ton))(-12)$$

Substituting 1, 2 and 3 in the above equation we get the following final result for t_{ON},

$$\frac{3}{Lout Cout} \cdot Ton^2 + Ton\left(\frac{2}{Rcombi Ccombi} + \frac{0.0252}{2 \cdot Lout} + \frac{6 \cdot esr}{Lout}\right)$$

$$+ 2 \cdot Vhys\_low := 0$$

Since the converter is operating in continuous conduction mode we can write the expression for Frequency in terms of t_{ON} only. Finding the expresssion for t_{OFF} is a similar procedure as we have for t_{ON} but for CCM mode we need not care.

Where,

$$Fs := \frac{D}{Ton}$$

$$D := \frac{Vout - Iout \cdot Rdrop}{Vin}$$

Example Showing Variation with V_{HYS_LOW} Voltage:

$$L_{OUT} := 0.47 \cdot \mu \cdot H$$

$$C_{OUT} = 330.0000 \times 10^{-6} F$$

$$\tau_{COMBI} := R_{COMBI} \cdot C_{COMBI}$$

$$\tau_{COMBI} = 116.0988 \times 10^{-6} s$$

$$R_{calc} := 0.0126\Omega + 6 \cdot ESR_{MAX}$$

R_{CALC} is a constant obtained from equation 4 above. It enables better presentation of the solution of equation 4 as follows:

$$Fs(V_{HYS\_LO}) := \frac{d_{NOM}}{Ton(V_{HYS\_LO})}$$

$$Ton(V_{HYS\_LO}) := \frac{\frac{-(2L_{OUT} + \tau_{COMBI} \cdot R_{calc})}{L_{OUT} \cdot \tau_{COMBI}} + \sqrt{\left(\frac{2L_{OUT} + \tau_{COMBI} \cdot R_{calc}}{L_{OUT} \cdot \tau_{COMBI}}\right)^2 - 4 \cdot \frac{3}{L_{OUT} \cdot C_{OUT} \cdot 6} \cdot 2V_{HYS\_LO}}}{2 \cdot \frac{3}{L_{OUT} \cdot C_{OUT} \cdot 6}}$$

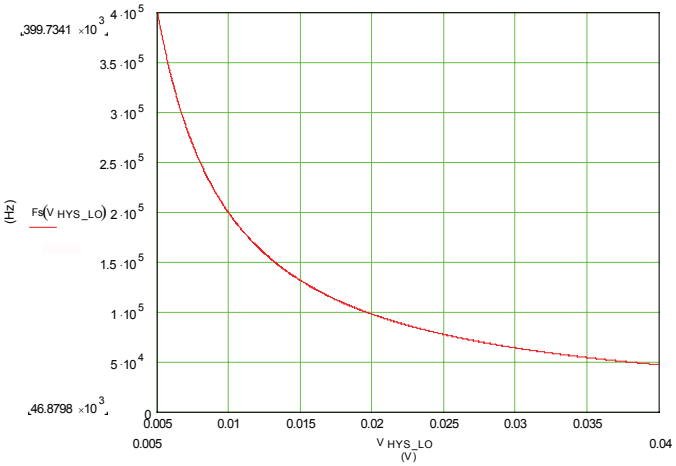


Figure 10 - Hysteresis Setting vs. Switching Frequency

Applications Information (Cont.)

STEP 6: Current Limit Calculation

Setting the threshold for current limit is a relatively straightforward process. To do this we must calculate the peak current based on the maximum DC value plus the worst-case ripple current. Because the SC452 has a current-limit comparator for each phase, the following calculations apply for a single phase.

Worst-case ripple occurs at the highest input voltage. Since ripple is also inversely proportional to inductance, it is recommended that the minimum inductance value be used based on the manufacturer's specified tolerance:

$d_{MIN} = 64.3750 \times 10^{-3}$ $L_{TOL} := 20\%$

$$I_{RIPPLE\_MAX} := \frac{(V_{INMAX} - V_{HFM\_NL}) \cdot d_{MIN}}{L_{MIN} \cdot F_S}$$

$L_{MIN} = 0.3760\,\mu H$

$I_{RIPPLE\_MAX} = 13.3333A$

To calculate the maximum DC value of current we must make an adjustment for the dynamic current-sharing tolerance. We then add the maximum DC current and the maximum ripple value to obtain peak current.

$I\_SHR_{TOL} := 5\%$ $I_{CC\_MAX} := I_{HFM\_FL}$

$$I_{PEAK} := \frac{1}{2} I_{CC\_MAX} \cdot (1 + I\_SHR_{TOL}) + \frac{I_{RIPPLE\_MAX}}{2}$$

$I_{PEAK} = 25.5667A$

It is recommended that the current limit be set at 110% of the peak value to allow for inductor current overshoot during load transients:

$I_{CLIM} := 1.10 \cdot I_{PEAK}$ $I_{CLIM} = 28.1233A$

In current limit, the voltage hysteretic converter is over-ridden by the current limit hysteretic comparator, and the TG pulse is terminated when the output of the current sense amplifier reaches the CL_hi threshold and BG terminated at the CL_lo threshold. These thresholds are set from the CLSET resistor divider:

$CL\_hi := 0.33 \cdot V(clset)$

$CL\_lo := 0.20 \cdot V(clset)$

Current limit pulses continue until 32 pulses after the voltage droops to the PWRGD low threshold; then the controller latches off.

$I_{CLIM} = 28.1233A$

$R_{SENSE} = 3.7658 \times 10^{-3}\,\Omega$

Per phase current limit is set by I_{CLIM}, Rsense (Combi-Sense), current sense amplifier gain in current limit mode and CLSET gain, therefore the dual phase current limit is set by the following equation:

$Ga_{CS\_CL} := 2 \cdot \frac{V}{V}$ $Ga_{CLSET} := \frac{1}{3} \cdot \frac{V}{V}$

$$V_{CLSET} := \frac{R_{SENSE} \cdot I_{CLIM} \cdot Ga_{CS\_CL}}{Ga_{CLSET}}$$

$V_{CLSET} = 635.4477 \times 10^{-3}\,V$

We calculate R14 and R13 based on the V_{CLSET} voltage,

$R_{14} := 100 \cdot 10^{3} \cdot \Omega$ $R_{13} := \frac{V_{CLSET} \cdot R_{14}}{2 \cdot V - V_{CLSET}}$

$R_{13} = 46568.2149\Omega$

We use 46.5K for R13 and 100K for R14.

Applications Information (Cont.)

STEP 7: OVP

No calculations are necessary for Over Voltage Protection. The OVP circuit of SC452 monitors the processor core Vcc_core voltage for an over-voltage condition. If the FB voltage is 200mV greater than the DAC_Droop (i.e., out of the powergood window), the SC452 will latch off and hold the low-side driver on permanently. Either the Power or EN must be recycled to clear the latch. The latch is disabled during soft-start and VID/DeeperSleep transitions. For safety, the latch is enabled if the FB voltage exceeds 1.8V even during VID/DeeperSleep transition.

STEP 8: Thermal Protection

SC452 will be disabled and latched off when the internal junction temperature reaches approximately 160°C. Either the Power or EN must be recycled to clear this fault.

STEP 9: Soft-Start/DAC Slew Control

The soft-start cap C12 in the SC452 eval board design serves two purposes: 1) define the soft-start ramp 2) define the DAC slew rate during DeeperSleep and VID transition. During VID/DeeperSleep transitions, the SS current is normally 120µA. During start-up, the SS current is normally 12µA.

Resistance of the node is set to provide a fixed gain of 10; as a result, only 0.21mW of resistance is required to produce the Intel-defined load line of 2.1mV/A.

According to Intel's IMVP-VI Timing Requirements, the maximum $t\_SFT\_START\_CC$ is specified at 3ms(max). And the slew rate for CPU_UP due to,

1) GV-III VID change is 3.2mV/µsec
2) Deeper Sleep exit is specified at 10mV/µsec

We will be doing three soft-start exercises based on the above three conditions:

1. Start-Up:

$$i_{SS\_STARTUP} := 12\cdot\mu\cdot A \qquad i_{SS\_STARTUP} := C_{SS}\cdot\frac{dV}{dt}$$

$$dV := V_{HFM\_NL} \qquad dt := 3m\cdot s$$

$$C_{SS} := \frac{i_{SS\_STARTUP}\cdot dt}{dV} \qquad C_{SS} = 27.9612\times 10^{-9}\,F$$

$$i_{SS\_GVIII} := 120\cdot\mu\cdot A$$

2. During GV-III Transition:

$$i_{SS\_GVIII} := C_{SS}\cdot\frac{dV}{dt}$$

$$Slew\_Rate_{GVIII} := 3.2\cdot\frac{mV}{\mu\cdot s}$$

$$\frac{dV}{dt} := Slew\_Rate_{GVIII}$$

3. During fast C4 exit:

$$C_{SS\_GVIII} := i_{SS\_GVIII}\cdot\frac{1}{Slew\_Rate_{GVIII}}$$

$$C_{SS\_GVIII} = 37.5000\times 10^{-9}\,F$$

$$i_{SS\_C4E} := 120\cdot\mu\cdot A \qquad i_{SS\_C4E} := C_{SS}\cdot\frac{dV}{dt}$$

$$\frac{dV}{dt} := Slew\_Rate_{C4E} \qquad Slew\_Rate_{C4E} := 10\cdot\frac{mV}{\mu\cdot s}$$

$$C_{SS\_C4} := i_{SS\_C4E}\cdot\frac{1}{Slew\_Rate_{C4E}}$$

$$C_{SS\_C4} = 12.0000\times 10^{-9}\,F$$

Taking into consideration of component tolerance, we use Css = 10nF to meet all three requirements.

STEP 10: DCR Droop Thermal Compensation

Note: (contact your local Semtech Representative for details)

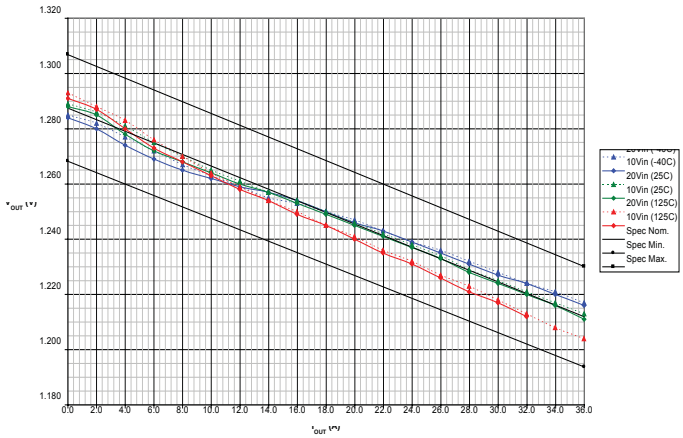
Applications Information (Cont.)

Component	Manufacturer	Series or Part Number
High Side MOSFET, HSFET	International Rectifier Fairchild Semiconductor Siliconix Infenion Technologies	IRF7821, IRF6602, SSC3002S, Si4860DY,Si4410BDY
Low Side MOSFET, LSFET	International Rectifier Fairchild Semiconductor Siliconix Infenion Technologies	Depends on Application
Boost Capacitor, Cbst	Various	X5R or better
Boost Diode, Dbst	Various	Schottky, 200mA or greater
Output Inductor, L	Panasonic / NEC TOKIN	0.5µH
Decoupling Capacitors	Various	X5R or better
Current Sense Resistor	IRC, Panasonic	ERJ-M1WTJ
Output Bulk Capacitors	Panasonic / NEC-TOKIN SPCAP	330µF, max ESR 6mΩ

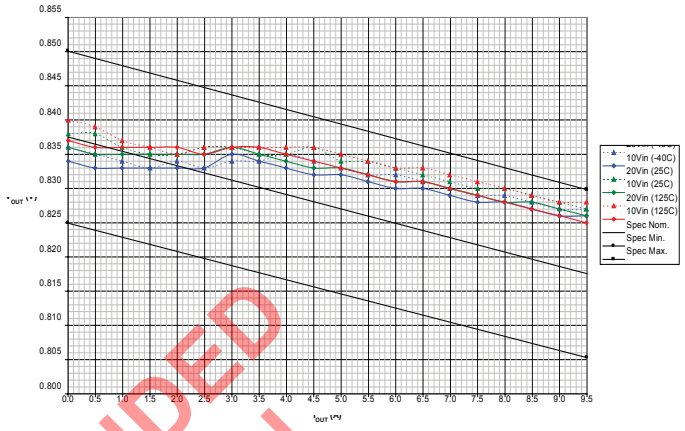
Company	Contact
International Rectifier	Web: http://www.irf.com/product-info/ Phone: (310) 726-8000
Panasonic	Web: http://www.panasonic.com/pic/ecg/ Phone: (201) 348-7522
IRC	Web: http://www.irctt.com Phone: (888) 472-4376
Kernet	Web: http://www.kernet.com/ Phone: (864) 963-6300
Sanyo	Web: http://www.sanyovideo.com/ Phone: (619) 661-6835
TDK	Web: http://www.component.tdk.com/components/components.html Phone: (847) 390-4373
Vishay/Dale	Web: http://www.vishay.com/brands/dale Phone: (402) 564-3131
Vishay/Siliconix	Web: http://www.vishay.com/brands/siliconix Phone: (800) 554-5565

Typical Characteristics

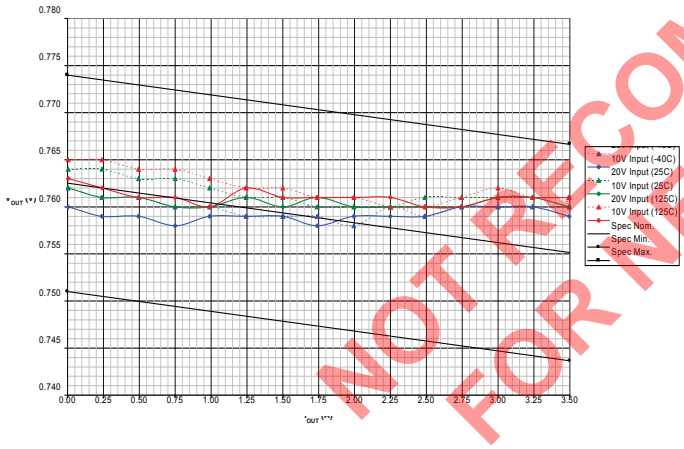
High Frequency Line and Load Regulation
V_{OUT} = 1.2875V, I_{OUT} = 0A to 36A (Spec bounds @ 25C)



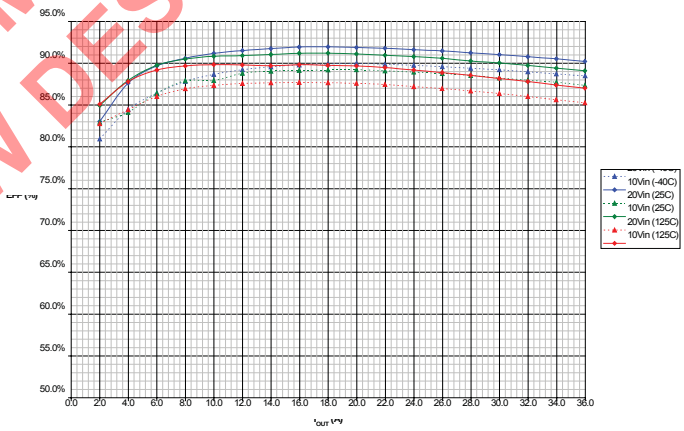
Low Frequency Line and Load Regulation
V_{OUT} = 0.8375V, I_{OUT} = 0A to 9.5A (Spec bounds @ 25C)



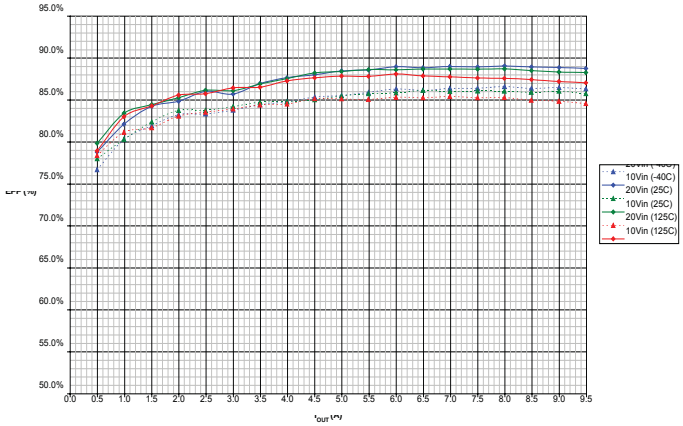
Deeper Sleep Line and Load Regulation
V_{OUT} = 0.7625V, I_{OUT} = 0A to 3.5A (Spec bounds @ 25C)



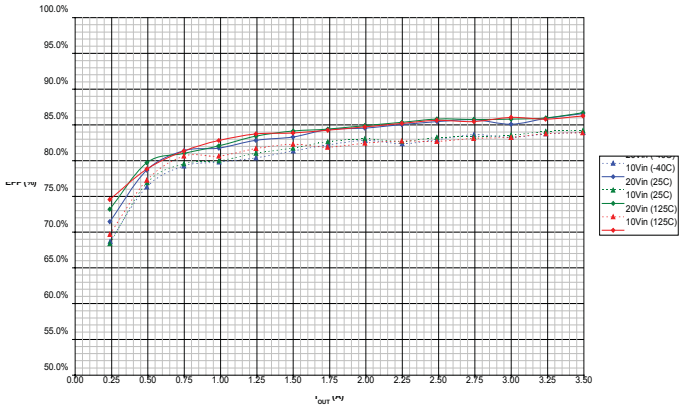
SC452 High Frequency Mode Output Power Efficiency
V_{OUT}=1.2875V, I_{OUT}=2A to 36A



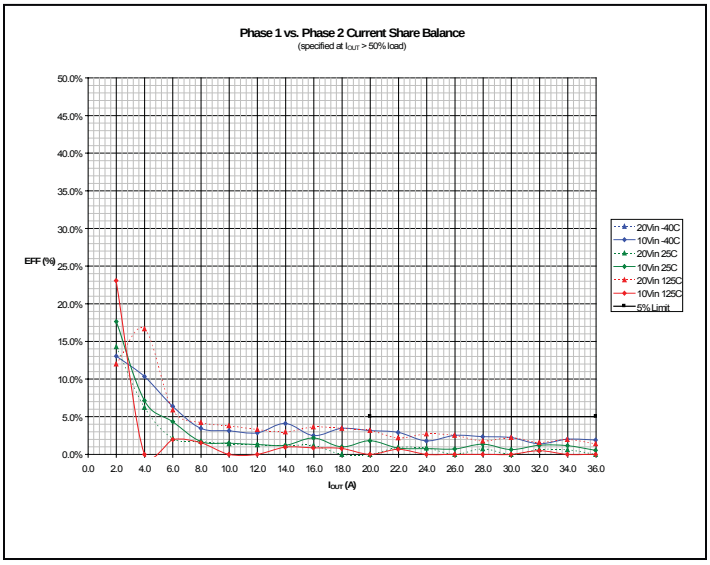
SC452 Low Frequency Mode Output Power Efficiency
V_{OUT}=0.8375V, I_{OUT}=1A to 9.5A

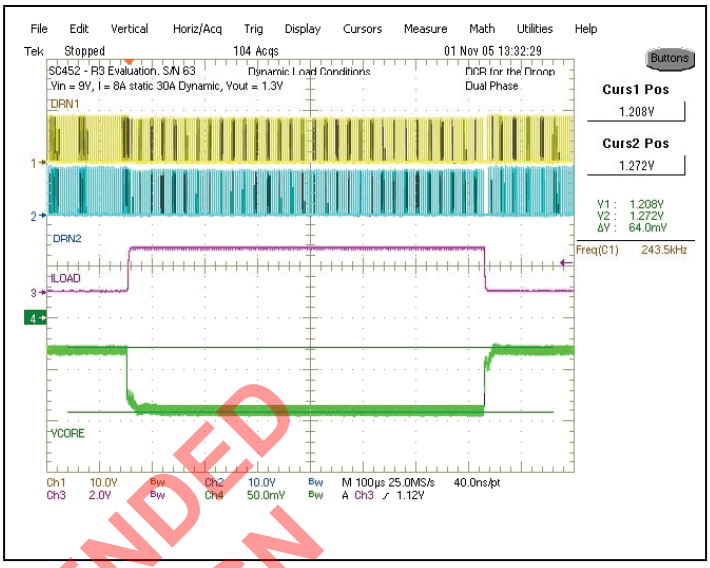


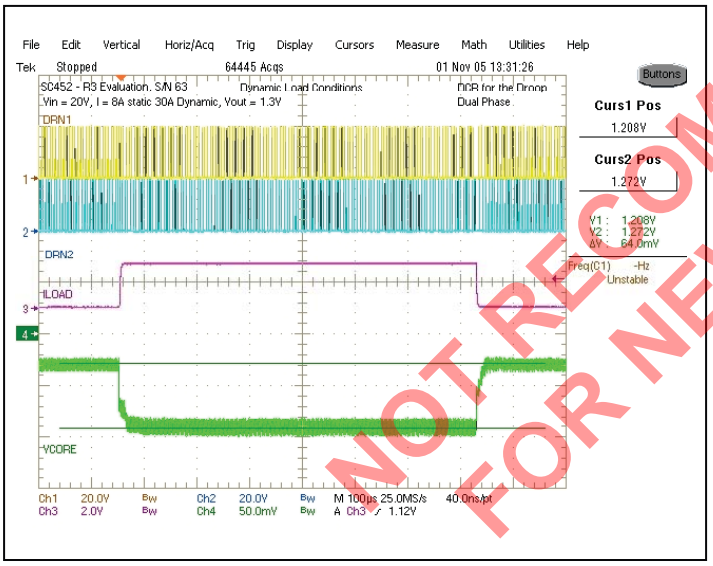
SC452 Deeper Sleep (C4) Mode Output Power Efficiency
V_{OUT}=0.7625V, I_{OUT}=0.25A to 3.5A

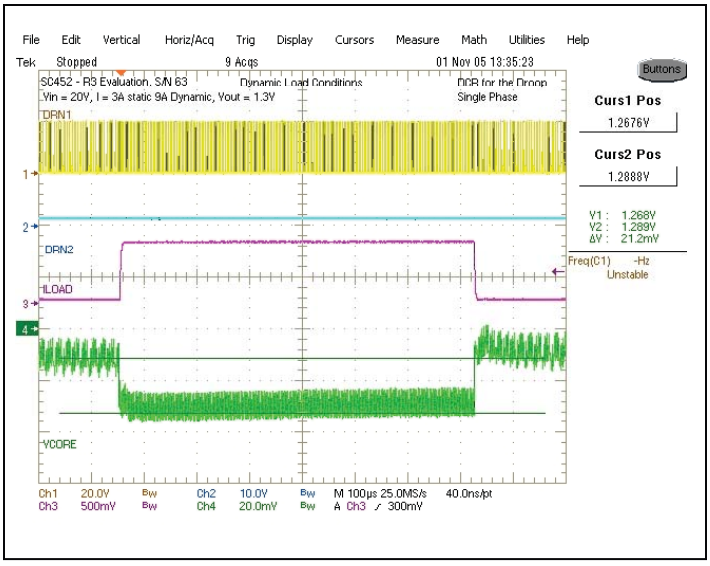


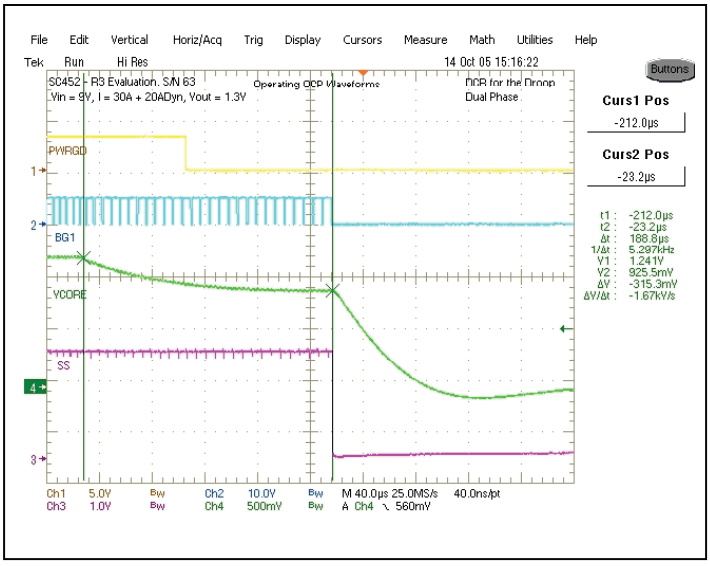
Typical Characteristics (Cont.)











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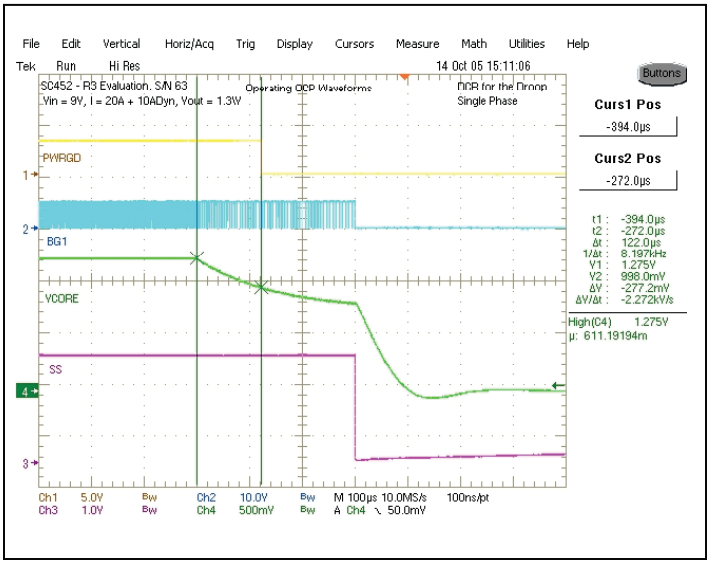
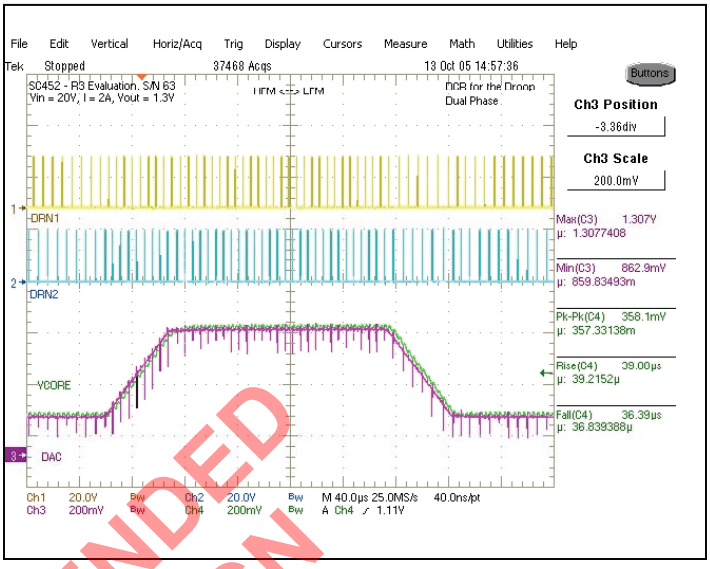
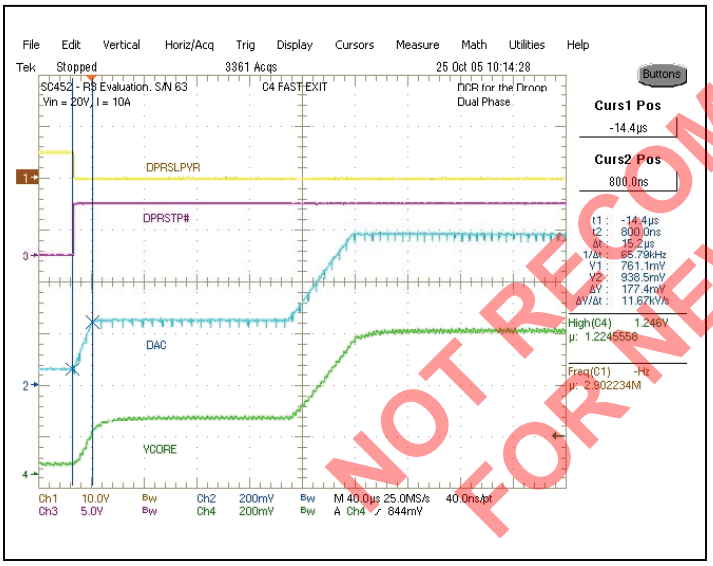
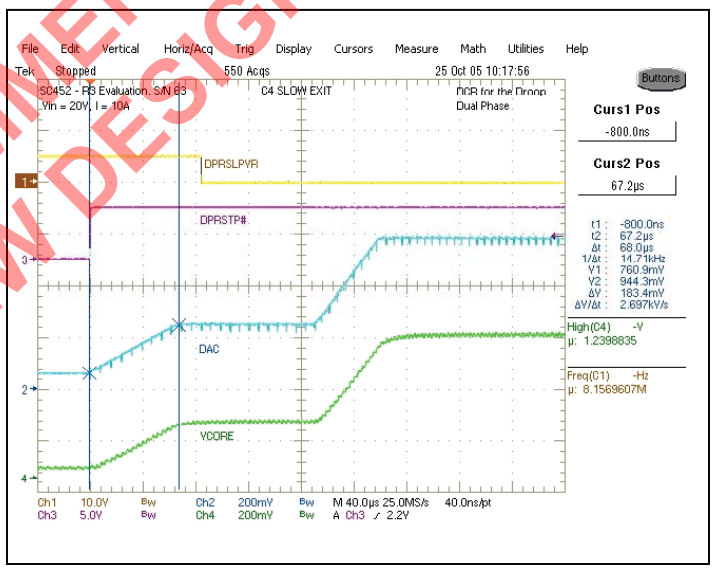
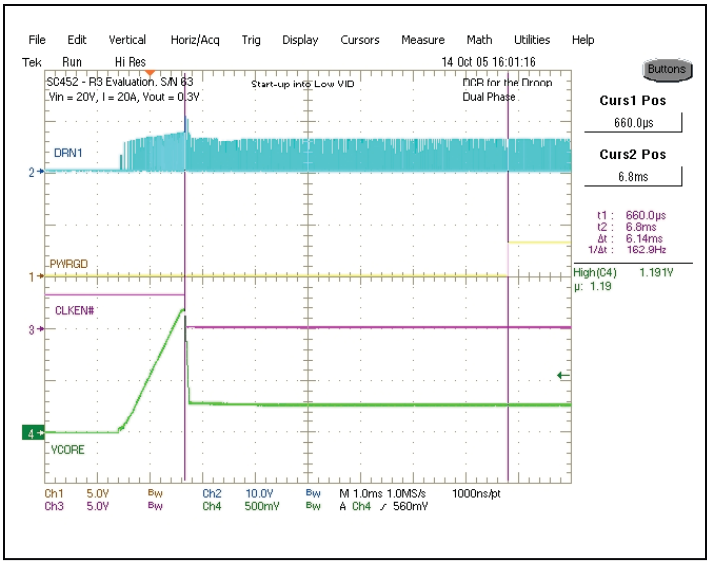
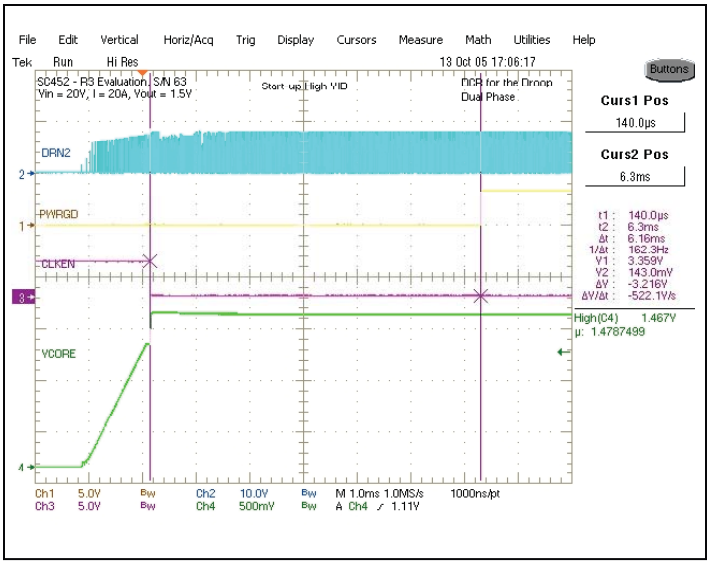




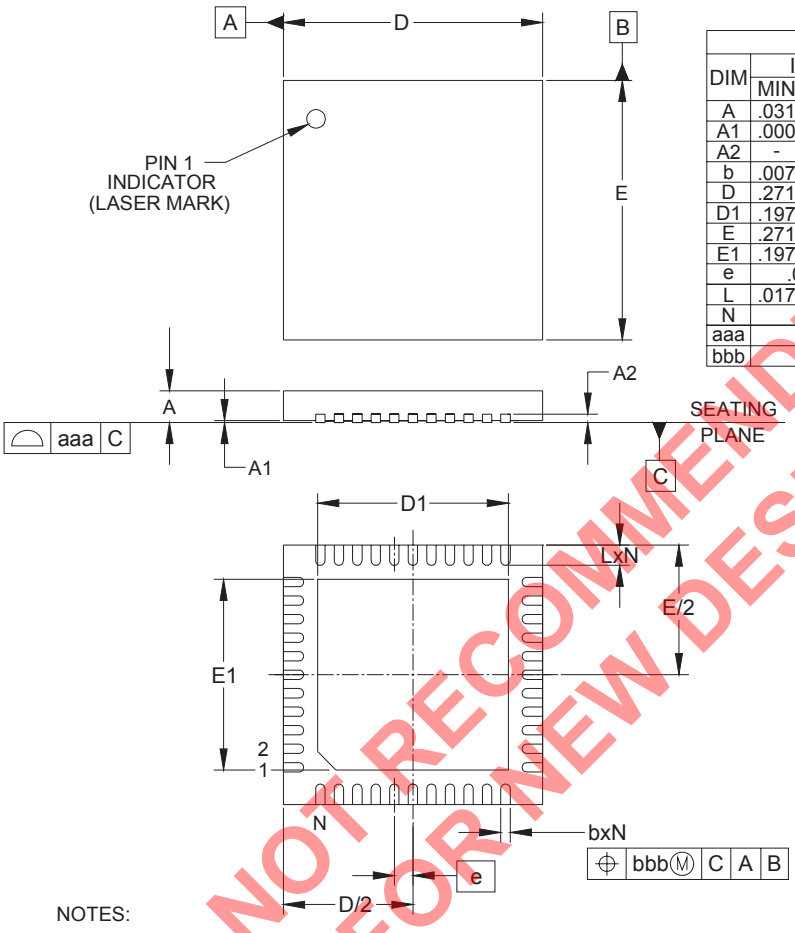








Outline Drawing - MLP-44

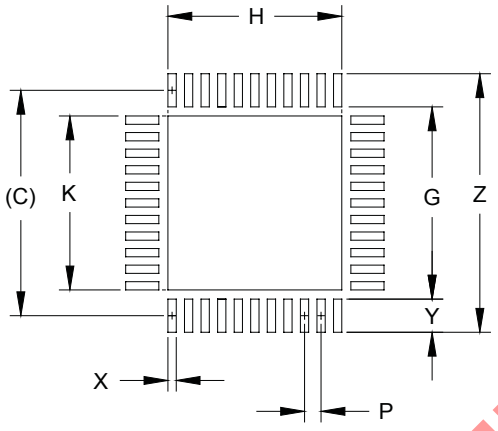


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.040	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.271	.275	.279	6.90	7.00	7.10
D1	.197	.203	.207	5.00	5.15	5.25
E	.271	.275	.279	6.90	7.00	7.10
E1	.197	.203	.207	5.00	5.15	5.25
e	.020 BSC			0.50 BSC		
L	.017	.021	.025	0.45	0.55	0.65
N	44			44		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLP-44



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.268)	(6.80)
G	.228	5.80
H	.207	5.25
K	.207	5.25
P	.021	0.50
X	.011	0.30
Y	.039	1.00
Z	.307	7.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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