

POWER MANAGEMENT

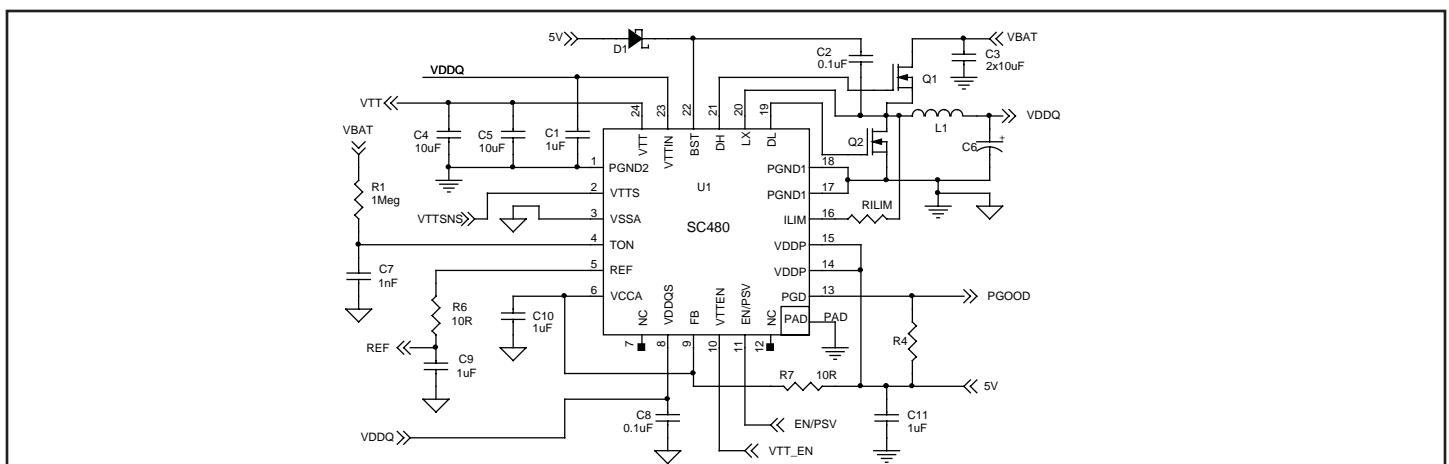
Description

The SC480 is a combination switching regulator and linear source/sink regulator intended for DDR1/2/3 memory systems. The purpose of the switching regulator is to generate the supply voltage, VDDQ, for the memory system. It is a pseudo-fixed frequency constant on-time controller designed for high efficiency, superior DC accuracy, and fast transient response. The purpose of the linear source/sink regulator is to generate the memory termination voltage, VTT, with the ability to source and sink a 3A peak current.

For the VDDQ regulator, the switching frequency is constant until a step in load or line voltage occurs at which time the pulse density, i.e., frequency, will increase or decrease to counter the transient change in output or input voltage. After the transient, the frequency will return to steady-state operation. At lighter loads, the selectable Power-Save Mode enables the PWM converter to reduce its switching frequency and improve efficiency. The integrated gate drivers feature adaptive shoot-through protection and soft-switching. Additional features include cycle-by-cycle current limiting, digital soft-start, over-voltage and under-voltage protection and a power good flag.

For the VTT regulator, the output voltage tracks REF, which is $\frac{1}{2}$ VDDQ to provide an accurate termination voltage. The VTT output is generated from a 1.2V to VDDQ input by a linear source/sink regulator which is designed for high DC accuracy, fast transient response, and low external component count. All three outputs (VDDQ, VTT and REF) are actively discharged when VDDQ is disabled, reducing external component count and cost. The SC480 is available in a 24-pin MLPQ (4x4 mm) package.

Typical Application Circuit



Features

- ◆ Constant On-Time Controller for Fast Dynamic Response on VDDQ
- ◆ DDR1/DDR2/DDR3 Compatible
- ◆ VDDQ = Fixed 1.8V or 2.5V, or Adjustable from 1.5V to 3.0V
- ◆ 1% Internal Reference (2% System Accuracy)
- ◆ Resistor Programmable On-Time for VDDQ
- ◆ VCCA/VDDP Range = 4.5V to 5.5V
- ◆ VIN Range = 2.5V to 25V
- ◆ VDDQ DC Current Sense Using Low-Side $R_{DS(ON)}$ Sensing or External R_{SENSE} in Series with Low-Side FET
- ◆ Cycle-by-Cycle Current Limit for VDDQ
- ◆ Digital Soft-Start for VDDQ
- ◆ Analog Soft-Start for VTT/REF
- ◆ Smart Over-Voltage VDDQ Protection Against Source-Current Loads
- ◆ Combined EN and PSAVE Pin for VDDQ
- ◆ Over-Voltage/Under-Voltage Fault Protection
- ◆ Power Good Output
- ◆ Separate VCCA and VDDP Supplies
- ◆ VTT/REF Range = 0.75V - 1.5V
- ◆ VTT Source/Sink 3A Peak
- ◆ Internal Resistor Divider for VTT/REF
- ◆ VTT is High Impedance in S3
- ◆ VDDQ, VTT, REF Are Actively Discharged in S4/S5
- ◆ 24 Lead MLPQ (4x4 mm) Lead-Free Package
- ◆ Fully WEEE and RoHS Compliant

Applications

- ◆ Notebook Computers
- ◆ CPU I/O Supplies
- ◆ Handheld Terminals and PDAs
- ◆ LCD Monitors
- ◆ Network Power Supplies

POWER MANAGEMENT
Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
TON to VSSA		-0.3 to +25.0	V
DH, BST to PGND1		-0.3 to +31.0	V
BST, DH to LX		-0.3 to +6.0	V
LX to PGND1		-2.0 to +25.0	V
DL, ILIM, VDDP to PGND1		-0.3 to +6.0	V
VDDP to DL		-0.3 to +6.0	V
VTTIN to PGND2; VTT to PGND2; VTTIN to VTT		-0.3 to +6.0	V
EN/PSV, FB, PGD, REF, VCCA, VDDQS, VTTEN, VTTS to VSSA		-0.3 to +6.0	V
VCCA to EN/PSV, FB, REF, VDDQS, VTT, VTTEN, VTTIN, VTTS		-0.3 to +6.0	V
PGND1 to PGND2; PGND1 to VSSA; PGND2 to VSSA		-0.3 to +0.3	V
Thermal Resistance Junction to Ambient ⁽¹⁾	θ_{JA}	29	°C/W
Operating Junction Temperature Range	T_J	-40 to +150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Peak IR Reflow Temperature, 10s - 40s	T_{PKG}	260	°C
ESD Protection Level ⁽²⁾	V_{ESD}	2	kV

Notes:

1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

TEST CONDITIONS: $V_{IN} = 15V$, $VCCA = VDDP = VTTEN = EN/PSV = 5V$, $VDDQ = VTTIN = 1.8V$, $R_{TON} = 1M\Omega$, $T_{AMB} = -40 TO +85C$.

Parameter	Conditions	25°C			-40°C to 85°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VCCA Operating Current	S0 State (VTT on); EN/PSV = VCCA; FB > Regulation Point, IVDDQ = 0A		1500			2500	μA
VCCA Operating Current	S3 State (VTT off); EN/PSV = VCCA; FB > Regulation Point, IVDDQ = 0A		800			1400	μA
VCCA Operating Voltage			5		4.5	5.5	V
VDDP Operating Current	FB > Regulation Point, IVDDQ = 0A		70			150	μA
TON Operating Current	$R_{TON} = 1M\Omega$		15				μA
VTTIN Operating Current	$IVTT = 0A$		1			5	μA
VCCA + VDDP + TON Shutdown Current	EN/PSV = VTTEN = 0V		5			11	μA
VTTIN Shutdown Current	EN/PSV = VTTEN = 0V		1				μA

POWER MANAGEMENT
Electrical Characteristics (Cont.)

 TEST CONDITIONS: $V_{IN} = 15V$, $V_{CCA} = V_{DDP} = V_{TTEN} = EN/PSV = 5V$, $V_{DDQ} = V_{TTIN} = 1.8V$, $R_{TON} = 1M\Omega$, $T_{AMB} = -40$ TO $+85C$.

Parameter	Conditions	25°C			-40°C to 85°C		Units
		Min	Typ	Max	Min	Max	
VDDQ Controller							
FB Error Comparator Threshold ⁽¹⁾	With Adjustable Resistor Divider		1.500		1.485	1.515	V
VDDQS Regulation Threshold	FB = AGND		2.5		2.475	2.525	V
	FB = VCCA		1.8		1.782	1.818	V
On-Time	$R_{TON} = 1M\Omega$, $V_{DDQ} = 1.8V$		460		368	552	ns
	$R_{TON} = 500k\Omega$, $V_{DDQ} = 1.8V$		265		212	318	
Minimum Off-Time			425			550	ns
VDDQS Input Resistance	FB < 0.3V		80				k Ω
	FB > 0.3V		91				k Ω
VDDQS Shutdown Discharge Resistance	EN/PSV = GND		16				Ω
FB Leakage Current					-1.0	1.0	μA
VDDQ Smart Psave Threshold			8				%
VTT Controller							
REF Source Current					10		mA
REF Sink Resistance			50				k Ω
REF Output Accuracy	$I_{REF} = 0$ to 10mA		900		882	918	mV
Shutdown Discharge Resistance (EN/PSV = GND)	VTT		0.25				Ω
	REF		8				Ω
VTT Output Accuracy (with respect to REF)	$-2A < I_{VTT} < 2A^{(9)}$		0		-40	+40	mV
VTTS Leakage Current					-1.0	1.0	μA
Current Sensing							
ILIM Current	DL High		10		9	11	μA
Current Comparator Offset	PGND1 - ILIM				-10	10	mV
Zero-Crossing Threshold	PGND1 - LX, EN/PSV = 5V		5				mV
VDDQ Fault Protection							
Current Limit (Positive) ⁽²⁾	PGND1 - LX, RLIM = 5k Ω		50		35	65	mV
	PGND1 - LX, RLIM = 10k Ω		100		80	120	
	PGND1 - LX, RLIM = 20k Ω		200		170	230	
Current Limit (Negative)	PGND1 - LX		-125		-160	-90	mV
Output Under-Voltage Fault	With Respect to FB Regulation Point		-30		-35	-25	%

POWER MANAGEMENT
Electrical Characteristics (Cont.)

 TEST CONDITIONS: $V_{IN} = 15V$, $V_{CCA} = V_{DDP} = V_{TTEN} = EN/PSV = 5V$, $V_{DDQ} = V_{TTIN} = 1.8V$, $R_{TON} = 1M\Omega$, $T_{AMB} = -40$ TO $+85C$.

Parameter	Conditions	25°C			-40°C to 85°C		Units
		Min	Typ	Max	Min	Max	
Under-Voltage Fault Delay	FB Forced Below UV V_{TH}		8				clks ⁽³⁾
Under-Voltage Blank Time	From EN High		440				clks ⁽³⁾
Output Over-Voltage Fault	With Respect to FB Regulation Point		+16		+12	+20	%
Over-Voltage Fault Delay	FB Above Over-Voltage Threshold		5				μs
PGD Low Output Voltage	Sink 1mA					0.1	V
PGD Leakage Current	FB in Regulation, PGD = 5V					1	μA
PGD UV Threshold	With Respect to FB Regulation Point		-10		-12	-8	%
PGD Fault Delay	FB Forced Outside PGD Window		5				μs
VCCA Under-Voltage (UVLO)	Falling Edge (Hysteresis 100 mV)		4		3.70	4.35	V
VTT Fault Protection							
UV Lower Threshold	VTT w/rt REF		-12		-16	-8	%
OV Upper Threshold	VTT w/rt REF		+12		+8	+16	%
Fault Shutdown Delay	VTT Outside OV/UV Window		50				μs
Thermal Shutdown ⁽⁴⁾⁽⁵⁾			160		150	170	°C
Inputs/Outputs							
Logic Input Low Voltage	EN/PSV Low/Low (Disabled)					1.2	V
	VTTEN Low (VTT Disabled)					0.6	
Logic Input High Voltage	EN/PSV Low/High (Enabled, Psave Disabled)				1.2	2.4	V
	VTTEN High (VTT Enabled)				2.4		
Logic Input High Voltage	EN/PSV High/High (Enabled, Psave Enabled)				3.1		V
EN/PSV Input Resistance	Sourcing		1.5				M Ω
	Sinking		1.0				M Ω
VTTEN Leakage Current					-1	+1	μA
Soft-Start							
VDDQ Soft-Start Ramp Time	EN/PSV High to PGD High		440				clks ⁽³⁾
VTT Soft-Start Ramp Rate ⁽⁶⁾			5.5				mV/ μs

POWER MANAGEMENT
Electrical Characteristics (Cont.)

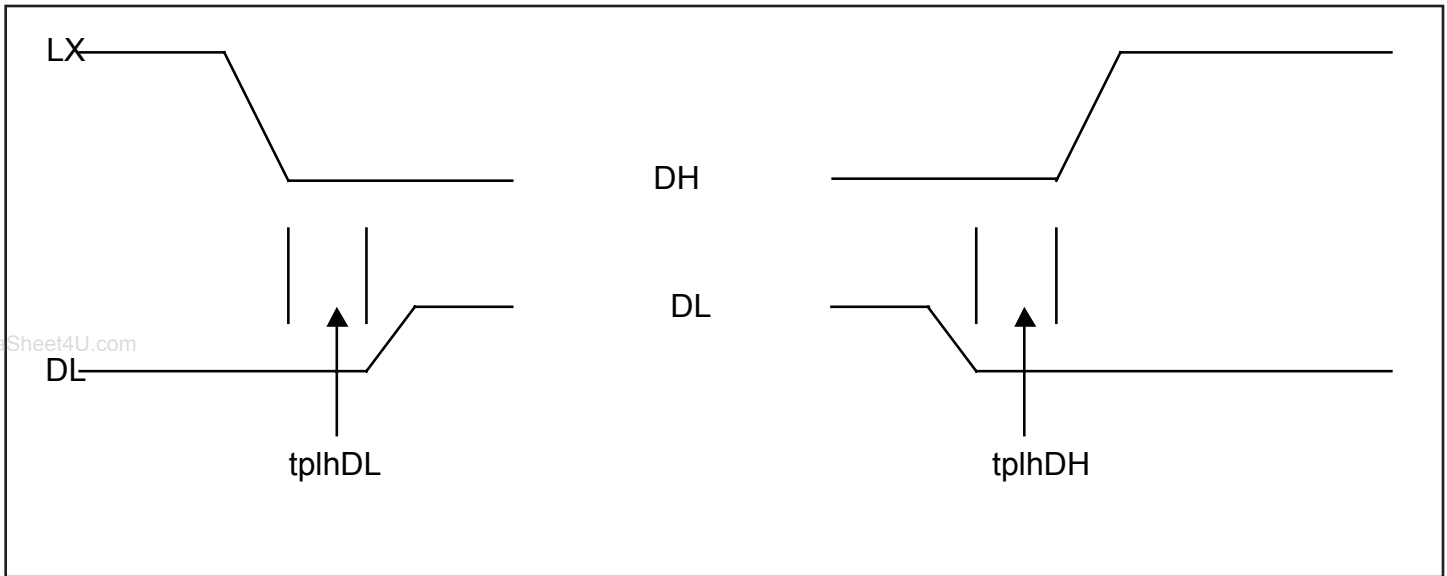
 TEST CONDITIONS: $V_{IN} = 15V$, $V_{CCA} = V_{DDP} = V_{TTEN} = EN/PSV = 5V$, $V_{DDQ} = V_{TTIN} = 1.8V$, $R_{TON} = 1M\Omega$, $T_{AMB} = -40$ TO $+85C$.

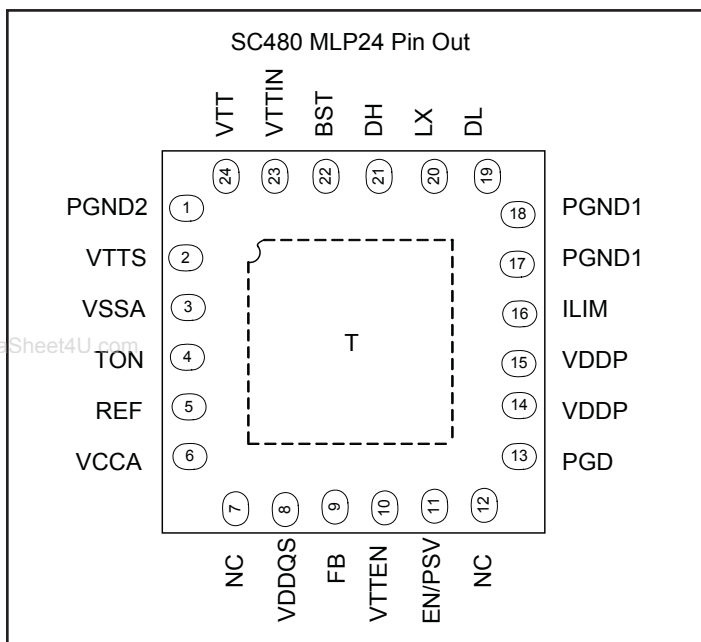
Parameter	Conditions	25°C			-40°C to 85°C		Units
		Min	Typ	Max	Min	Max	
FB Input Thresholds							
FB Logic Input Low	VDDQ Set for 2.5V (DDR1)		0.3				V
FB Logic Input High	VDDQ Set for 1.8V (DDR2)		VCCA - 0.7				V
Gate Drives							
Shoot-Thru Protection Delay ⁽⁴⁾⁽⁷⁾	DH or DL Rising		30				ns
DL Pull-Down Resistance	DL Low		0.8				Ω
DL Sink Current	$V_{DL} = 2.5V$		3.1				A
DL Pull-Up Resistance	DL High		2				Ω
DL Source Current	$V_{DL} = 2.5V$		1.3				A
DH Pull-Down Resistance	DH Low, BST - LX = 5V		2				Ω
DH Pull-Up Resistance ⁽⁸⁾	DH High, BST - LX = 5V		2				Ω
DH Sink/Source Current	$V_{DH} = 2.5V$		1.3				A
VTT Pull-Up Resistance	VTTs < REF		0.25				Ω
VTT Pull-Down Resistance	VTTs > REF		0.25				Ω
VTT Peak Sink/Source Current ⁽⁹⁾			3.6		2.0		A

Notes:

- 1) The VDDQ DC regulation level is higher than the FB error comparator threshold by 50% of the ripple voltage.
- 2) Using a current sense resistor, this measurement relates to PGND1 minus the source of the low-side MOSFET.
- 3) clks = switching cycles, consisting of one high side and one low side gate pulse.
- 4) Guaranteed by design.
- 5) Thermal shutdown latches both outputs (VTT and VDDQ) off, requiring VCCA or EN/PSV cycling to reset.
- 6) VTT soft-start ramp rate is limited to 5.5mV/ μ s typical. If the VDDQ/2 ramp rate is slower than 5.5mV/ μ sec, the VTT soft-start ramp will follow the VDDQ/2 ramp.
- 7) See Shoot-Through Delay Timing Diagram on Page 6.
- 8) Semtech's SmartDriver™ FET drive first pulls DH high with a pull-up resistance of 10 Ω (typ.) until LX = 1.5V (typ.). At this point, an additional pull-up device is activated, reducing the resistance to 2 Ω (typical). This creates a softer turn-on with minimal power loss, eliminating the need for an external gate or boost resistor.
- 9) Provided operation below $T_{j(MAX)}$ is maintained. VTT output current is also limited by internal MOSFET resistance which is typically 0.25 Ω at 25°C and which increases with temperature, and by available source voltage (typically VDDQ/2).

Shoot-Through Delay Timing Diagram



POWER MANAGEMENT
Pin Configuration

Ordering Information

Device ⁽²⁾	Package ⁽¹⁾
SC480IMLTRT	MLPQ-24
SC480EVB	Evaluation Board

Notes:

- 1) Only available in tape and reel packaging. A reel contains 3000 devices.
- 2) This product is fully WEEE and RoHS compliant.

Pin Description

Pin #	Pin Name	Pin Function
1	PGND2	Power ground for VTT output. Connect to thermal pad and ground plane.
2	VTTS	Sense pin for VTT. Connect to VTT at the load.
3	VSSA	Ground reference for analog circuitry. Connect to thermal pad.
4	TON	This pin is used to sense VBAT through a pull-up resistor, RTON, which sets the top MOSFET on-time. Bypass this pin with a 1nF capacitor to VSSA.
5	REF	Reference output. An internal resistor divider from VDDQS sets this voltage to 50% VDDQ (nominal). Bypass this pin with a series 10Ω/1μF to VSSA.
6	VCCA	Analog supply voltage input. Use a 10Ω/1μF RC filter from +5V to VSSA.
7	NC	No Connect.
8	VDDQS	Sense input for VDDQ. Used to set the on-time for the top MOSFET and also to set REF/VTT.
9	FB	Feedback select input for VDDQ. See FB Configuration Table.
10	VTTEN	Enable pin for VTT. Pull this pin low to disable VTT (REF remains present as long as VDDQ is present).
11	EN/PSV	Enable/Power Save input pin. Tie to ground to disable VDDQ. Tie to +5V to enable VDDQ and activate PSAVE mode. Float to enable VDDQ and activate continuous conduction mode. If floated, bypass to VSSA with a 10nF capacitor.
12	NC	No Connect.
13	PGD	Power good output for VDDQ. PGD is low if VDDQ is outside the power good thresholds. This pin is an open drain NMOS output and requires an external pull-up resistor.
14,15	VDDP	+5V supply voltage input for the VDDQ gate drivers.

POWER MANAGEMENT
Pin Description (Cont.)

16	ILIM	Current limit input pin. Connect to drain of low-side MOSFET for RDS(on) sensing or the source for resistor sensing through a threshold sensing resistor.
17,18	PGND1	Power ground for VDDQ switching circuits. Connect to thermal pad and ground plane.
19	DL	Gate drive output for the low side MOSFET switch.
20	LX	Phase node - the junction between the top and bottom FETs and the output inductor.
21	DH	Gate drive output for the high side MOSFET switch.
22	BST	Boost capacitor connection for the high side gate drive.
23	VTTIN	Input supply for the high side switch for VTT regulator. Decouple with a 1 μ F capacitor to PGND2.
24	VTT	Output of the linear regulator. Decouple with two (minimum) 10 μ F ceramic capacitors to PGND2, locating them directly across pins 24 and 1.
T	THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

Enable Control Logic

Enable Pin Status		Output Status		
EN/PSV ⁽¹⁾	VTTEN	VDDQ ⁽³⁾	VTT ⁽²⁾	REF ⁽²⁾
0	0	OFF, Discharged	OFF, Discharged	OFF, Discharged
0	1	OFF, Discharged	OFF, Discharged	OFF, Discharged
1	0	ON	OFF, High Impedance	ON
1	1	ON	ON	ON

Notes:

1) EN/PSV = 1 = EN/PSV high or floating.

2) Typical discharge resistances: VTT = 0.25 Ω . REF = 8 Ω .

3) VDDQ is discharged via external series resistance which must be added to SC480 internal discharge resistance to calculate discharge times. This is separate from any external load on VDDQ.

FB Configuration Table

The FB pin can be configured for fixed or adjustable output voltage as shown.

FB	VDDQ(V)	VREF & VTT (V)	Note
GND	2.5	VDDQS/2	DDR1
VCCA	1.8	VDDQS/2	DDR2
FB Resistors	Adjustable	VDDQS/2	1.5V < VDDQ < 3.0V

Block Diagram

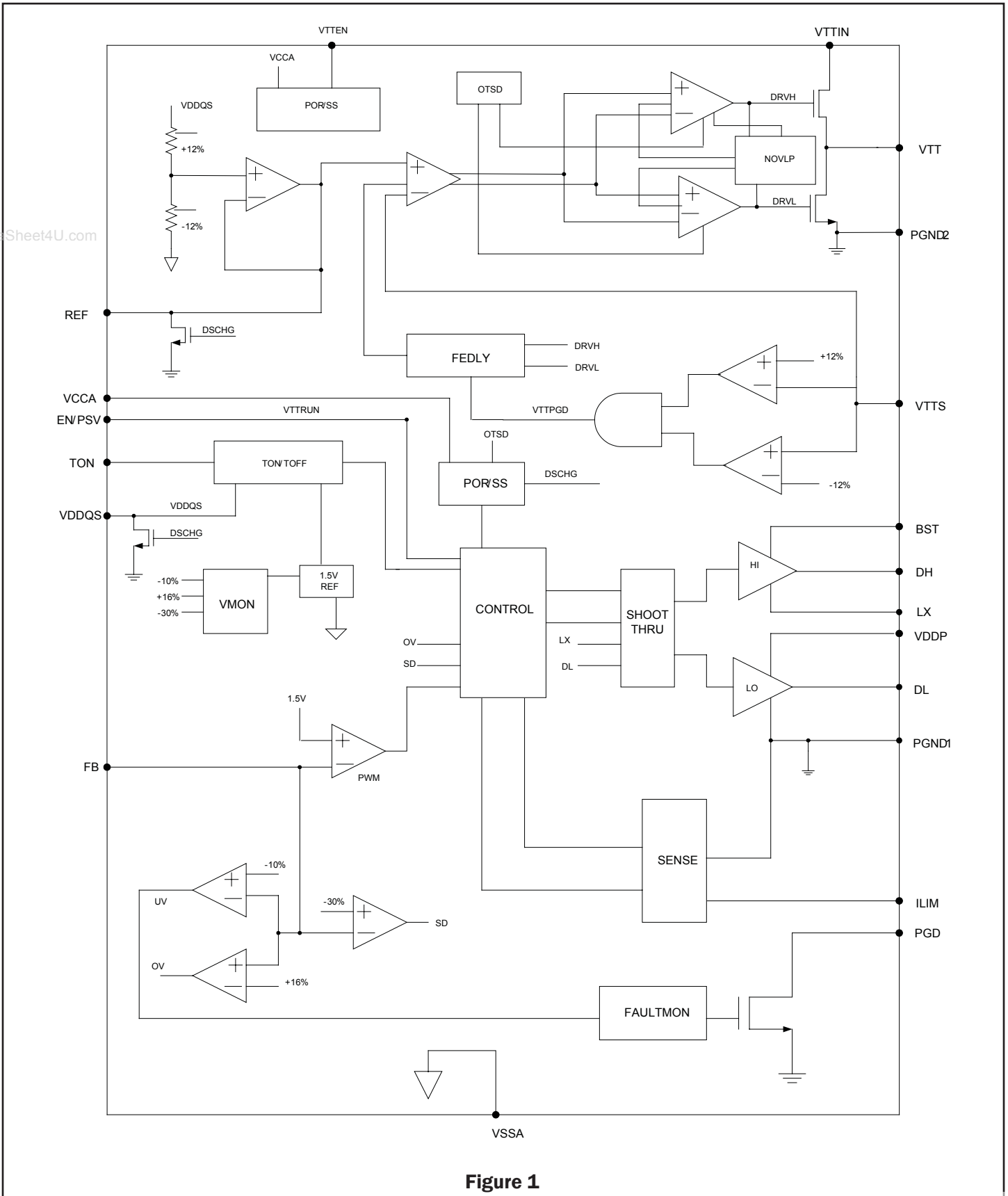


Figure 1

Application Information
+5V Bias Supplies

The SC480 requires an external +5V bias supply in addition to the battery. If stand-alone capability is required, the +5V supply can be generated with an external linear regulator. To minimize crosstalk, the controller has seven supply pins: VDDP (2 pins), PGND1 (2 pins), PGND2, VCCA and AGND.

The controller requires its own AGND plane which should be tied by a single trace to the negative terminal of the output capacitor. All external components referenced to AGND in the schematic should then be connected to the AGND plane. The supply decoupling capacitor should be tied between VCCA and AGND. A single 10Ω resistor should be used to decouple the VCCA supply from the main VDDP supply. PGND can then be a separate plane which is not used for routing analog traces. All PGND connections should connect directly to this plane with special attention given to avoiding indirect connections between AGND and PGND which will create ground loops. As mentioned above, the AGND plane must be connected to the PGND plane at the negative terminal of the output capacitor. The VDDP input provides power to the upper and lower gate drivers. A decoupling capacitor for the VDDP supply and PGND is recommended. No series resistor between VDDP and the 5 volt bias is required.

Pseudo-Fixed Frequency Constant On-Time PWM Controller

The PWM control method is a constant-on-time, pseudo-fixed frequency PWM controller, see Figure 1. The ripple voltage seen across the output capacitor's ESR provides the PWM ramp signal, eliminating the need for a current sense resistor. The on-time is determined by a one-shot whose period is proportional to output voltage, and inversely proportional to input voltage. A separate one-shot sets the minimum off-time (typically 425ns).

On-Time One-Shot (T_{ON})

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a proportional current. This current charges an internal on-time capacitor. The TON time is the time required for this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a nearly constant switching frequency without the need of a clock generator.

$$T_{ON} = 3.3 \times 10^{-12} \cdot (R_{TON} + 37 \times 10^3) \cdot \left(\frac{V_{OUT}}{V_{IN}} \right) + 50ns$$

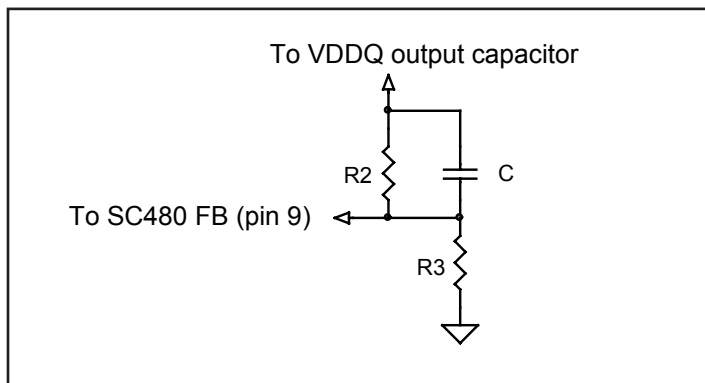
R_{TON} is a resistor connected between the input supply and the TON pin.

VDDQ/VTT Enable & Power-Save

The EN/PSV pin controls the VDDQ supply and the REF output (1/2 of VDDQ). VTEN enables the VTT supply. The VTT and VDDQ supplies may be enabled independently. When EN/PSV is tied to VCCA the VDDQ controller is enabled in power-save mode. When the EN/PSV pin is floated, an internal resistor divider activates the VDDQ controller with power-save disabled. If PSAVE is enabled, the SC480 PSAVE comparator looks for inductor current to cross zero on eight consecutive cycles. Once observed, the controller enters power-save and turns off the low-side MOSFET when the current crosses zero. To improve the efficiency and add hysteresis, the on-time is increased by 20% in power-save. The efficiency improvement at light loads more than offsets the disadvantage of slightly higher output ripple. If the inductor current does not cross zero on any switching cycle, the controller immediately exits power-save. Since the controller counts zero crossings, the converter can sink current as long as the current does not cross zero on eight consecutive cycles. This allows the output voltage to recover quickly in response to negative load steps even when power-save is enabled.

VDDQ Voltage Selection

VDDQ voltage is set using the FB pin. Grounding FB sets VDDQ to fixed 2.5V. Connecting FB to +5V sets VDDQ to fixed 1.8V. VDDQ can also be adjusted from 1.5 to 3.0V using external resistors, see Figure 2. The voltage at FB is then compared to the internal 1.5V reference.


Figure 2

Application Information

Referencing Figure 2, the equation for setting the output voltage is:

$$V_{OUT} = \left(1 + \frac{R_2}{R_3}\right) \cdot 1.5$$

Current Limit Circuit

Current limiting of the SC480 can be accomplished in two ways. The on-state resistance of the low-side MOSFETs can be used as the current sensing element, or a sense resistor in the low-side source can be used if greater accuracy is desired. R_{DS(ON)} sensing is more efficient and less expensive. In both cases, the R_{ILIM} resistor between the ILIM pin and LX sets the over-current threshold. This resistor R_{ILIM} is connected to a 10µA current source within the SC480 which is turned on when the low-side MOSFET turns on. When the voltage drop across the sense resistor or low-side MOSFET equals the voltage across the R_{ILIM} resistor, current limit will activate. The high-side MOSFET will not be allowed to turn on until the voltage drop across the sense element (resistor or MOSFET) falls below the voltage across the R_{ILIM} resistor.

The current sensing circuit actually regulates the inductor valley current, see Figure 3. This means that if the current limit is set to 10A, the peak current through the inductor would be 10A plus the peak ripple current, and the average current through the inductor would be 10A plus 1/2 the peak-to-peak ripple current.

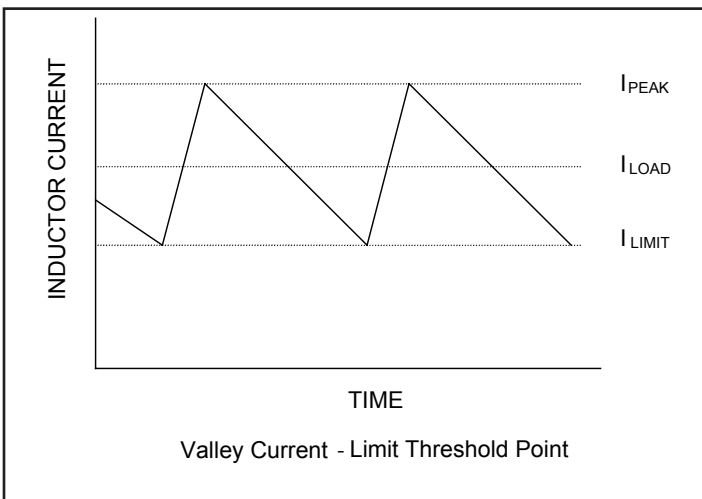


Figure 3

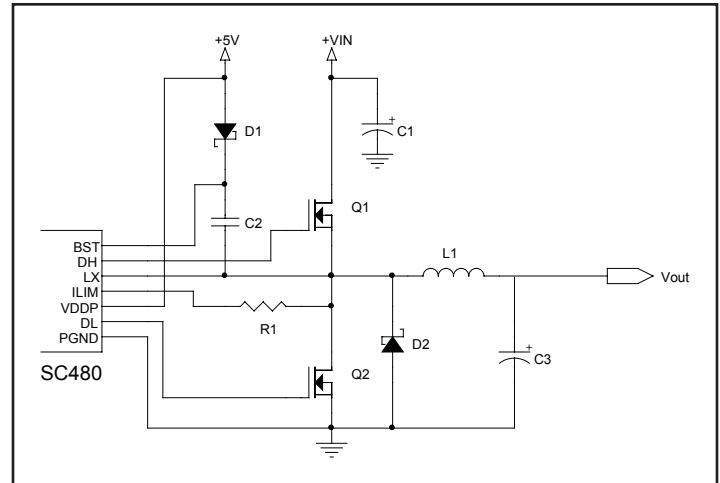


Figure 4

The schematic of R_{DS(ON)} sensing circuit is shown in Figure 4 with R_{ILIM} = R1 and R_{DS(ON)} of Q2.

Similarly, for resistor sensing, the current through the lower MOSFET and the source sense resistor develops a voltage that opposes the voltage developed across R_{ILIM}. When the voltage developed across the R_{SENSE} resistor reaches voltage drop across R_{ILIM}, an over-current exists and the high-side MOSFET will not be allowed to turn on. The over-current equation when using an external sense resistor is:

$$I_{LOC}(\text{Valley}) = 10\mu\text{A} \cdot \frac{R_{ILIM}}{R_{SENSE}}$$

Schematic of resistor sensing circuit is shown in Figure 5 with R_{ILIM} = R1 and R_{SENSE} = R4.

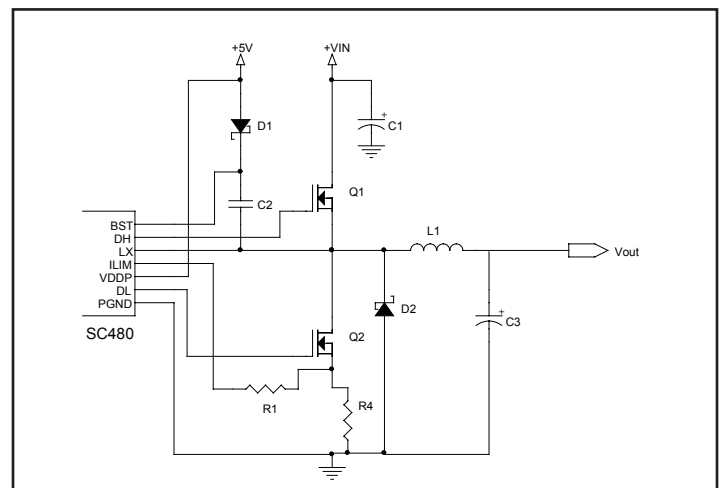


Figure 5

Application Information (Cont.)

Power Good Output

The VDDQ controller has a power good (PGD) output. Power good is an open-drain output and requires a pull-up resistor. When the output voltage is +16%/-10% from its nominal voltage, PGD gets pulled low. It is held low until the output voltage returns to within +16%/-10% of nominal. PGD is also held low during start-up and will not be allowed to transition high until soft-start is over and the output reaches 90% of its set voltage. There is a 5 μ s delay built into the PGD circuit to prevent false transitions.

Output Over-Voltage Protection

When the VDDQ output exceeds 16% of its set voltage, the low-side MOSFET is latched on. It stays latched and the SMPS stays off until the EN/PSV input is toggled or VCCA is recycled. There is a 5 μ s delay built into the OV protection circuit to prevent false transitions. During a VDDQ OV shutdown, VTT is alive until VDDQ falls to typically 0.4V, at which point VTT is tri-stated.

When VTT exceeds 12% above its set voltage, the VTT regulator will tristate. There is a 50 μ s delay to prevent false OV trips due to transients or noise. The VDDQ regulator continues to operate after VTT OV shutdown. The VTT OV condition is removed by toggling VTEN or EN/PSV, or by recycling VCCA.

Smart Over-Voltage Protection

In some applications, the active loads on VDDQ can actually leak current into VDDQ. If PSAVE mode is enabled at very light loading, this leak can cause VDDQ to slowly rise and reach the OV threshold, causing a hard shutdown. To prevent this, the SC480 uses Smart OVP to prevent this. When VDDQ exceeds 8% above nominal, DL drives high to turn on the low-side MOSFET, which starts to draw current from VDDQ via the inductor. When VDDQ drops to the FB trip point, a normal TON switching cycle begins. This prevents a hard OV shutdown.

Output Under-Voltage Protection

When VDDQ falls 30% below its set point for eight clock cycles, the VDDQ output is shut off; the DL/DH drives are pulled low to tristate the MOSFETS, and the SMPS stays off until the Enable input is toggled or VCCA is recycled. When VTT is 12% below its set voltage the VTT output is tristated. There is a 50 μ s delay for VTT built into the UV protection circuits to prevent false transitions.

POR, UVLO and Soft-Start

An internal power-on reset (POR) occurs when VCCA exceeds 3V, resetting the fault latch and soft-start counter, and preparing the PWM for switching. VCCA under-voltage lockout (UVLO), circuitry inhibits switching and tristates the drivers until VCCA rises above 4.2V. At this time the circuit will come out of UVLO and begin switching and the soft-start circuit will progressively limit the output current over a pre-determined time period. The ramp occurs in four steps: 25%, 50%, 75% and 100%, thereby limiting the slew rate of the output voltage. There is 100mV of hysteresis built into the UVLO circuit and when VCCA falls to 4.1V the output drivers are shutdown and tristated.

MOSFET Gate Drivers

The DH and DL drivers are optimized for moderate, high-side, and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off, and conversely, monitors the DH output and prevents the low-side MOSFET from turning on until DH is fully off. (*Note: be sure there is low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.*)

Design Procedure

Prior to designing a switch mode supply for a notebook computer, the input voltage, load current, switching frequency and inductor ripple current must be specified.

Input Voltage Range

The maximum input voltage (V_{IN_MAX}) is determined by the highest AC adaptor voltage. The minimum input voltage (V_{IN_MIN}) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches.

Maximum Load Current

There are two values of load current to consider: continuous load current and peak load current. Continuous load current has more to do with thermal stresses and therefore drives the selection of input capacitors, MOSFETs and commutation diodes. Peak load current determines instantaneous component stresses and filtering requirements such as, inductor saturation, output capacitors and design of the current limit circuit.

Application Information (Cont.)
Switching Frequency

Switching frequency determines the trade-off between size and efficiency. Higher frequency increases switching losses in the MOSFETs, since losses are a function of $F \cdot V_{IN}^2$. Knowing the maximum input voltage and budget for MOSFET switches usually dictates the final design.

Inductor Ripple Current

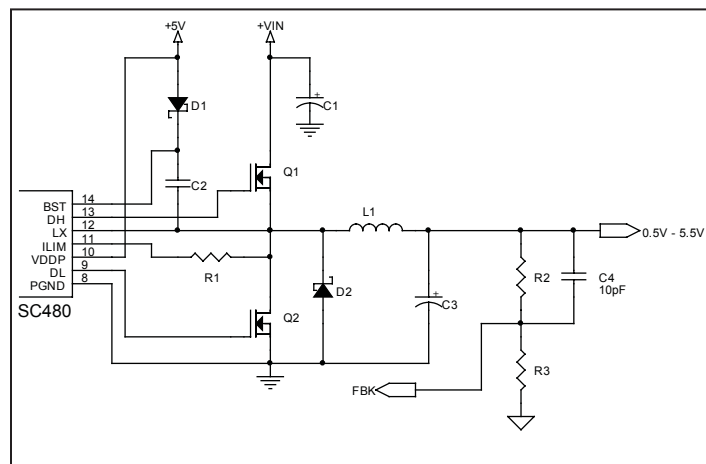
Low inductor values result in smaller size, but create higher ripple current and are less efficient because of the high AC current flowing in the inductor. Higher inductor values do reduce the ripple current and are more efficient, but are larger and more costly. The selection of the ripple current is based on the maximum output current and tends to be between 20% to 50% of the maximum load current. Again, cost, size and efficiency all play a part in the selection process.

Stability Considerations

Unstable operation shows up in two related but distinctly different ways: double pulsing and fast-feedback loop instability. Double-pulsing occurs due to noise on the output or because the ESR is too low, causing insufficient voltage ramp in the output signal. This causes the error amplifier to trigger prematurely after the 400ns minimum off-time has expired. Double-pulsing will result in higher ripple voltage at the output, but in most cases is harmless. In some cases, however, double-pulsing can indicate the presence of loop instability, which is caused by insufficient ESR. One simple way to solve this problem is to add some trace resistance in the high current output path. A side effect of doing this is output voltage droop with load. Another way to eliminate doubling-pulsing is to add a 10pF capacitor across the upper feedback resistor divider network. This is shown in Figure 6, by capacitor C4 in the schematic. This capacitance should be left out until confirmation that double-pulsing exists. Adding this capacitance will add a zero in the transfer function and should eliminate the problem. It is best to leave a spot on the PCB in case it is needed.

Loop instability can cause oscillations at the output as a response to line or load transients. These oscillations can trip the over-voltage protection latch or cause the output voltage to fall below the tolerance limit.

The best way for checking stability is to apply a zero to full load transient and observe the output voltage ripple envelope for overshoot and ringing. Over one cycle of ringing after the initial step is a sign that the ESR should be increased.


Figure 6
SC480 ESR Requirements

The constant on-time control used in the SC480 regulates the ripple voltage at the output capacitor. This signal consists of a term generated by the output ESR of the capacitor and a term based on the increase in voltage across the capacitor due to charging and discharging during the switching cycle. The minimum ESR is set to generate the required ripple voltage for regulation. For most applications the minimum ESR ripple voltage is dominated by PCB layout and the properties of SP or POSCAP type output capacitors. For applications using ceramic output capacitors, the absolute minimum ESR must be considered. If the ESR is low enough the ripple voltage is dominated by the charging of the output capacitor. This ripple voltage lags the on-time due to the LC poles and can cause double pulsing if the phase delay exceeds the off-time of the converter. Referring to Figure 5 on Page 11, the equation for the minimum ESR as a function of output capacitance and switching frequency and duty cycle is:

$$ESR > \left(\frac{V_{OUT}}{1.5V} \right) \cdot \left(\frac{1 + 3 \cdot \left(\frac{F_s - 200000}{F_s} \right)}{2 \cdot \pi \cdot C_{out} \cdot F_s \cdot (1 - D)} \right)^2$$

Application Information (Cont.)
Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 400nS (typical) Minimum Off-time One-shot. For best dropout performance, use the slowest on-time setting of 200KHz. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The IC duty-factor limitation is given by:

$$\text{DUTY} = \frac{\text{TON(MIN)}}{\text{TON(MIN)} + \text{TOFF (MAX)}}$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case dropout duty-factor calculations.

SC480 System DC Accuracy (VDDQ Controller)

Three IC parameters affect VDDQ accuracy: the internal 1.5V reference, the error comparator offset voltage, and the switching frequency variation with line and load.

The internal 1%, 1.5V reference contains two error components, a 0.5% DC error and a 0.5% supply and temperature error. The error comparator offset is trimmed so that it trips when the feedback pin is nominally 1.5 volts +/-1% at room temperature. The comparator offset trim compensates for any DC error in the reference. Thus, the percentage error is the sum of the reference variation over supply and temperature and the offset in the error comparator, or 1.5% total.

The on-time pulse in the SC480 is calculated to give a pseudo-fixed frequency. Nevertheless, some frequency variation with line and load can be expected. This variation changes the output ripple voltage. Because constant on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, If the output ripple is 50mV with VIN = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with VIN = 25 volts, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation it is often desirable to use passive droop. Take the feedback directly from the output side of the inductor, incorporating a small amount

of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced.

Board components and layout also influence DC accuracy. The use of 1% feedback resistors contributes up to 1% error. If tighter DC accuracy is required use 0.1% feedback resistors.

The output inductor value may change with current. This will change the output ripple and thus the DC output voltage (it will not change the frequency).

Switching frequency variation with load can be minimized by choosing lower RDS_{ON} MOSFETs. High RDS_{ON} MOSFETs will cause the switching frequency to increase as the load current increases. This will reduce the ripple and thus the DC output voltage. This inherent droop should be considered when deciding if passive droop is required, or if passive droop is desired in order to further reduce the output capacitance.

Output DC Accuracy (VTT Output)

The VTT accuracy compared to VDDQ is determined by two parameters: the REF output accuracy, and the VTT output accuracy with respect to REF. The REF output is generated internally from the VDDQS (sense input), and tracks VDDQS with 2% accuracy. This REF output becomes the reference for the VTT regulator. The VTT regulator then tracks REF within +/-40mV (typically zero). The total VTT/VDDQ tracking accuracy is then:

$$\text{VTT error} = \frac{\text{VDDQS}}{2} \bullet \pm 0.02 \pm 40\text{mV}$$

DDR Reference Buffer

The reference buffer is capable of sourcing 10mA. The reference buffer has a class A output stage and therefore will not sink significant current; there is an internal 50 kΩ (typical) pulldown to ground. If higher current sinking is required, an external pulldown resistor should be added. Make sure that the ground side of this pulldown is tied to the VTT ground plane near the PGND2 pin.

Application Information (Cont.)

For stability, place a 10Ω/1μF series combination from REF to VSSA. If REF load capacitance exceeds 1μF, place at least 10Ω in series with the load capacitance to prevent instability. It is possible to use only one 10Ω resistor, by connecting the load capacitors in parallel with the 1μF, and connecting the load REF to the capacitor side of the 10Ω resistor. (See the Typical Application Circuit on Page 1.) Note that this resistor creates an error term when REF has a DC load. In most applications this is not a concern since the DC load on REF is negligible.

Design Procedure

Prior to designing a switching output and making component selections, it is necessary to determine the input voltage range and output voltage specifications. To demonstrate the procedure, the output for the schematic in Figure 7 on page 18 will be designed.

The maximum input voltage ($V_{BAT(MAX)}$) is determined by the highest AC adaptor voltage. The minimum input voltage ($V_{BAT(MIN)}$) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches. For the purposes of this design example we will use a VBAT range of 8V to 20V to design VDDQ.

Four parameters are needed for the design:

1. Nominal output voltage, V_{OUT} . We will use 1.8V with internal feedback resistors (FB pin tied to VCCA).
2. Static (or DC) tolerance, TOL_{ST} (we will use +/-2%).
3. Transient tolerance, TOL_{TR} and size of transient (we will use +/-8% for a 10A to 5A load release for this demonstration).
4. Maximum output current, I_{OUT} (we will design for 10A).

Switching frequency determines the trade-off between size and efficiency. Increased frequency increases the switching losses in the MOSFETs, and losses are a function of V_{BAT}^2 . Knowing the maximum input voltage and budget for MOSFET switches usually dictates where the design ends up. The default R_{TON} values of 1MΩ and 715kΩ are suggested only as a starting point.

The first thing to do is to calculate the on-time, t_{ON} , at $V_{BAT(MIN)}$ and $V_{BAT(MAX)}$, since this depends only upon V_{BAT} , V_{OUT} and R_{TON} .

$$t_{ON_VBAT(MIN)} = \left[3.3 \cdot 10^{-12} \cdot (R_{TON} + 37 \cdot 10^3) \cdot \frac{V_{OUT}}{V_{BAT(MIN)}} \right] + 50 \cdot 10^{-9} \text{ s}$$

and,

$$t_{ON_VBAT(MAX)} = \left[3.3 \cdot 10^{-12} \cdot (R_{TON} + 37 \cdot 10^3) \cdot \frac{V_{OUT}}{V_{BAT(MAX)}} \right] + 50 \cdot 10^{-9} \text{ s}$$

From these values of t_{ON} we can calculate the nominal switching frequency as follows:

$$f_{SW_VBAT(MIN)} = \frac{V_{OUT}}{(V_{BAT(MIN)} \cdot t_{ON_VBAT(MIN)})} \text{ Hz}$$

and,

$$f_{SW_VBAT(MAX)} = \frac{V_{OUT}}{(V_{BAT(MAX)} \cdot t_{ON_VBAT(MAX)})} \text{ Hz}$$

t_{ON} is generated by a one-shot comparator that samples V_{BAT} via R_{TON} , converting this to a current. This current is used to charge an internal 3.3pF capacitor to V_{OUT} . The equations above reflect this along with any internal components or delays that influence t_{ON} . For our example we select $R_{TON} = 1\text{M}\Omega$:

$$t_{ON_VBAT(MIN)} = 820\text{ns} \text{ and } t_{ON_VBAT(MAX)} = 358\text{ns}$$

$$f_{SW_VBAT(MIN)} = 274\text{kHz} \text{ and } f_{SW_VBAT(MAX)} = 251\text{kHz}$$

Now that we know t_{ON} we can calculate suitable values for the inductor. To do this we select an acceptable inductor ripple current. The calculations below assume 50% of I_{OUT} which will give us a starting place.

$$L_{VBAT(MIN)} = (V_{BAT(MIN)} - V_{OUT}) \cdot \frac{t_{ON_VBAT(MIN)}}{(0.5 \cdot I_{OUT})} \text{ H}$$

and,

$$L_{VBAT(MAX)} = (V_{BAT(MAX)} - V_{OUT}) \cdot \frac{t_{ON_VBAT(MAX)}}{(0.5 \cdot I_{OUT})} \text{ H}$$

For our example:

$$L_{VBAT(MIN)} = 1.02\mu\text{H} \text{ and } L_{VBAT(MAX)} = 1.30\mu\text{H},$$

Application Information (Cont.)

We will select an inductor value of 1.5μH to reduce the ripple current, which can be calculated as follows:

$$I_{\text{RIPPLE_VBAT(MIN)}} = \left(V_{\text{BAT(MIN)}} - V_{\text{OUT}} \right) \cdot \frac{t_{\text{ON_VBAT(MIN)}}}{L} A_{\text{P-P}}$$

and,

$$I_{\text{RIPPLE_VBAT(MAX)}} = \left(V_{\text{BAT(MAX)}} - V_{\text{OUT}} \right) \cdot \frac{t_{\text{ON_VBAT(MAX)}}}{L} A_{\text{P-P}}$$

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For our example:

$$I_{\text{RIPPLE_VBAT(MIN)}} = 3.39A_{\text{P-P}} \text{ and } I_{\text{RIPPLE_VBAT(MAX)}} = 4.34A_{\text{P-P}}$$

From this we can calculate the minimum inductor current rating for normal operation:

$$I_{\text{INDUCTOR(MIN)}} = I_{\text{OUT(MAX)}} + \frac{I_{\text{RIPPLE_VBAT(MAX)}}}{2} A_{\text{(MIN)}}$$

For our example:

$$I_{\text{INDUCTOR(MIN)}} = 12.2A_{\text{(MIN)}}$$

Next we will calculate the maximum output capacitor equivalent series resistance (ESR). This is determined by calculating the remaining static and transient tolerance allowances. Then the maximum ESR is the smaller of the calculated static ESR ($R_{\text{ESR_ST(MAX)}}$) and transient ESR ($R_{\text{ESR_TR(MAX)}}$):

$$R_{\text{ESR_ST(MAX)}} = \frac{(\text{ERR}_{\text{ST}} - \text{ERR}_{\text{DC}}) \cdot 2}{I_{\text{RIPPLE_VBAT(MAX)}}} \text{ Ohms}$$

Where ERR_{ST} is the static output tolerance and ERR_{DC} is the DC error. The DC error will be 1% plus the tolerance of the internal feedback. (Use 2% for external feedback, which is 1% plus another 1% for the external resistors.)

For our example:

$$\text{ERR}_{\text{ST}} = 36\text{mV} \text{ and } \text{ERR}_{\text{DC}} = 18\text{mV}, \text{ therefore,}$$

$$R_{\text{ESR_ST(MAX)}} = 8.3\text{m}\Omega$$

$$R_{\text{ESR_TR(MAX)}} = \frac{\left(\text{ERR}_{\text{TR}} - \text{ERR}_{\text{DC}} \right)}{\left(I_{\text{TRANS}} + \frac{I_{\text{RIPPLE_VBAT(MAX)}}}{2} \right)} \text{ Ohms}$$

where ERR_{TR} is the transient output tolerance. For this case, I_{TRANS} is the load transient of 5A (10A - 5A).

For our example:

$$\text{ERR}_{\text{TR}} = 144\text{mV} \text{ and } \text{ERR}_{\text{DC}} = 18\text{mV}, \text{ therefore,}$$

$$R_{\text{ESR_TR(MAX)}} = 17.6\text{m}\Omega \text{ for a full 5A load transient.}$$

We will select a value of 6mΩ maximum for our design, which would be achieved by using two 12mΩ output capacitors in parallel. Now that we know the output ESR we can calculate the output ripple voltage:

$$V_{\text{RIPPLE_VBAT(MIN)}} = R_{\text{ESR}} \cdot I_{\text{RIPPLE_VBAT(MIN)}} V_{\text{P-P}}$$

and,

$$V_{\text{RIPPLE_VBAT(MAX)}} = R_{\text{ESR}} \cdot I_{\text{RIPPLE_VBAT(MAX)}} V_{\text{P-P}}$$

For our example:

$$V_{\text{RIPPLE_VBAT(MAX)}} = 20\text{mV}_{\text{P-P}} \text{ and } V_{\text{RIPPLE_VBAT(MIN)}} = 26\text{mV}_{\text{P-P}}$$

Note that in order for the device to regulate in a controlled manner, the ripple content at the feedback pin, V_{FB} , should be approximately 15mV_{P-P} at minimum V_{BAT} and worst case no smaller than 10mV_{P-P}. Note that the voltage ripple at FB is smaller than the voltage ripple at the output capacitor, due to the resistor divider. Also, when using internal feedback (FB pin tied to 5V or GND), the FB resistor divider is actually inside the IC. If $V_{\text{RIPPLE_VBAT(MIN)}}$ as seen at the FB point is less than 15mV_{P-P} - whether internal or external FB is used - the above component values should be revisited in order to improve this. For our example, since the internal divider reduces the ripple signal by a factor of (1.5V/1.8V), the internal FB ripple values are then 17mV and 22mV, which is above the 15mV minimum.

When using external feedback, and with VDDQ greater than 1.5V, a small capacitor, C_{TOP} , can be used in parallel with the top feedback resistor, R_{TOP} , in order to ensure that ripple at VFB is large enough. C_{TOP} should not be greater than 100pF. The value of C_{TOP} can be calculated as follows, where R_{BOT} is the bottom feedback resistor. Firstly calculating the value of Z_{TOP} required:

Application Information (Cont.)

$$Z_{TOP} = \frac{R_{BOT}}{0.015} \cdot (V_{RIPPLE_VBAT(MIN)} - 0.015) \text{ Ohms}$$

Secondly calculating the value of C_{TOP} required to achieve this:

$$C_{TOP} = \frac{\left(\frac{1}{Z_{TOP}} - \frac{1}{R_{TOP}} \right)}{2 \cdot \pi \cdot f_{SW_VBAT(MIN)}} \text{ F}$$

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Since our example uses internal feedback, this method cannot be used, however the voltage seen at the internal FB point is already greater than 15mV.

Next we need to calculate the minimum output capacitance required to ensure that the output voltage does not exceed the transient maximum limit, $POSLIM_{TR}$, starting from the actual static maximum, $V_{OUT_ST_POS}$, when a load release occurs:

$$V_{OUT_ST_POS} = V_{OUT} + ERR_{DC} V$$

For our example:

$$V_{OUT_ST_POS} = 1.818V,$$

$$POSLIM_{TR} = V_{OUT} \cdot TOL_{TR} V$$

Where TOL_{TR} is the transient tolerance. For our example:

$$POSLIM_{TR} = 1.944V,$$

The minimum output capacitance is calculated as follows:

$$I_{init} = I_{OUT(MAX)} + \frac{I_{RIPPLE_VBAT(MAX)}}{2} A$$

and,

$$C_{OUT(MIN)} = L \cdot \frac{(I_{init})^2 - (I_{final})^2}{(POSLIM_{TR}^2 - V_{OUT_ST_POS}^2)} F$$

This calculation assumes the condition of a full-load to no-load step transient occurring when the inductor current is

at its highest. The capacitance required for smaller transient steps may be calculated by substituting the desired current for the I_{final} term. In this case I_{final} is set for 5A. For our example:

$$C_{OUT(MIN)} = 392\mu F.$$

We will select 440 μ F, using two 220 μ F, 12m Ω capacitors in parallel.

Next we calculate the RMS input ripple current, which is largest at the minimum battery voltage:

$$I_{IN(RMS)} = \sqrt{V_{OUT} \cdot (V_{BAT(MIN)} - V_{OUT})} \cdot \frac{I_{OUT}}{V_{BAT_MIN}} A_{RMS}$$

For our example:

$$I_{IN(RMS)} = 4.17A_{RMS}$$

Input capacitors should be selected with sufficient ripple current rating for this RMS current, for example a 10 μ F, 1210 size, 25V ceramic capacitor can handle approximately 3A $_{RMS}$. Refer to manufacturer's data sheets and derate appropriately.

Finally, we calculate the current limit resistor value. As described in the current limit section, the current limit looks at the "valley current", which is the average output current minus half the ripple current.

$$I_{VALLEY} = I_{OUT} - \frac{I_{RIPPLE_VBAT(MIN)}}{2} A$$

The ripple at low battery voltage is used because we want to make sure that current limit does not occur under normal operating conditions.

$$R_{ILIM} = (I_{VALLEY} \cdot 1.2) \cdot \frac{R_{DS(ON)} \cdot 1.4}{10 \cdot 10^{-6}} \text{ Ohms}$$

For our example:

$$I_{VALLEY} = 8.31A, R_{DS(ON)} = 4m\Omega, \text{ giving } R_{ILIM} = 5.62k\Omega$$

Application Information (Cont.)
Thermal Considerations

The junction temperature of the device may be calculated as follows:

$$T_J = T_{AMB} + \theta_{JA}$$

where T_J is the junction temperature, T_{AMB} is the ambient temperature, P_D is the total SC480 device dissipation,

The SC480 device dissipation can be determined using:

$$P_D = V_{CCA} \cdot I_{CCA} + V_{DDP} \cdot I_{DDP} + V_{TT} \cdot |I_{TT}|$$

The first two terms are losses for the analog and gate drive circuits and generally do not present a thermal problem. Typical I_{CCA} (V_{CCA} operating current) is roughly 1.5mA, which creates 7.5mW loss from the 5V V_{CCA} supply. The V_{DDP} supply current is used to drive the MOSFETs and can be much higher, on the order of 30mA, which can create up to 150mW of dissipation.

The last term, $V_{TT} \cdot |I_{TT}|$, is the most significant term from a thermal standpoint. The V_{TT} regulator is a linear device and will dissipate power proportional to the V_{TT} current and the voltage drop across the regulator. If $V_{TT} = V_{DDQ}/2$, then the voltage drop across the regulator is always $V_{DDQ}/2$, regardless of whether the regulator is sinking or sourcing current. In either case the power lost in the V_{TT} regulator is $V_{TT} \cdot |I_{TT}|$. The average or long-term value for I_{TT} should be used.

The thermal resistance of the MLPQ package is affected by PCB layout and the available ground planes and vias which conduct heat away. A typical value is 29°C/watt.

Example: $I_{CCA} = 1.5\text{mA}$ $I_{DDP} = 25\text{mA}$
 $V_{CCA} = V_{DDP} = 5\text{V}$
 $V_{TT} = 1.25\text{V}$
 $I_{TT} = 0.75\text{A}$ (average)
 Ambient = 45 degrees C
 Thermal resistance = 29

$$P_D = 5\text{V} \cdot 0.0015\text{A} + 5\text{V} \cdot 0.025\text{A} + 0.9\text{V} \cdot |0.75\text{A}|$$

$$P_D = 0.808\text{W}$$

$$T_J = T_{AMB} + P_D \cdot T_{JA} = 45 + 0.808\text{W} \cdot 29^\circ\text{C/W} = 68.4^\circ\text{C}$$

Layout Guidelines

One (or more) ground planes are recommended to minimize the effect of switching noise and copper losses, and maximize heat dissipation. The IC ground reference, V_{SSA} , should be connected to $PGND1$ and $PGND2$ as a star connection at the thermal pad, which in connects using 4 vias to the ground plane. All components that are referenced to V_{SSA} should connect to it directly on the chip side, and not through the ground plane.

VDDQ: The feedback trace must be kept far away from noise sources such as switching nodes, inductors and gate drives. Route the feedback trace in a quiet layer if possible, from the output capacitor back to the chip. Chip supply decoupling capacitors (V_{CCA} , V_{DDP}) should be located next to the pins (V_{CCA}/V_{SSA} , $V_{DDP}/PGND1$) and connected directly to them on the same side.

VTT: Because of the high bandwidth of the V_{TT} regulator, proper component placement and routing is essential to prevent unwanted high-frequency oscillations which can be caused by parasitic inductance and noise. The input capacitors should be located at the V_{TT} input pins (V_{TTIN} and $PGND2$), as close as possible to the chip to minimize parasitics. Output capacitors should be directly located at the V_{TT} output pins (V_{TT} and $PGND2$). The routing of the feedback signal V_{TTS} is critical. The trace from V_{TTS} (pin 2) should be connected directly to the output capacitor that is farthest from V_{TT} (pin24); route this signal away from noise sources such as the V_{DDQ} power train or high-speed digital signals.

The switcher power section should connect directly to the ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses. Make all the connections on one side of the PCB using wide copper filled areas if possible. Do not use "minimum" land patterns for power components. Minimize trace lengths between the gate drivers and the gates of the MOSFETs to reduce parasitic impedances (and MOSFET switching losses); the low-side MOSFET is most critical. Maintain a length to width ratio of <20:1 for gate drive signals. Use multiple vias as required by current handling requirement (and to reduce parasitics) if routed on more than one layer. Current sense connections must always be made using Kelvin connections to ensure an

Application Information (Cont.)

accurate signal. The layout can be generally considered in three parts; the control section referenced to VSSA, the VTT output, and the switcher power section.

Looking at the control section first, locate all components referenced to VSSA on the schematic and place these components at the chip. Connect VSSA using a wide (>0.020") trace. Very little current flows in the chip ground therefore large areas of copper are not needed. Connect the VSSA pin directly to the thermal pad under the device as the only connection from PGND1 and PGND2 from VSSA.

Decoupling capacitors for VCCA/VSSA and VDDP/PGND1 should be placed as close as possible to the chip. The feedback components connected to FB, along with the VDDQ sense components, should also be located at the chip. The feedback trace from the VDDQ output should route from the top of the output capacitors, in a quiet layer back to the FB components.

Next, looking at the switcher power section, there are a few key guidelines to follow:

1. There should be a very small input loop, well decoupled.
2. The phase node should be a large copper pour, but still compact since this is the noisiest node.
3. Input power ground and output power ground should not connect directly, but through the ground planes instead.

Finally, connecting the control and switcher power sections should be accomplished as follows:

1. Route VDDQ feedback trace in a "quiet" layer, away from noise sources.
2. Route DL, DH and LX (low side FET gate drive, high side FET gate drive and phase node) to the chip using wide traces with multiple vias if using more than one layer. These connections are to be as short as possible for loop minimization, with a length to width ratio less than 20:1 to minimize impedance. DL is the most critical gate drive, with power ground as its return path. LX is the noisiest node in the circuit, switching between VBAT and ground at high frequencies, thus should be kept as short as practical. DH has LX as its return path.
3. BST is also a noisy node and should be kept as short as possible.
4. Connect PGND1 pins on the chip directly to the VDDP decoupling capacitor and then drop vias directly to the ground plane. Locate the current limit resistor at the chip with a kelvin connection to the phase node.

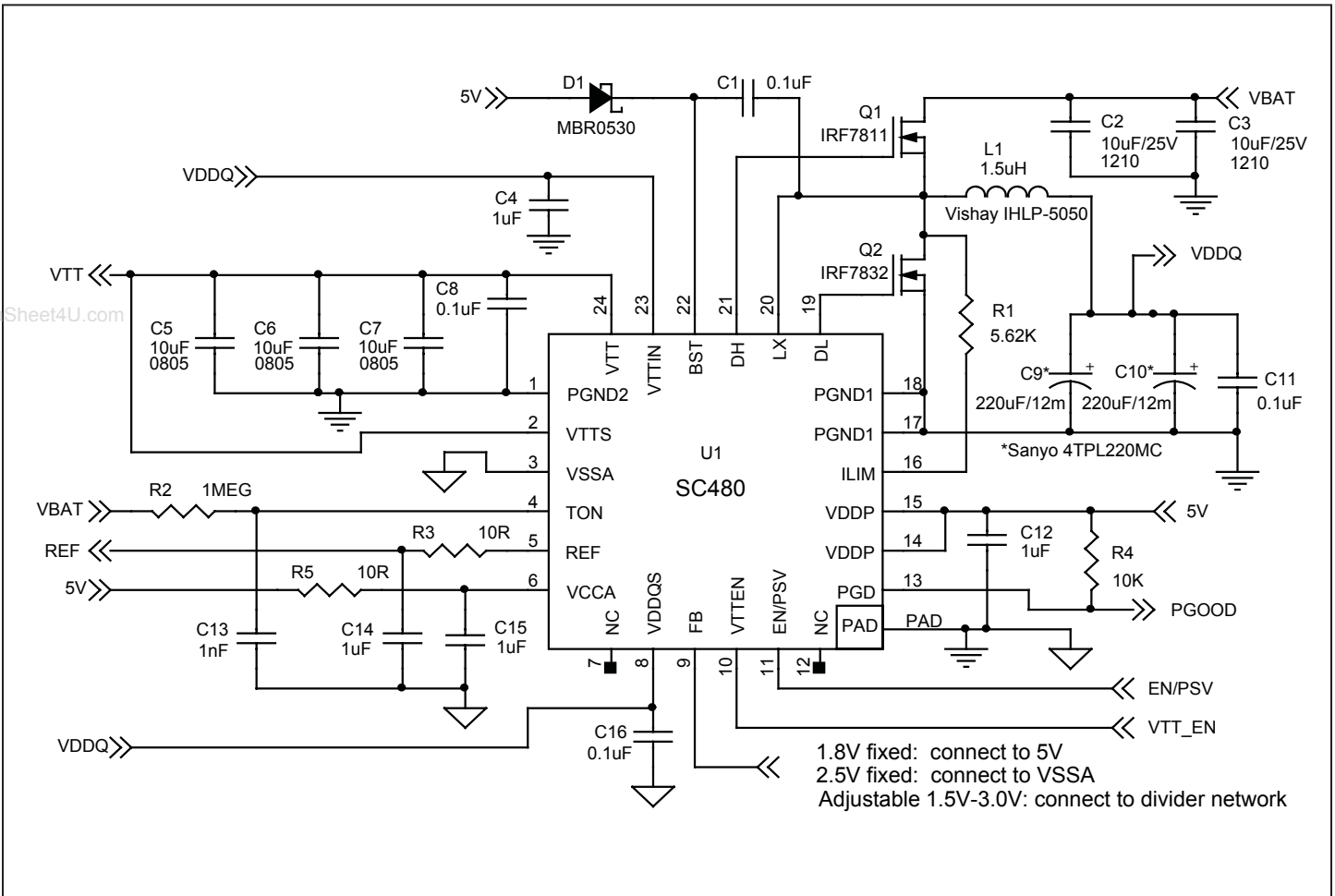
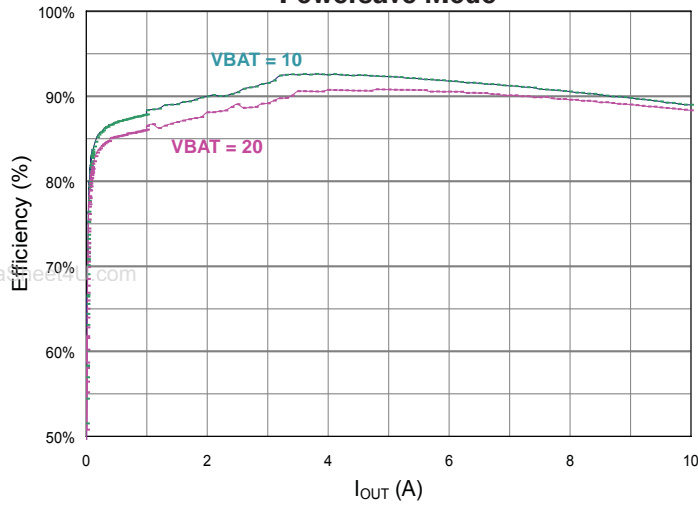


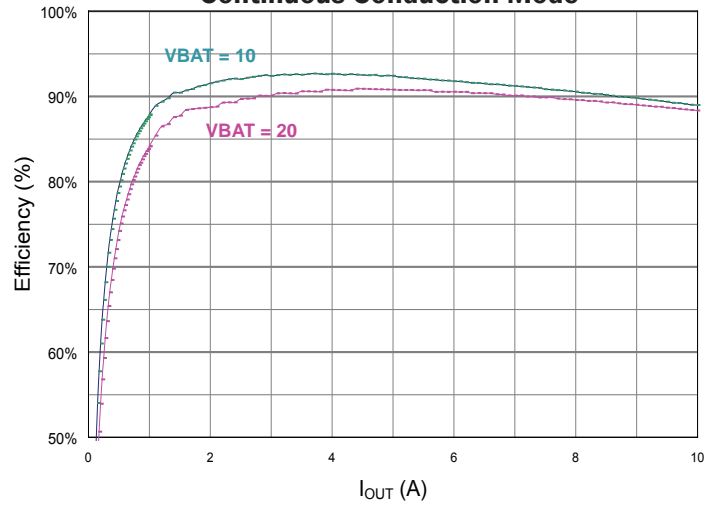
Figure 7 - Reference Design

Typical Characteristics

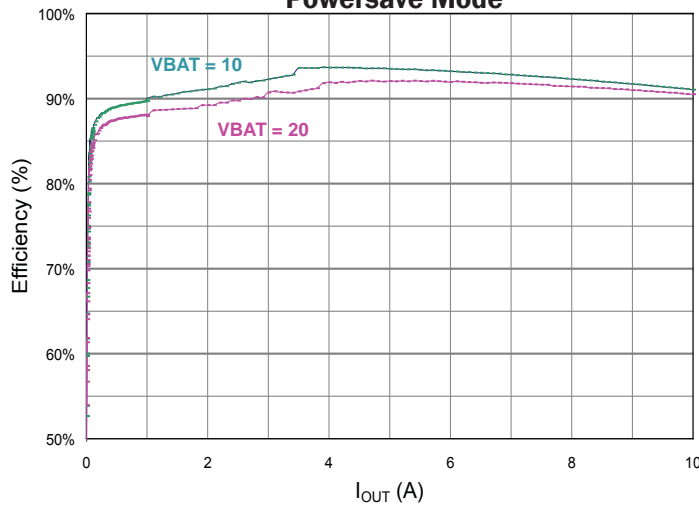
**1.8V Efficiency vs. Output Current
Powersave Mode**



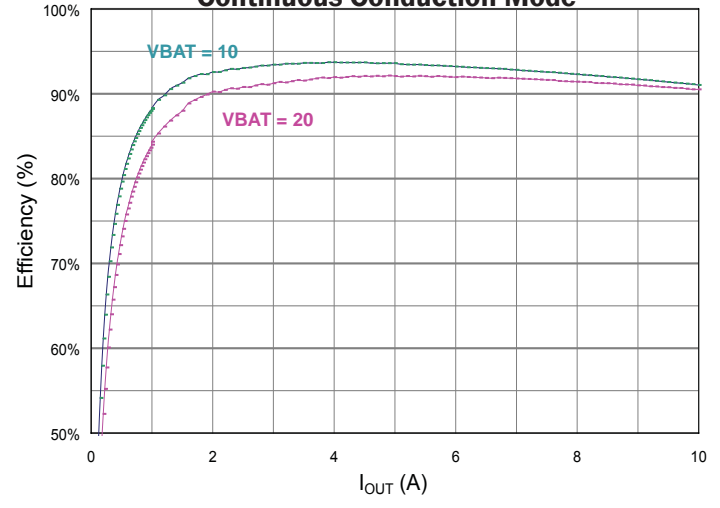
**1.8V Efficiency vs. Output Current
Continuous Conduction Mode**



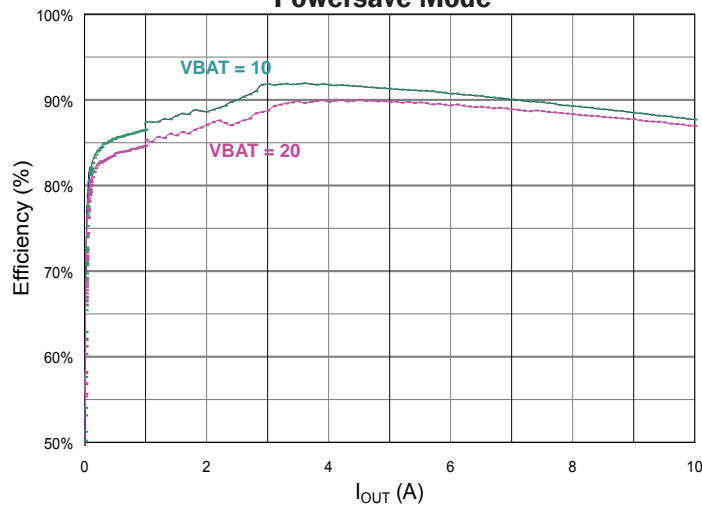
**2.5V Efficiency vs. Output Current
Powersave Mode**



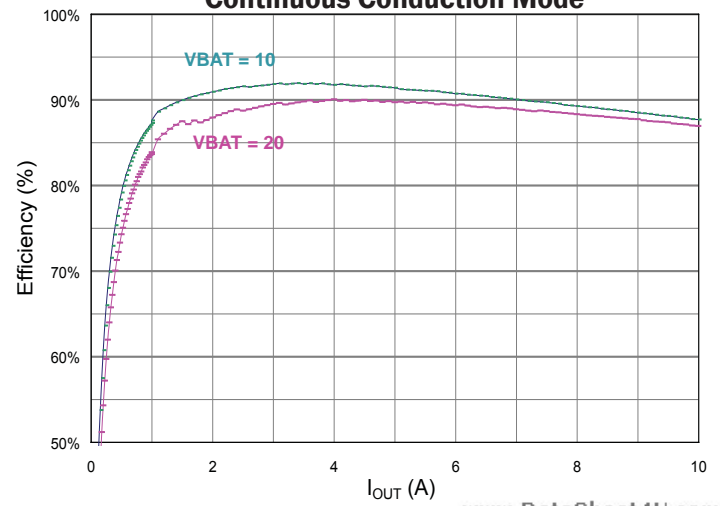
**2.5V Efficiency vs. Output Current
Continuous Conduction Mode**



**1.5V Efficiency vs. Output Current
Powersave Mode**

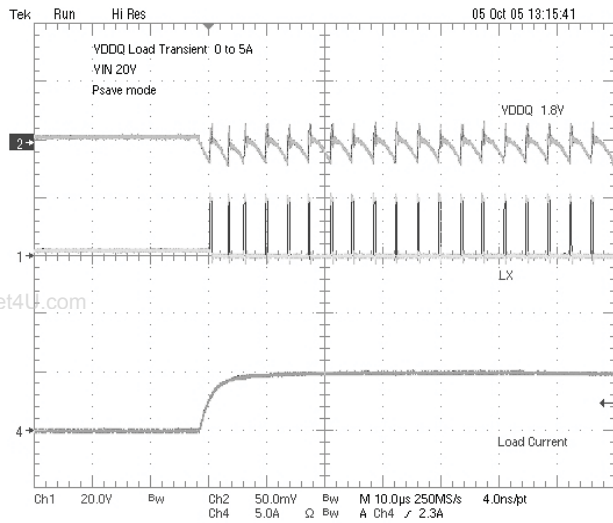


**1.5V Efficiency vs. Output Current
Continuous Conduction Mode**

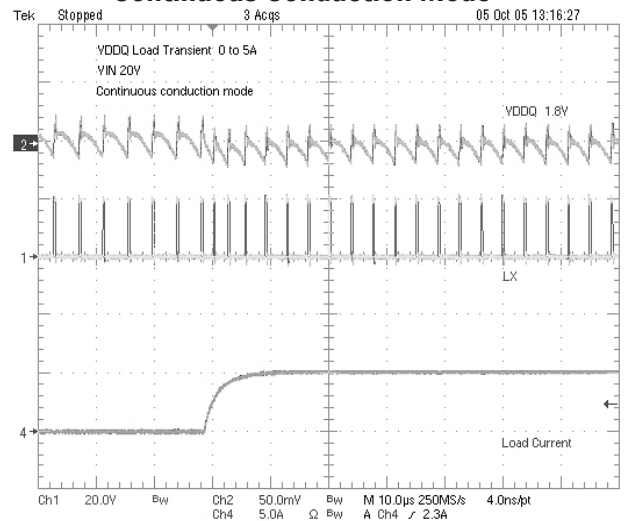


Typical Characteristics (Cont.)

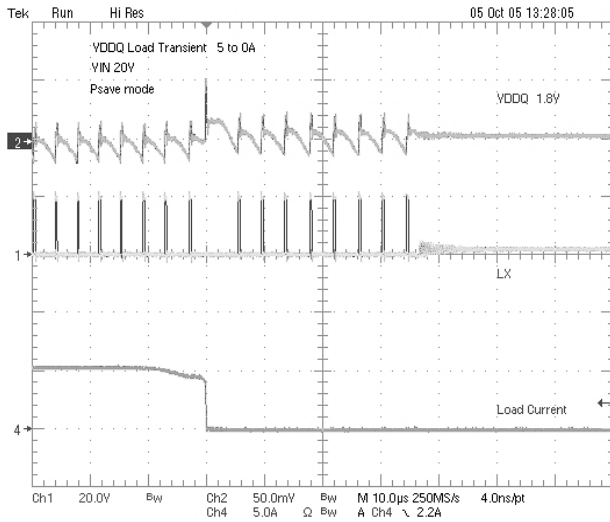
Load Transient Response, 0 to 5A, Psave Mode



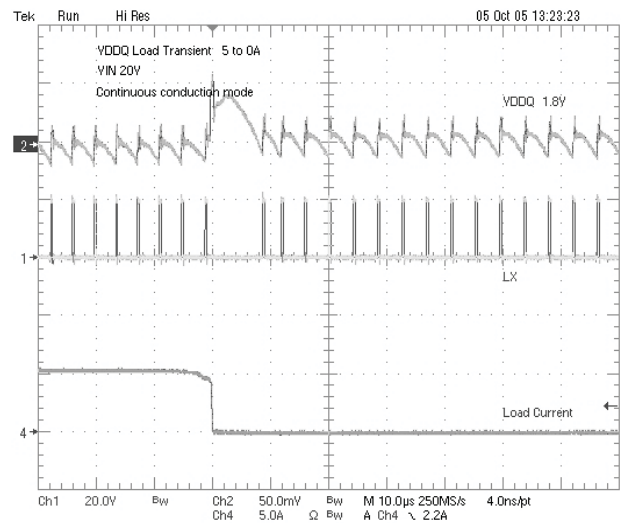
Load Transient Response, 0 to 5A, Continuous Conduction Mode



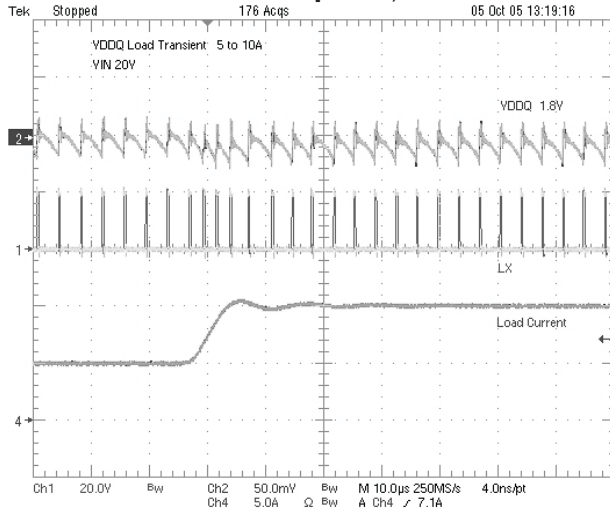
Load Transient Response, 5 to 0A, Psave Mode



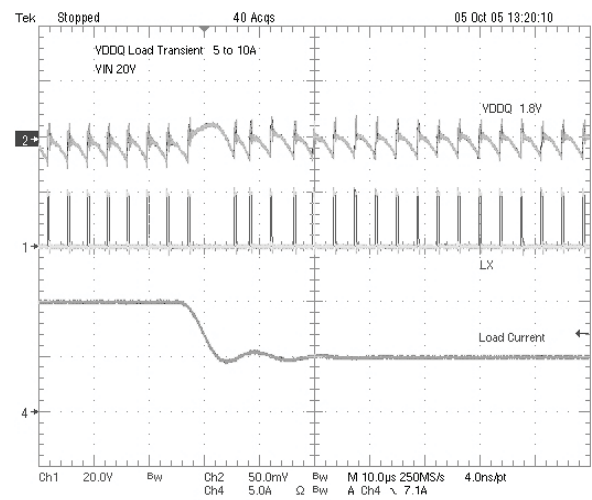
Load Transient Response, 5 to 0A, Continuous Conduction Mode



Load Transient Response, 5 to 10A

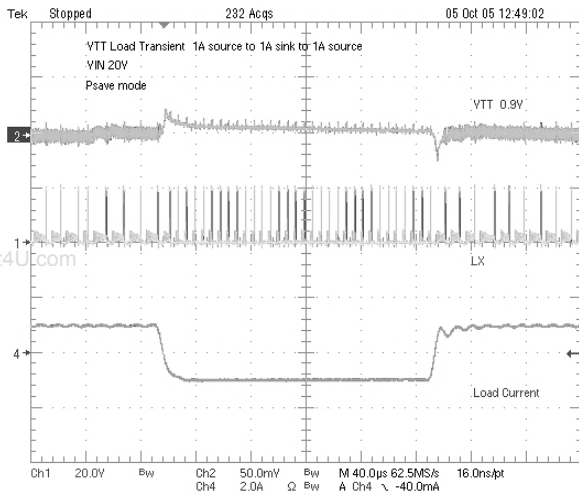


Load Transient Response, 10 to 5A

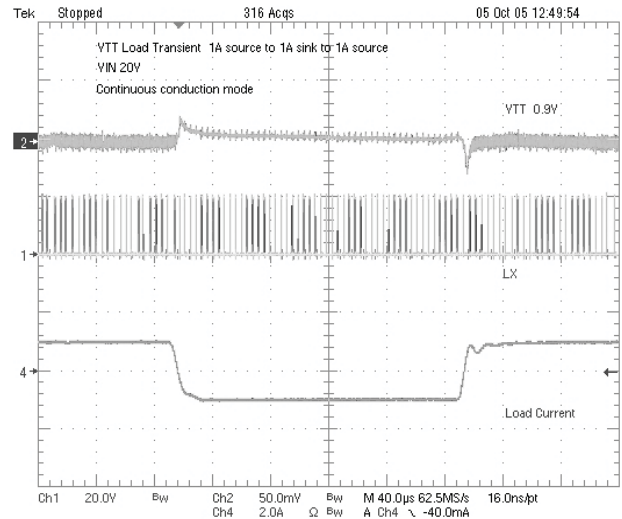


Typical Characteristics (Cont.)

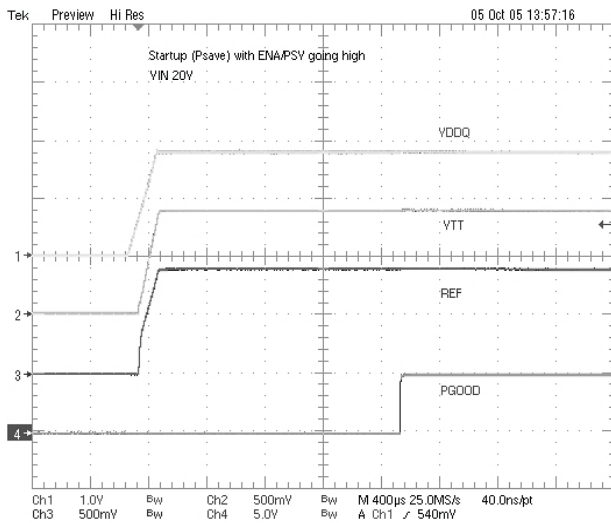
VTT Load Transient Response, 1A Sink/Source, Psave Mode



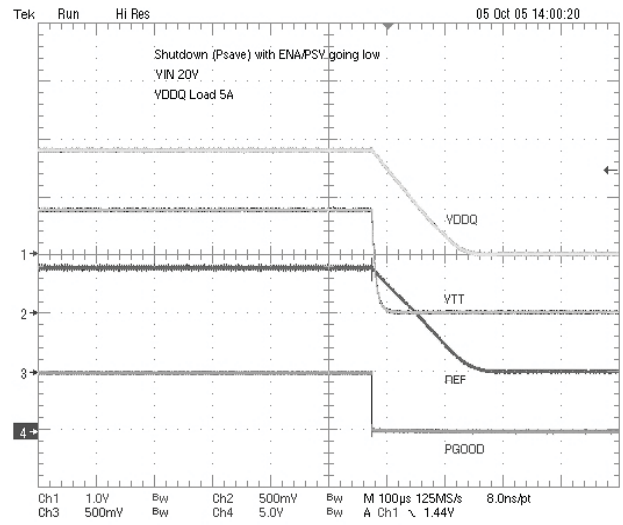
VTT Load Transient Response, 1A Sink/Source, Continuous Conduction Mode



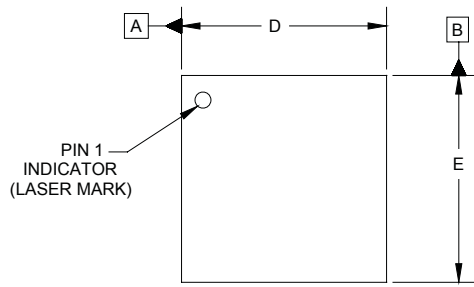
Startup (PSV), EN/PSV Going High



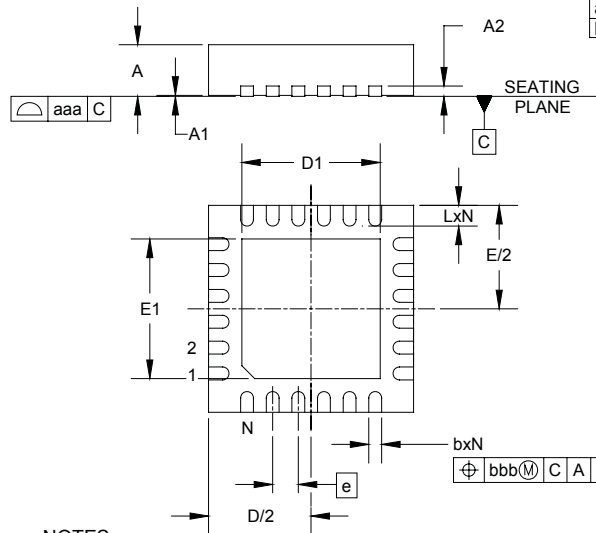
Startup (PSV), EN/PSV Going Low, VDDQ = 5A



Outline Drawing - MLPQ 24 (4x4mm)



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.040	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.151	.157	.163	3.85	4.00	4.15
D1	.100	.106	.110	2.55	2.70	2.80
E	.151	.157	.163	3.85	4.00	4.15
E1	.100	.106	.110	2.55	2.70	2.80
e	.020 BSC			0.50 BSC		
L	.011	.016	.020	0.30	0.40	0.50
N	24			24		
aaa	.004			0.10		
bbb	.004			0.10		



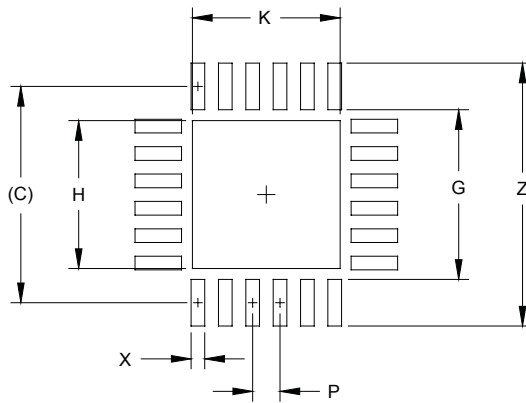
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

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POWER MANAGEMENT

Land Pattern - MLPQ 24 (4x4mm)



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.155)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.021	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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