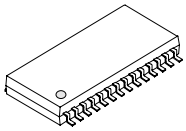
REMOTE CONTROL WITH BUILT-IN FLASH AND CODE SAMPLING FUNCTION

DESCRIPTIONS

SC51D01Fxx series is mainly used in remote controls with learning function. It is based on Silan's S51 8-bit MCU compliance with standard MCS-51 instructions and has built-in large FLASH program memory, infrared signal amplifier, and code sampling/transmitting modules. Under the support of few periphery components, these ICs can be easily used to make a remote control with on-chip self-learning function, which will enable one remote control to control all the devices related to TV sets.



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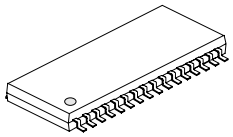

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FEATURES

* Compliance with standard MCS-51 instructions.
* Built-in 16K/32K/64K bytes FLASH program memory(can also used as data memory).
* Built-in 4K bytes XRAM.
* Integrate infrared signal amplifier.
* Integrate code sampling circuit which support code sampling with carrier, and has 256 bytes receive buffer.
* Integrate code transmitting circuit whose carrier frequency and duty can be set flexibly and has 32 bytes send buffer.
* 8 keyboard input pins.
* Support in system program (ISP).
* Adopt CMOS technology, operating voltage is 2.2V-3.6V, and quiescent current is less than 1μA.

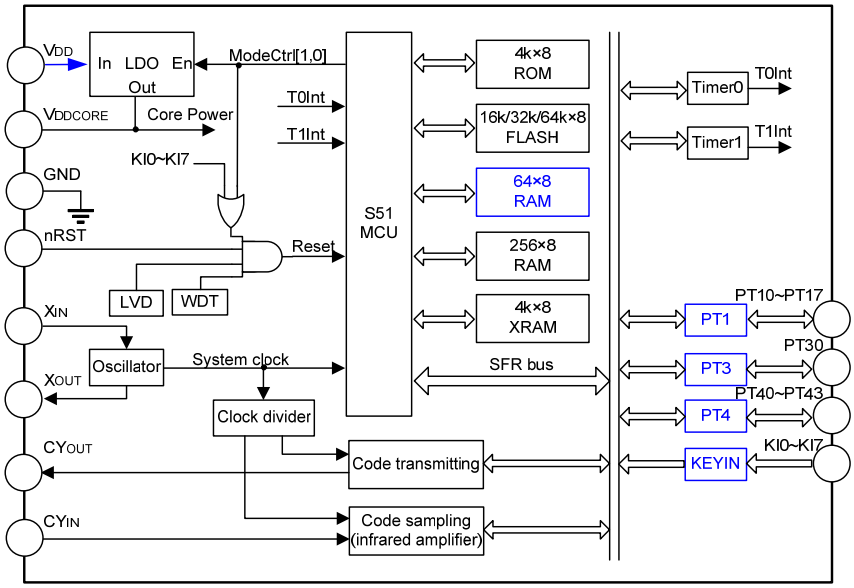
APPLICATIONS

* Remote control with learning function
* Preset universal remote control

ORDERING INFORMATION

Device	General I/O ports	On-chip FLASH （Bytes）	Package
SC51D01F16A	10	16K	SOP28-375-1.27
SC51D01F32A	10	32K	SOP28-375-1.27
SC51D01F64A	10	64K	SOP28-375-1.27
SC51D01F16B	13	16K	SOP32-375-1.27
SC51D01F32B	13	32K	SOP32-375-1.27
SC51D01F64B	13	64K	SOP32-375-1.27

BLOCK DIAGRAM



Note: The blue mark in the diagram is powered directly by VDD.

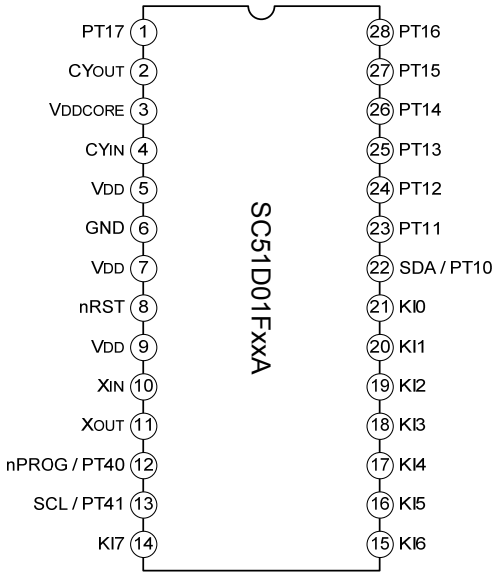
ABSOLUTE MAXIMUM RATING

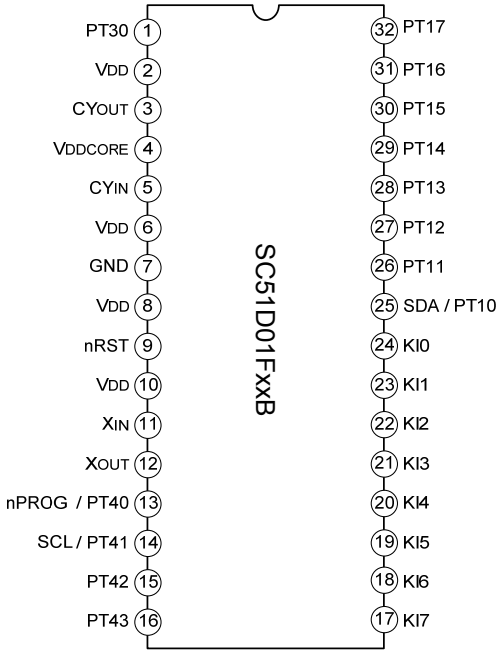
Characteristics	Symbol	Ratings	Unit
Power Supply	VDD	-0.3 ~ +4.0	V
Port Tolerance Voltage	VIN	-0.3 ~ VDD+0.3	V
Storage Temperature	TSTG	-65 ~ +150	°C
Operating Temperature	TOPR	-40 ~ +85	°C

ELECTRICAL CHARACTERISTICS(Unless otherwise specified,VDD=3V,Tamb=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	--	2.2	--	3.6	V
Operating Current	IDD	VDD=3V;No load code transmitting	--	12	--	mA
Quiescent Current	Iq	Core power is off	--	--	1	μA
Operating Clock	fosc	VDD=3V	12	12	12	MHz
High Input Voltage	VIH	--	0.7VDD	--	VDD	V
Low Input Voltage	VIL	--	0	--	0.3VDD	V
High Output Voltage	VOH	No load	0.9VDD	--	--	V
Low Output Voltage	VOL	No load	--	--	0.1VDD	V
High Output Current	IOH	VDD=3V;VOH=2.7V	--	3	--	mA
Low Output Current	IOL	VDD=3V;VOL=0.3V	--	4	--	mA
Port Pull-Up Resistor	Rpu	--	--	50	--	kΩ
FLASH Erase/Write Life	--	--	20K	100K	--	Time

PIN CONFIGURATION





PIN DESCRIPTIONS

Pin Name	Pin No.		I/O	Function Descriptions
	SC51D01FxxA	SC51D01FxxB		
VDD	5,7,9	2,6,8,10	PWR	Power supply.
VDDCORE	3	4	PWR	Core power output(Connect 1~10μF capacitor to the ground).
GND	6	7	PWR	Ground.
XIN	10	11	I	External oscillator input (Connect 1MΩ resistor between XIN and XOUT).
XOUT	11	12	O	External oscillator output.
nRST	8	9	I	External reset pin (low active).
CYOUT	2	3	O	Infrared signal control output.
CYIN	4	5	I	Infrared signal input.
KI0~KI7	21~14	24~17	I	Keyboard input.
SDA / PT10	22	25	I/O	I/O pin (also used as FLASH program data port).
PT11~PT17	23~28,1	26~32	I/O	I/O pin.
PT30	-	1	I/O	I/O pin.
nPROG / PT40	12	13	I/O	I/O pin(also used as FLASH program ‘enable’ singal, low active).
SCL / PT41	13	14	I/O	I/O pin(also used as FLASH program ‘clock’ signal input).
PT42~PT43	-	15~16	I/O	I/O pin.

FUNCTION DESCRIPTIONS

Summary Table Of Registers

Name	Description	Bit accessable	Read/write permission	Reset value	Byte address
S51 MCU					
ACC	Accumulator	√	R/W	00H	E0H
B	B register	√	R/W	00H	F0H
PSW	Program status word	√	R/W	00H	D0H
SP	Stack pointer	×	R/W	07H	81H
DPH	High byte of data pointer	×	R/W	00H	83H
DPL	Low byte of data pointer	×	R/W	00H	82H
TCON	Timer control register	√	R/W	00H	88H
IE	Interrupt enable control register	√	R/W	00H	A8H
IP	Interrupt PRI control register	√	R/W	00H	B8H
AUXR1	DPTR selection register	×	W	00H	A2H
CS_IntDM_ CTRL	Internal extended RAM selection control register	×	W	96H	9EH
ModeCtrl	Working mode control register	×	W	03H	94H
Low voltage detecting					
LVDCtrl	Low voltage detect control/status register	×	R/W	XXX10001B	97H
Watchdog timer					
Wdt_Ctrl	WDT prescaler setting register	×	R/W	XXXXXX00B	F3H
Wdt_Clr0	Watchdog clear register 0	×	W	--	F4H
Wdt_Clr1	Watchdog clear register1	×	W	--	F5H
Keybord input ports					
KEYIN	Keyboard input register	×	R	--	F7H
General purpose I/O					
PT1Reg	PT1 register	×	R/W	FFH	F8H
Name	Description	Bit accessable	Read/write permission	Reset value	Byte address
PT1Ctrl	PT1 output mode control register	×	R/W	00H	F9H
PT1PUCtrl	PT1 internal weak pull-up control register	×	R/W	00H	FAH
PT1ODCtrl	PT1 open-drain output register	×	R/W	FFH	FBH
PT3Reg	PT3 register	×	R/W	FFH	E1H
PT3Ctrl	PT3 output mode control register	×	R/W	00H	E2H
PT3PUCtrl	PT3 internal weak pull-up control register	×	R/W	00H	E3H

(To be continued)

(Continued)

Name	Description	Bit accessable	Read/write permission	Reset value	Byte address
PT3ODCtrl	PT3 open-drain ouitput register	×	R/W	FFH	E4H
PT4Reg	PT4 register	×	R/W	FFH	E5H
PT4Ctrl	PT4 output mode control register	×	R/W	00H	E6H
PT4PUCtrl	PT4 internal weak pull-up control register	×	R/W	00H	E7H
PT4ODCtrl	PT4 open-drain output register	×	R/W	FFH	E8H
Timer					
TH0	High byte of timer 0	×	R/W	00H	8CH
TL0	Low byte of timer 0	×	R/W	00H	8AH
TH1	High byte of timer 1	×	R/W	00H	8DH
TL1	Low byte of timer 1	×	R/W	00H	8BH
TIMER_PRESCALER	Timer prescaler control register	×	R/W	X111X111B	8EH
TMOD	Timer working mode control register	×	R/W	00H	89H
Code sampling module					
CARCount	Carrier period register	×	R	00H	C1H

ADDRESS SPACE ASSIGNMENT

Internal Data Space

Fig. 1 shows that the internal data space of SC51D01Fxx series is divided into direct addressing space and indirect addressing space.

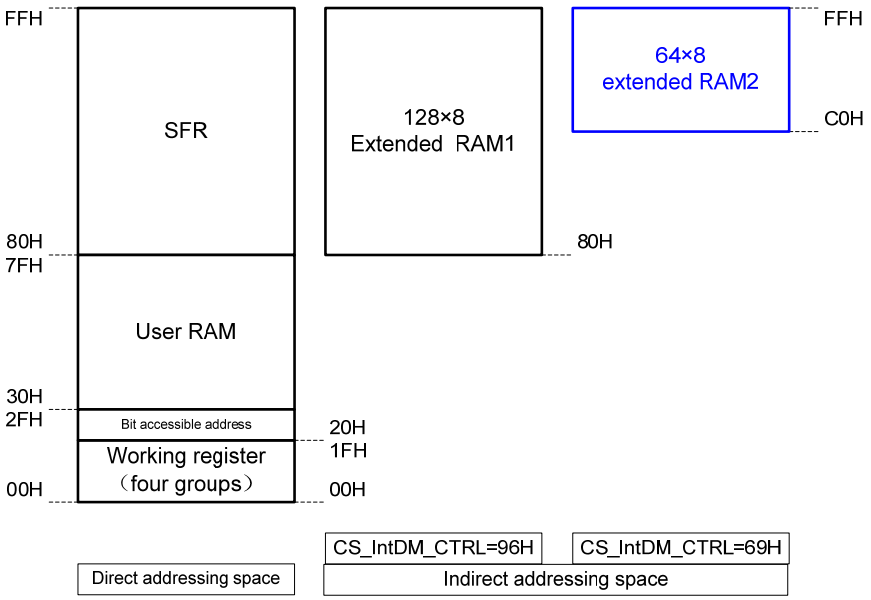


Fig. 1 – Internal data space assignment

Direct addressing space includes 128 bytes RAM and special function register area (SFR). 00H~1FH of direct addressing 128 bytes RAM are working register area(including four groups of working registers),20H~2FH are bit addressing area(Corresponding address range is 00H~7FH),The 30H~7FH are user RAM area, the details refer to Fig. 2.

The address range of SFR is 80H~FFH, including the special function registers of MCU and peripheral equipment.

Indirect addressing space includes two extended RAM: the extended RAM1 is 128 bytes, and the address range is 80H~FFH; the extended RAM2 is 64 bytes, and the address range is C0H~FFH. Access only one extended RAM at the same time: set the value of special function register CS_IntDM_CTRL as 96H, then it can access extended RAM1; Set CS_IntDM_CTRL as 69H, then it can access extended RAM2.

The difference between two extended RAM is different power supply. Extended RAM1 and S51 core share the same power supply, when enter the standby mode, the core power is off, so the data in extended RAM1 can not be held. The extended RAM2 is powered directly by V_{DD}, so the data can be reserved in standby mode.

Attention should be paid that, because two extended RAM share the address space of C0H~FFH, the stack is better to set within 08H~BFH.

Byte address \ Bit		Bit address							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
User RAM	7FH … 30H	(Only byte addressing, can used as stack and data buffer)							
Bit addressing space	2FH	7FH	7EH	7DH	7CH	7BH	7AH	79H	78H
	2EH	77H	76H	75H	74H	73H	72H	71H	70H
	2DH	6FH	6EH	6DH	6CH	6BH	6AH	69H	68H
	2CH	67H	66H	65H	64H	63H	62H	61H	60H
	2BH	5FH	5EH	5DH	5CH	5BH	5AH	59H	58H
	2AH	57H	56H	55H	54H	53H	52H	51H	50H
	29H	4FH	4EH	4DH	4CH	4BH	4AH	49H	48H
	28H	47H	46H	45H	44H	43H	42H	41H	40H
	27H	3FH	3EH	3DH	3CH	3BH	3AH	39H	38H
	26H	37H	36H	35H	34H	33H	32H	31H	30H
	25H	2FH	2EH	2DH	2CH	2BH	2AH	29H	28H
	24H	27H	26H	25H	24H	23H	22H	21H	20H
	23H	1FH	1EH	1DH	1CH	1BH	1AH	19H	18H
	22H	17H	16H	15H	14H	13H	12H	11H	10H
	21H	0FH	0EH	0DH	0CH	0BH	0AH	09H	08H
	20H	07H	06H	05H	04H	03H	02H	01H	00H
General registers	1FH … 18H	R7 of the third group working register … R0 of the third group working register							
	17H … 10H	R7 of the second group working register … R0 of the second group working register							
	0FH … 08H	R7 of the first group working register … R0 of the first group working register							
	07H … 00H	R7 of the zero group working register … R0 of the zero group working register							

Fig. 2 –128 bytes RAM of direct addressing

Program and External Data Space

SC51D01Fxx series support maximum 64K bytes program and external data space. The program memory and external data memory of SC51D01Fxx series are all embedded without extended. The space assignment refers to Fig. 3.

Program memory includes 4K bytes ROM(address range: 0000H~0FFFH) and maximum 60K bytes FLASH(address range: 1000H~FFFFH). By calling the system function in ROM, FLASH can be erased/written.

External data space includes 4K bytes XRAM. Special attention should be pait that: 0100H~01EDH of XRAM has been occupied by the system, and can not be changed by user; 0D00H~0DFFH is receiving buffer of code sampling module(Code sampling buffer for short).

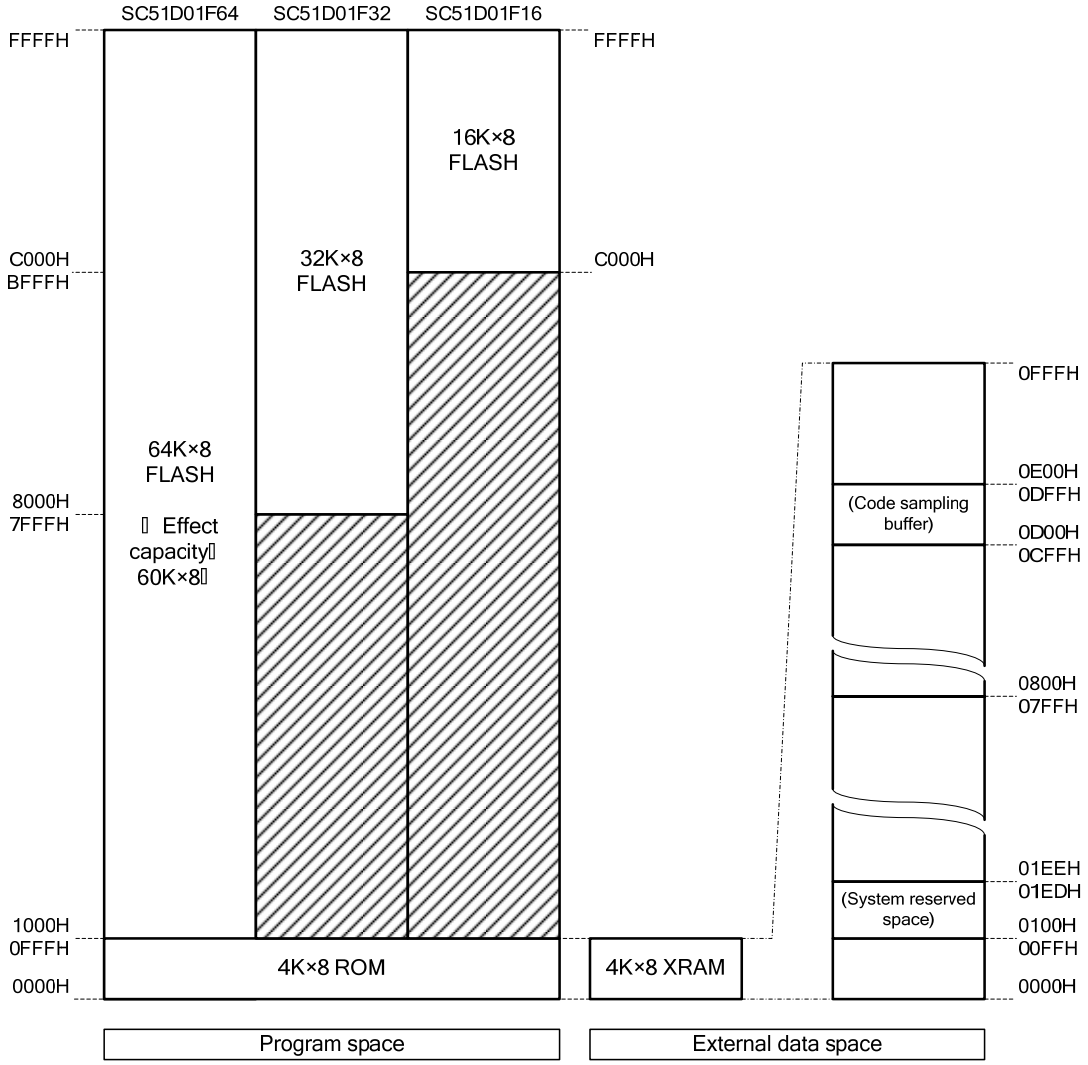


Fig. 3 – Program and external data space

S51 MCU

SC51D01Fxx series use S51 MCU compatible with MCS-51 instructions. Users can develop the software using standard 805x assembler and compiler.

The difference between S51 MCU and standard 8051 lies in:

- S51 MCU supports dual DPTR.
- In the condition of the same external oscillator frequency, the instruction period of S51 MCU is shorter than that of 8051.
- S51 MCU supports two extended RAM.
- S51 MCU's MOVX A,@Ri and MOVX @Ri, A commands can only access 00H~FFH of on-chip XRAM.
- S51 MCU only supports 2 interrupt sources: the overflow interrupt of timer 0 and timer 1. The interrupt vector is different from that of standard 8051.
- S51 MCU only supports 2 working modes: normal working and standby modes. The working mode control is also different from that of standard 8051.

RESET

SC51D01Fxx series has external reset, keying reset, power down reset and watchdog reset 4 reset sources. Where, the external reset, keying reset and power down reset can make the chip awake from standby mode.

External rset

External reset is adding a no less than 10ms low level on pin nRST to make MCU reset.

Connect tandem resistor and capacitor to pin nRST to implement the power on reset of MCU, shown in Fig. 4:

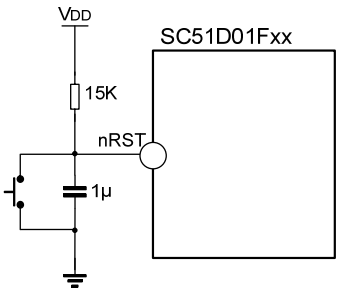


Fig. 4 – External reset and power on reset circuit

Keying reset

Keying reset means that when MCU is in standby mode, apply effective time of low level to any one or more keyboard input ports among KI0~KI7 to make MCU reset. This is often used to awake the MCU by keying.

In normal working mode, applying low level to KI0~KI7 will not make the MCU reset.

Power down reset

When power down or V_{DD} is dropped to less than 1.85V caused by power fluctuation, the low voltage detector (LVD) will generate a reset signal to make MCU reset.If V_{DD} returns to more than 1.95V, MCU will exit the reset state, and enter normal working state.

Watchdog reset

The watchdog reset make MCU reset when the internal 20-bit counter (watchdog timer WDT) overflows. The

program should always clear the WDT to avoid that WDT overflows. When the program enters dead loop, maybe WDT is not clear in time. WDT will overflow to make MCU reset to avoid the system is in abnormal state for a long time.

OSCILLATION CIRCUIT

SC51D01Fxx series contain an inverting amplifier with high gain. The amplifier's input is XIN, output is XOUT. A quartz crystal, a feedback resistor, and two capacitors are connected between XIN and XOUT to form a stable self-oscillator, shown in Fig. 5. The waveform generated by the oscillation circuit produced the system clock MClk which provides clock to S51 MCU and some periphery modules after it is shaped by the inverter.

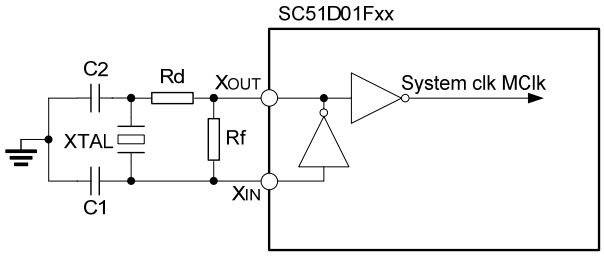


Fig. 5 – Oscillation circuit

Where:

- Rf is the feedback resistor, 1MΩ.
- Rd is the dirve resistor , 300~600Ω
- C1 and C2 are load capacitors, capacitance is the same and the range is 10pF~30pF.
- XTAL is crystal oscillator, and the fixed frequency is 12MHz.

PERIPHERY MODULES

Keyboard Input Ports

[Brief]

SC51D01Fxx series has 8 input ports KI0~KI7 used to connect with the keyboard. Every port has pull-up resistor and Schmitt trigger.

[Structure Diagram]

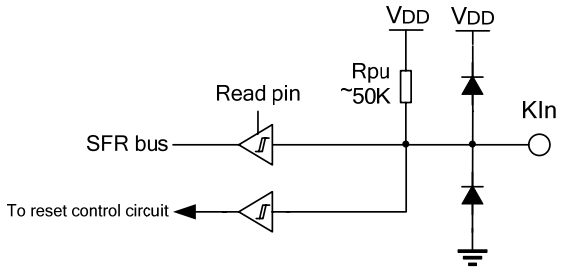


Figure 6 – Keyboard input structure

[Function Description]

In standby mode, low level applied to any keyboard input port will make the chip reset and enter the normal working mode; however, in normal working mode, input low level will not reset the chip.

General Purpose I/O Ports

[Brief]

SC51D01FxxA has PT1 and PT4 two groups of 10 general purpose I/O ports (GPIO); SC51D01FxxB has PT1, PT3 and PT4 three groups of 14 GPIO. The structure and the manipulation of SC51D01Fxx series' GPIO are different from those of standard 8051.

[Structure Diagram]

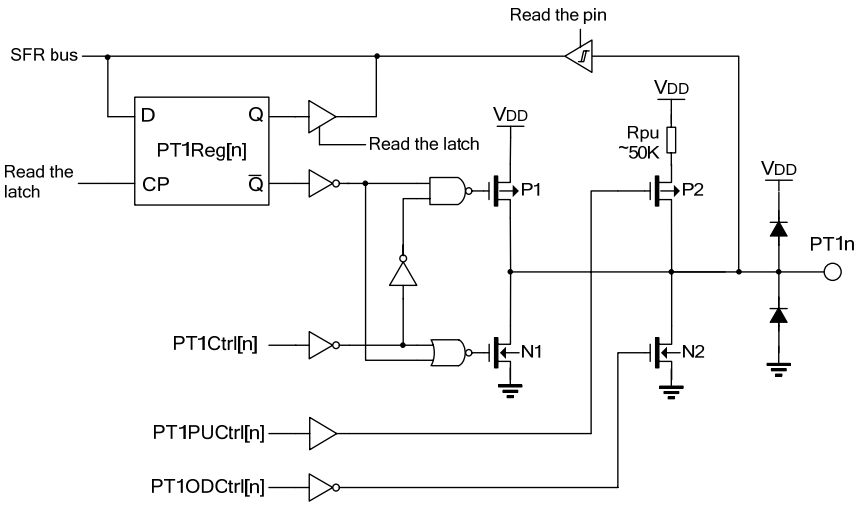


Fig. 7– PT1 structure

Note: The structure of PT3 and PT4 is the same as that of PT1.

[Function Description]

Related with Fig. , the following takes PT1 for example to introduce the function of general purpose I/O ports. The function of PT3 and PT4 is the same as that of PT1.

Configure the output mode of GPIO pins

The output mode of every GPIO pin can be configured as open-drain or pull-push mode, default is open-drain. When PT1Ctrl[n]=0, no matter PT1Reg[n] output 1 or 0,P1 and N1 misfits are both off, and the output mode corresponding to PT1n pin is open-drain; when PT1Ctrl[n]=1, the off/on of P1 and N1 is decided by the output status of PT1Reg[n], and the output mode corresponding to PT1n pin is pull-push.

In pull-push mode, PT1Reg[n]=0 will turn P1 off, N1 on, and PT1n pin will connect to GND; PT1Reg[n]=1 will turn P1 on, N1 off, and PT1n pin will connect to V_{DD}.

In open-drain mode, PTODCtrl[n]=0 of open-drain output register will turn N2 on, PT1n pin will connect to GND;PTODCtrl[n]=1 will turn N2 off, PT1n pin is in high impedance. When the application system needs many output ports connected to one physical wire (e.g. the scanning output wire of keyboard), those ports must be in open-drain mode! In open-drain mode, the port needs to connect pull-up resistor to V_{DD} or using internal pull-up resistor(PT1PUCtrl[n]=0,P2 is on, PT1n is pulled-up to V_{DD} via Rpu).

Configure GPIO pin as input ports

Set the port output mode to open-drain mode(P1 and N1 are both off), and write 1 to the corresponding bits of open-drain output register PT1ODCtrl to make N2 off, after that this port is configured as input port. For example, set PT1Ctrl[7] =0, PT1ODCtrl[7] =1 to configure PT17 as input port.

Configrue ports' weak pull-up

Every GPIO pin of SC51D01Fxx series has an internal weak pull-up(about 50 kΩ). Set PT1PUCtrl[n]=1 to make P2 off, and the weak pull-up is disabled; set PT1PUCtrl[n]=0 to make P2 on, and the weak pull-up is enable.

Timer

[Brief]

SC51D01Fxx contains two timers(timer 0 and timer 1),which only have timing function but not external counting function. Its timing function is compatible with standard 8051, the difference is that the timer of SC51D01Fxx should be turned off when loading the initial value every time, open the timer after that. Timer 0 and timer 1 are almost the same, which both have four working modes(where, timer 1 cannot work in mode 3).

[Function Description]

Timer 0 and timer 1 are both 16-bit registers, presented in two bytes when they are accessed. The low byte of timer 0 is TL0, the high byte is TH0;the low byte of timer 1 is TL1, the high byte is TH1. Timer 0 and timer 1 have independent clock sources which are derived from the frequency dividing of the system clock by setting timer clock prescaler control register TIMER_PRESCALER. Timer control register TCON is used to enable timer 0 and timer 1 and show their status. Set ET0 of the IE register to enable the timer 0 interrupt, and set ET1 to enable the timer 1 interrupt. You can select the two timers' working mode by setting the mode selection bits T0M1 and T0M0(or T1M1 and T1M0) of TMOD register, each bit can be configured independently. Next we will take timer 0 for example to introduce these four working modes.

FLASH Memory

[Brief]

SC51D01Fxx series has 16/32/64K bytes FLASH memory used to store the program code and non-volatile data. You can manipulate the erase/write operation to FLASH memory by system function, one byte or one block (512 bytes) each time. Once write '0' to a FLASH bit, it returns '1' until it is erased. In general, data bytes should be erased (set as FFH) before reprogramming. The erase manipulation to FLASH of SC51D01Fxx series can only adopt block as unit, the mapping of each block is shown in Fig.8.

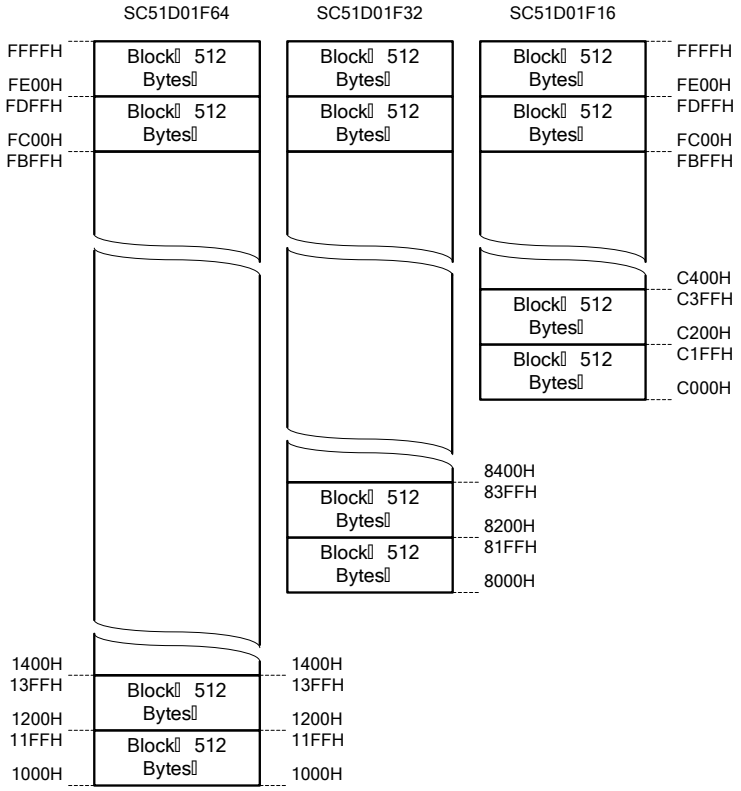


Fig. 8 – Mapping address of FLASH blocks

FLASH erase/write operation is manipulated by calling system function. The system function is pre-stored in the ROM of 0000H~0FFFH. In order to make sure the correct of FLASH's content, we recommend user to check 2.2V low voltage detecting flag LVDCtrl[2] before manipulate write or erase operation to FLASH. If LVDCtrl[2]=1, it means that V_{DD} is lower than 2.2V, you'd better not manipulate write or erase operation.

XRAM

SC51D01Fxx series integrates 4K bytes RAM as external data memory XRAM, the address space is 0000H~0FFFH.

XRAM can be accessed by external movement instructions "MOVX A, @DPTR"."MOVX @DPTR, A"."MOVX A, @Ri" and "MOVX @Ri, A" . If using the latter two instructions, only can access the address space 0000H~00FFH.

Special attention should be paid that: 0100H~01EDH of XRAM is occupied by the system, can not be changed by the system; 0D00H~0DFFH is receiving buffer of code sampling module(code sampling buffer for short).

Code Sampling Module

[Brief]

Code sampling module is used to collect the infrared signal from other remote control which can implement the self-learning function. When select inner infrared amplifier function, you only connect an infrared receiving diode and 1nF capacitor between CYIN pin and GND(refer to typical application circuit) to realize the sampling of the infrared signal.

[Structure Diagram]

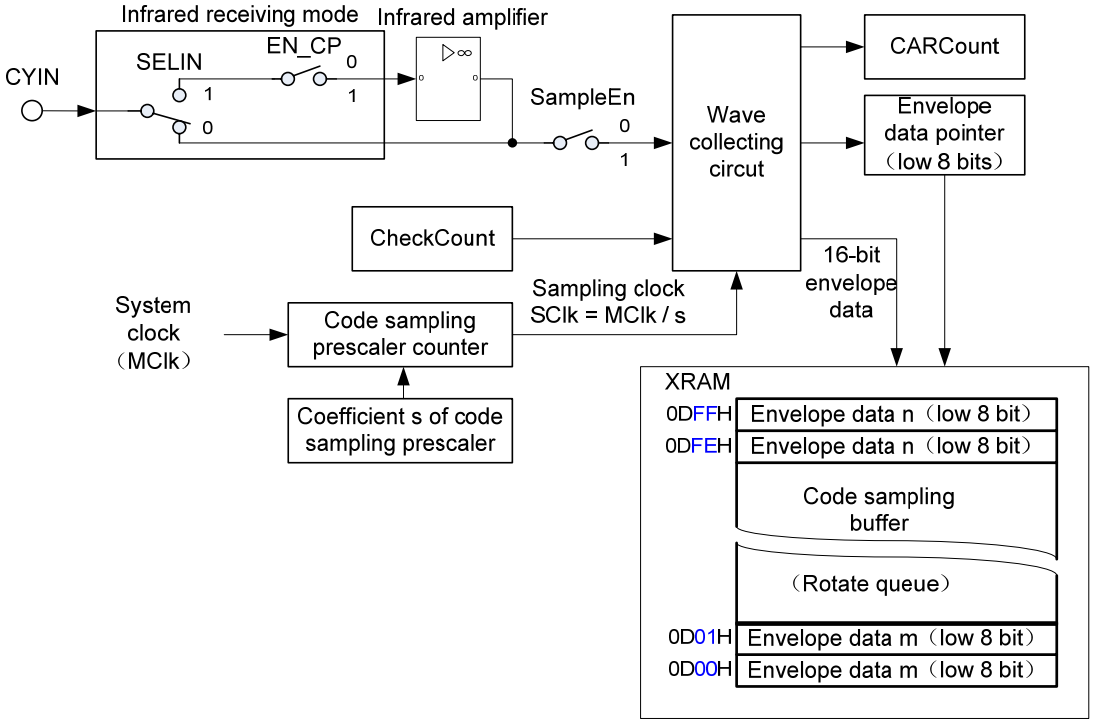


Fig. 9 – The structure diagram of code sampling module

[Function Description]

The code sampling module of SC51D01Fxx series can realize the code sampling with carrier. It can recognize if the received wave has the carrier by setting detecting register CheckCount, and the carrier information is stored in carrier period register CARCount(For the wave without carrier, the value of CARCount is 0). This module can also automatically save the envelope information filtered carrier in the code sampling buffer (0D00H~0DFFH of XRAM). The code sampling buffer is a 128 levels rotate queue and each level is two bytes (even address is the high 8-bit of the envelope data, odd address is the low 8-bit). The envelope data pointer points at the high byte of the lately sampled data. Add 2 to the pointer every time sampled an envelope data, when the pointer is 0DFEH, it will return to 0D00H after sampled a data again.

Wave sampling circuit includes a detecting counter (counting clock is the code sampling clock SClk). When the wave sampling circuit is enable, the detecting counter counts the time interval and low level width of adjoin two rising edges. As shown in Fig.10, T1 is the time interval between the first rising edge and the second rising edge, and T2 is the first low level width. If T2 is more than the detecting time, no carrier is considered, and CARCount=0; if T1 is less than the detecting time, carrier is considered, and CARCount=T3(T3 is the time interval between the third rising edge and the fourth rising edge).

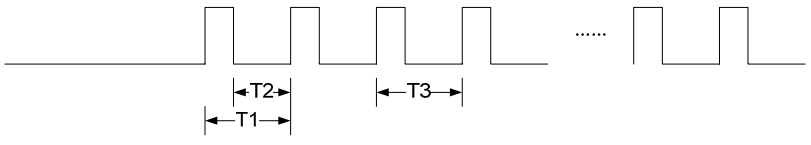


Fig. 10 – Detecting principle

Wave sampling circuit has one 15-bit envelope counter (counting clock is the code sampling clock SClk). When the wave sampling circuit is enable and detect the first rising edge, the envelope counter begins to count until the low level time is over the detecting time, then store the envelope type(the most significant bit of 16-bit envelope data, 1:high level; 0:low level) and counting value(low 15-bit of envelope data) in the code sampling buffer, after that, the envelope counter restarts to count. As shown in Fig.11(a), T4 is the envelope high level width stored in the buffer, T5 is the low level width stored in the buffer, T6 is the detecting time. That is, the data stored in the code sampling buffer needs to be compensated to be the real envelope level width. Of course, if T4 or T5 beyond the range of 15 binary bits, it will be divided into many segments to be stored in the buffer, as shown in Fig.11(b).

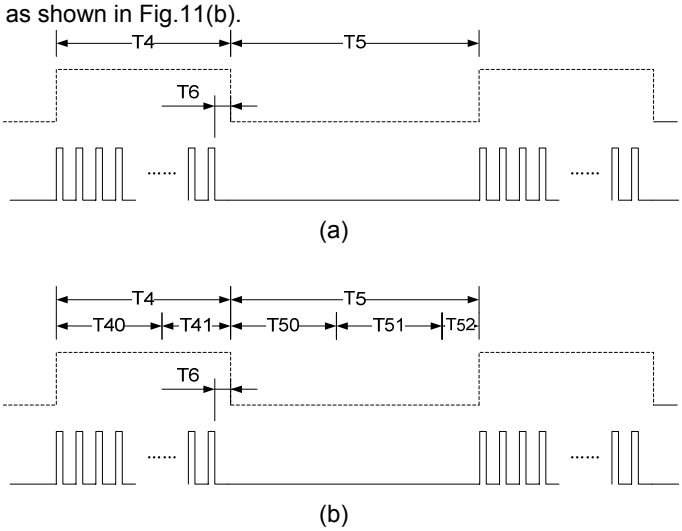


Fig. 11 – Envelope sampling principle

The compensation arithmetic of envelope high level width is: total width of successive high levels T4 – detecting time T6; the compensation arithmetic of envelope low level width is: total width of successive high levels T5 + detecting time T6.

Code Transmitting Module

[Brief]

The code transmitting module is used to generate the high and low levels which control the infrared diode. It contains carrier generator and 32 bytes code transmitting buffer, which can transmit the code accurately.

[Structure Diagram]

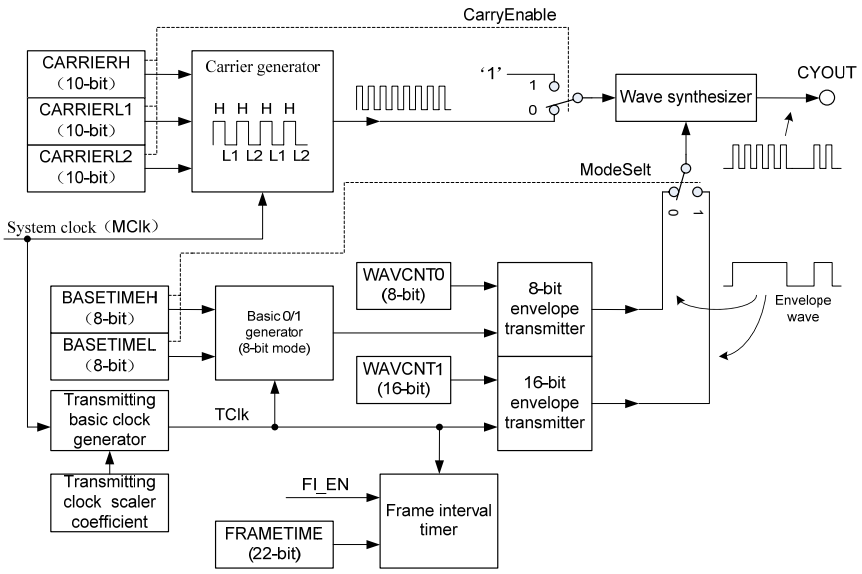


Fig. 12– The structure diagram of code transmitting module

[Function Description]

The transmitting module of SC51D01Fxx series defines an universal wave format (as shown in Fig.13), code transmitting should abide by this format.

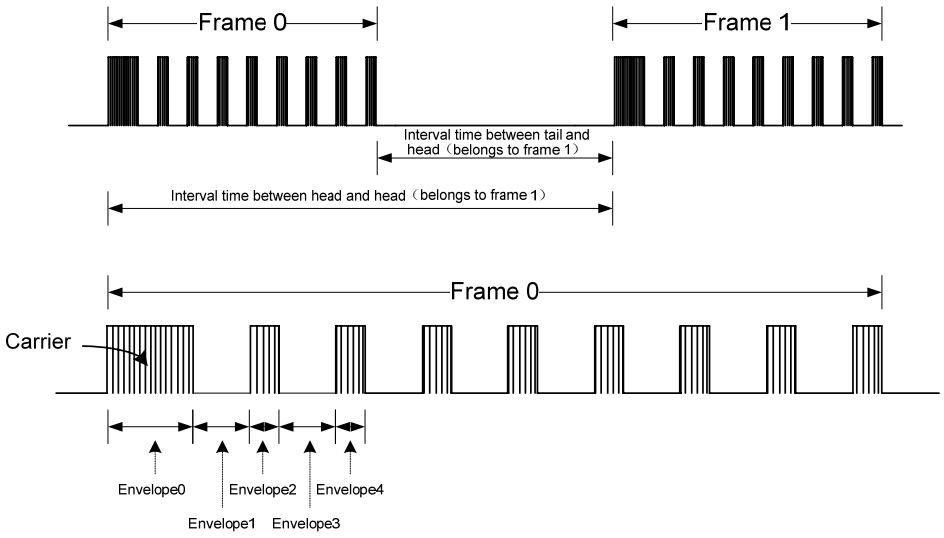


Fig. 13 – Code transmitting format

The counting clock of carrier generator comes from the system clock MClk, and generated carrier shown in Fig.14. Where, H, L1 and L2 are separately from the three characteristics CARRIERH, CARRIERL1 and CARRIERL2 set by the user. In general, L1 is only 1 MClk clock different from L2, thus the average period of carrier is more accurate.

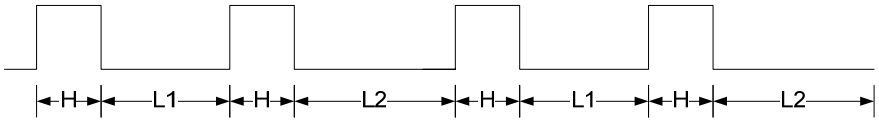


Fig. 14 – Carrier generator principle

The code transmitting of SC51D01Fxx series supports two modes: 8-bit mode, 16-bit mode.

The code transmitting principle of 8-bit mode is shown in Fig.15. The system clock MClk generated TClk (the period is T) via code transmitting reference clock generator. TClk produces high level Base unit (Base 1) time TH and low level Base unit (Base 0) time TL via Base 0/1 generator. TH and TL are decided by setting BASETIMEH and BASETIMEL, and unit T. TH is the Base unit time of high level envelope time, and TL is the Base unit time of low level envelope time.

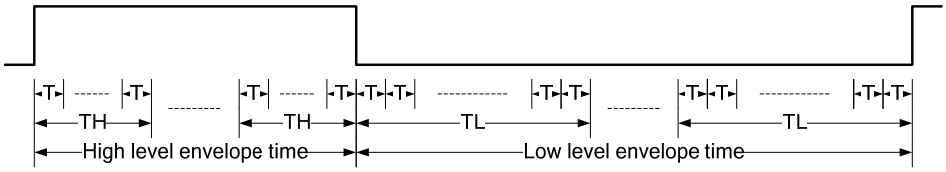


Fig. 15 – 8-bit code transmitting principle

16-bit code transmitting principle is shown in Fig.16. System clock MClk generates TClk (the period is T). T is the Base unit of high and low level envelope time.

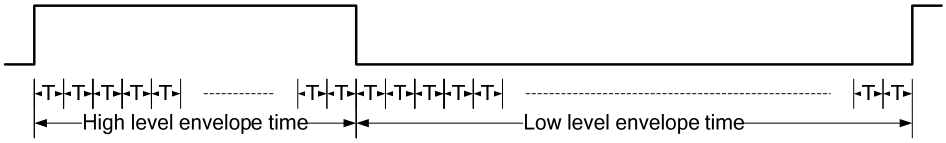


Fig. 16 – 16-bit code transmitting principle

FLASH PROGRAM INTERFACE

SC51D01Fxx series support in system program (ISP), but you should use Silan's special programmer. Usually the programmer connects with 6 pins, as shown in Table.

FLASH program interface

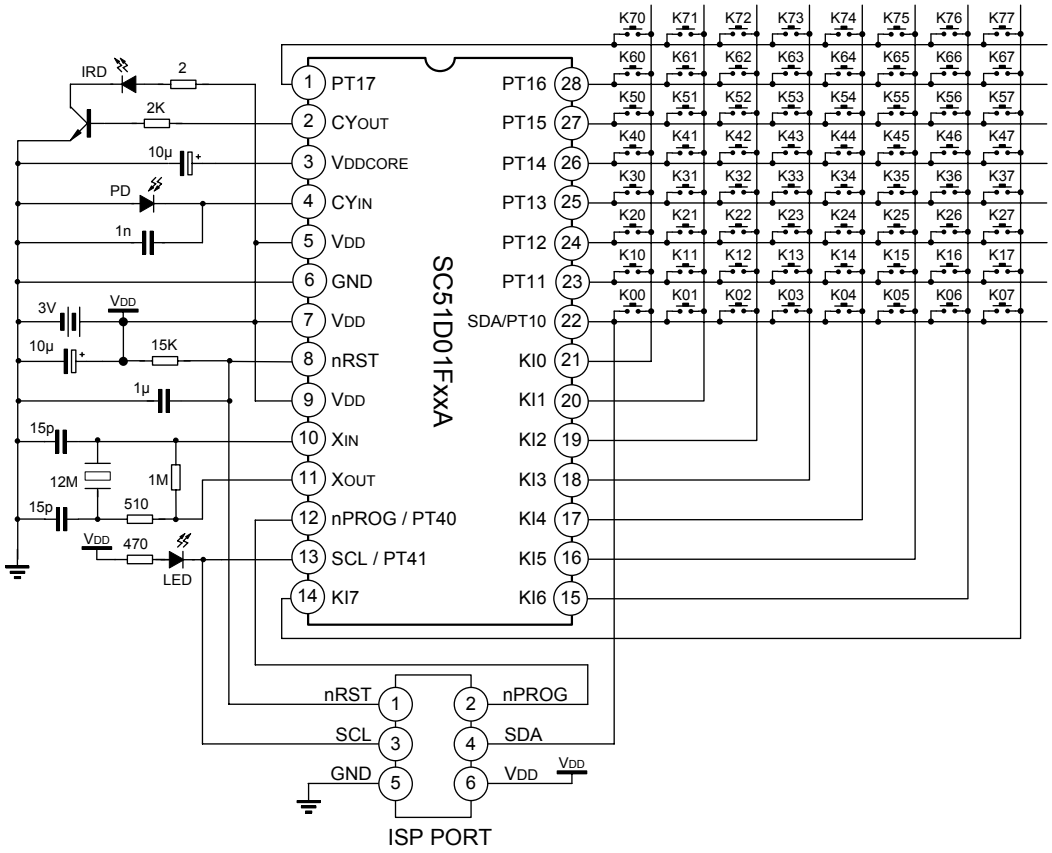
Name	Pin No.		Function
	SC51D01FxxA	SC51D01FxxB	
nRST	8	9	Chip reset signal
nPROG	12	13	Mode selection signal
SCL	13	14	Program clock signal
SDA	22	25	Program data signal
V_{DD}	5(7,9)	6(2,8,10)	Power supply
GND	6	7	Ground

nPROG is selection signal of the chip's boot mode.

When the chip is power on or reset , check nPROG pin first, if nPROG pin is low level, enter Flash program mode; if nPROG pin is high level, enter normal working mode.

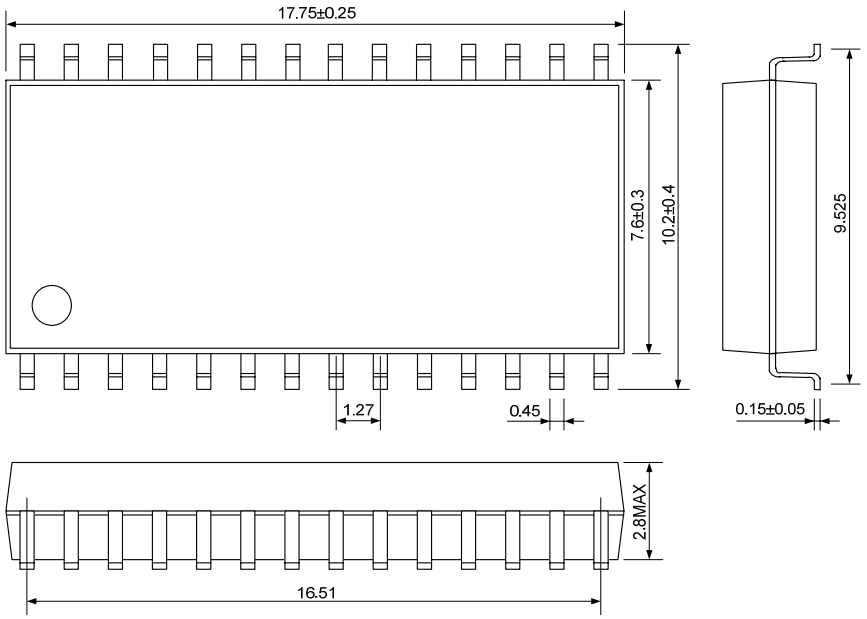
After enter Flash program mode or normal working mode, the nPROG pin's level is not considered.

TYPICAL APPLICATION CIRCUIT

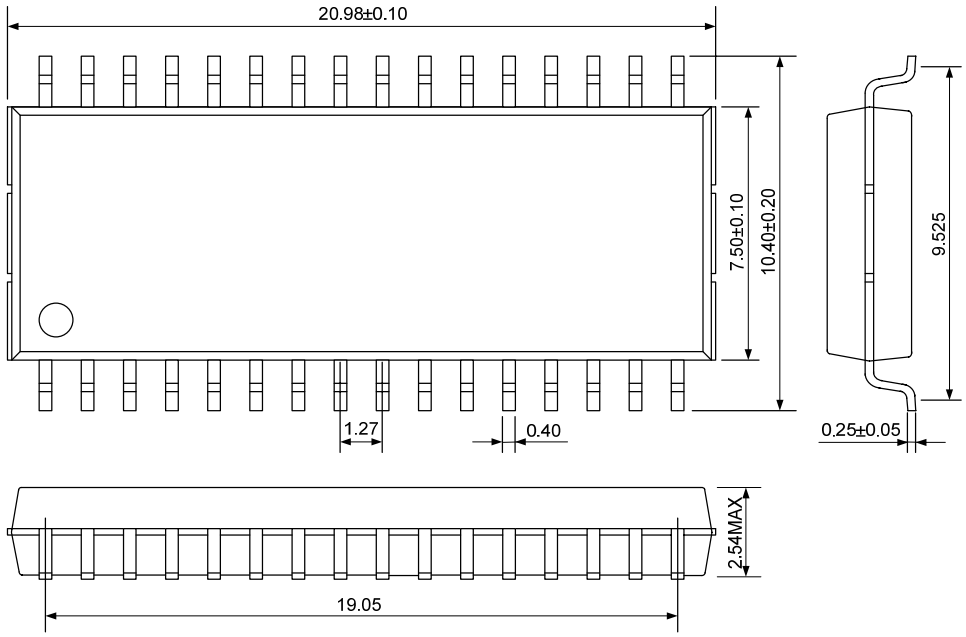


PACKAGE OUTLINE

SOP-28-375-1.27 Unit: mm



SOP-32-375-1.27 Unit: mm



ATTACH

System Function Table

Periphery module	Entry address	Function description
FLASH memory	002EH	Block erase
	0034H	Single byte write
	003AH	Block write
Code sampling module	0049H	Set infrared receiving mode
	0040H	Initialize the wave sampling circuit
	0046H	On-off wave sampling circuit
	0043H	Capture envelope data pointer
Code transmitting modlue	004CH	Set carrier parameter
	004FH	Set scaler coeffiecent and base unit time
	0052H	Initialize frame interval timer
	0055H	Set frame interval time
	0058H	8-bit code transmitting
	005BH	16-bit code transmitting
	005EH	Wait for the data in the buffer completing
	0061H	Close frame interval timer

HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

Note：Silan reserves the right to make changes without notice in this specification for the improvement of the design and performance. Silan will supply the best possible product for customers