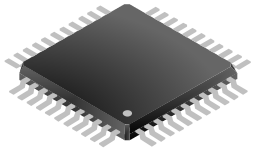
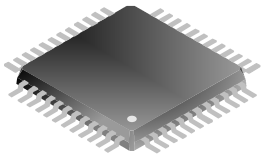
LOW POWER 8-BIT MCU INTEGRATED WITH LCD DRIVER AND CHARGE PUMP

DESCRIPTION

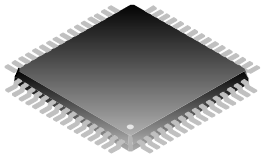
SC51P18A16 is an 8-bit MCU integrated with LCD driver and charge pump. It uses SC51 core with built-in 16K-byte OTP and 512-byte RAM, 8MHz high precision RC oscillator, rail-to-rail analog comparator, flexible clock system, rich timer resource and communication interface, which designed for various control applications. It features 1.8V~3.6V operating voltage range, low display current in IDLE mode, and ultra-low Stop current, which makes it well suitable for the battery-powered systems.



LQFP44-10 x10-0.8



LQFP-48-7×7-0.5



LQFP-64-10x10-0.5

APPLICATION

- Air conditioner remote control
- Medical and healthcare equipments
- Panel display
- Audio system
- Intelligent instruments

FEATURES

- 8 bit SC51 CPU
  - Compatible with MCS51 instruction set, dual DPTR; support software reset instruction.
  - Improved instruction structure, the execution time of 90% instructions is two to four clock cycles.
- On-Chip Memory
  - 16K-byte OTP, data retention time > 10 years.
  - 512-byte RAM.
  - Support In-System-Programming (ISP), only 5 pins are needed (including VDD/VSS).
  - Support multi-time-programming (MTP): 4Kx4 times/8Kx2 times/16Kx1 time.
  - Support OTP page encryption, page size: 4K.
- Power supply and Reset
  - Operating voltage: 1.8V~3.6V.
  - Built-In Power-On-Reset (POR).
  - Built-In Low-Voltage-Reset (LVR) with 2 levels selectable:1.7V, 2.4V.
  - Built-In Low-Voltage-Detect (LVD) with 8 levels selectable:2.0V, 2.1V, 2.2V, 2.3V, 2.4V, 2.5V, 2.7V, 3.0V.
  - Built-in watchdog (WDT).
- System clock
  - Built-In 32KHz low frequency Oscillator (RCL).
  - Built-In 8MHz high precision Oscillator (RCH), ±1% @V_{DD}=1.8~3.6V, T_A=-10~50℃.
  - External 1~8MHz high frequency crystal oscillator or External 32.768KHz low frequency crystal oscillator,

configured by information byte.

- Pre-scale factors for system clock: 8/4/2/1.
- CPU maximum operating frequency: 8MHz @V_{DD}=2.4V~3.6V.

- Input/output
  - Support up to 54 I/O Ports.
  - Built-in high current open-drain output transistor, I_{OL}=200mA or 230mA @ V_{OL}=0.3V, V_{DD}=3V.
  - Keyboard Interrupt wake-up function at P0,P1,P2,P4 (total 32 pins), interrupt polarity selectable.
  - 4-channel external interrupt, interrupt polarity selectable.
- Peripherals
  - 2 channel 16-bit Timers (T0/T1), compatible with traditional MCS51. T0 supports square wave output while T1 supports PWM output.
  - 1 channel 16-bit Timer2 with capture function.
  - 1 channel Carrier Timer for carrier modulation and demodulation (CRT).
  - 1 channel 8-bit PWM generator, with arbitrary settable period and high 6-bit settable duty cycle (low 2 bits fixed as 0).
  - 1 channel 8-bit WT timer, generating Buzzer output with 4 kinds of frequency selectable (8K/4K/2K/1KHz).
  - 1 channel UART with configurable high-precision baud rate.
  - 1 channel SPI, supporting up to 4Mbps @system clock = 8MHz.
  - 1 channel rail-to-rail analog comparator (ACMP) with 16 levels reference voltage selectable, which source is selectable between band gap voltage(VBG) and V_{DD} .
  - Built-in LCD driver with charge pump, supporting up to 4*36, 5*35 and 6*34 segment, 1/2 and 1/3 bias selectable.
- Operation Modes
  - Normal mode.
  - IDLE mode.
  - STOP mode.
- Package Type
  - LQFP-44-10*10-0.8
  - LQFP-48-7*7-0.5
  - LQFP-64-10*10-0.5

ORDERING INFORMATION

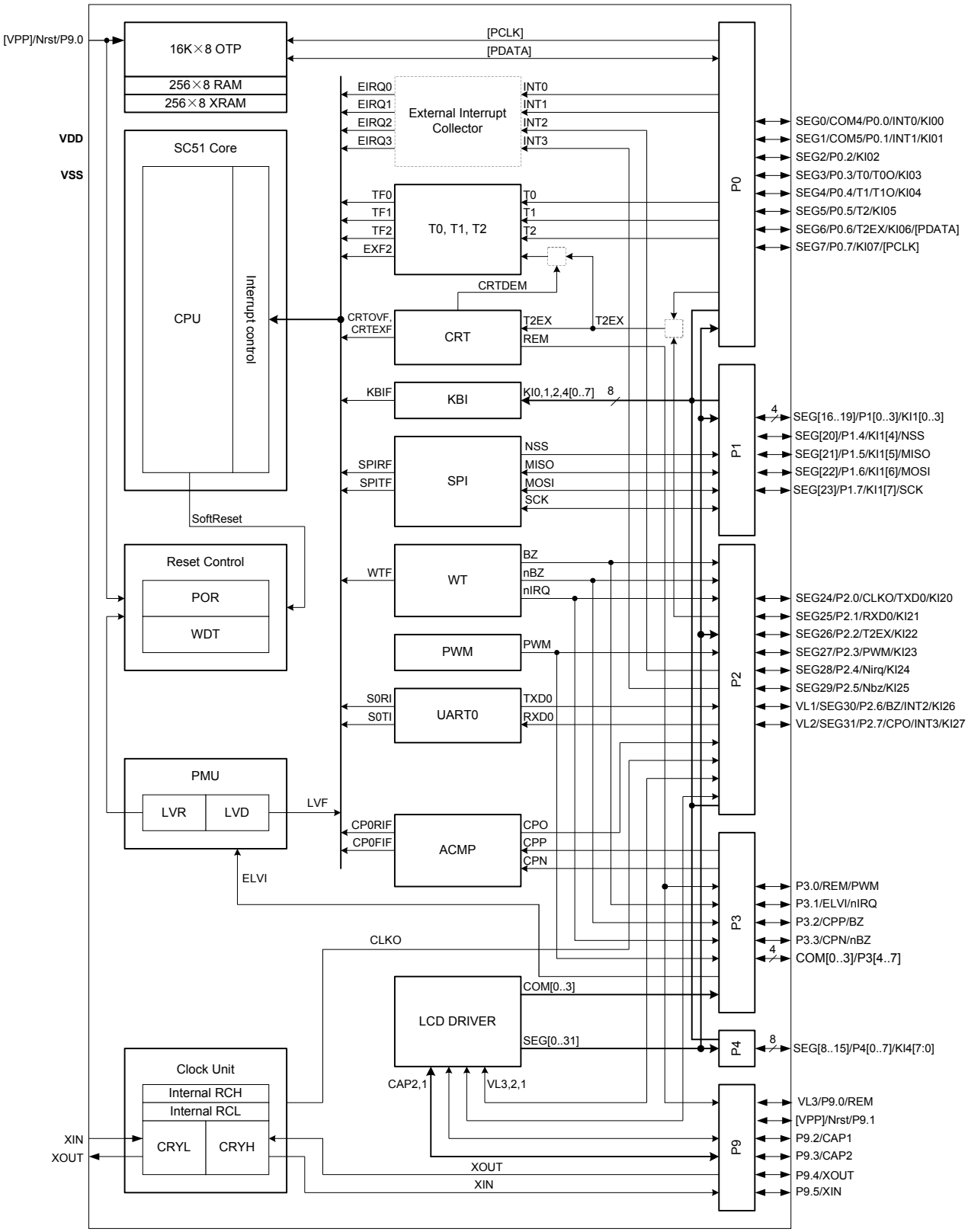
Ordering information

Part No.	Package	Marking	Hazardous substance control	Packing
SC51P18A16LLG	LQFP-48-7×7-0.5	18A16LLG	Halogen free	Tray
SC51P18A16LBG	LQFP-64-10×10-0.5	18A16LBG	Halogen free	Tray
SC51P18A16LAG	LQFP-44-10×10-0.8	18A16LAG	Halogen free	Tray

Resource information

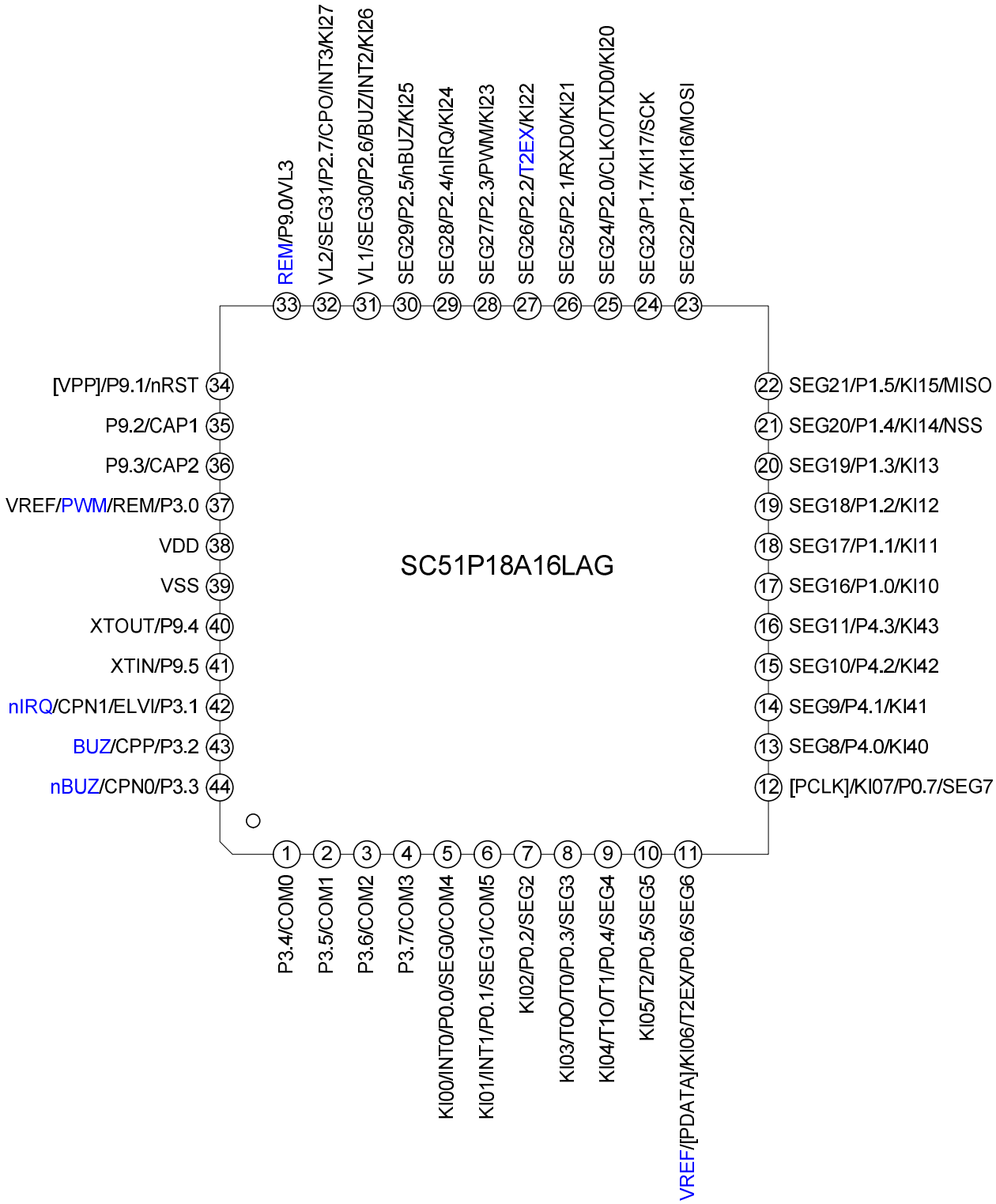
Resource	SC51P18A16		
Package	LQFP-44	LQFP-48	LQFP-64
OTP	16K*8	16K*8	16K*8
RAM	512*8	512*8	512*8
I/O	42	46	54
External interrupt	4	4	4
T0	Y	Y	Y
T1	Y	Y	Y
T2	Y	Y	Y
CRT	Y	Y	Y
PWM	Y	Y	Y
WT	Y	Y	Y
KBI	28	32	32
CMP	Y	Y	Y
UART	Y	Y	Y
SPI	Y	Y	Y
LCD	4*28/5*27/6*26	4*32/5*31/6*30	4*36/5*35/6*34

BLOCK DIAGRAM



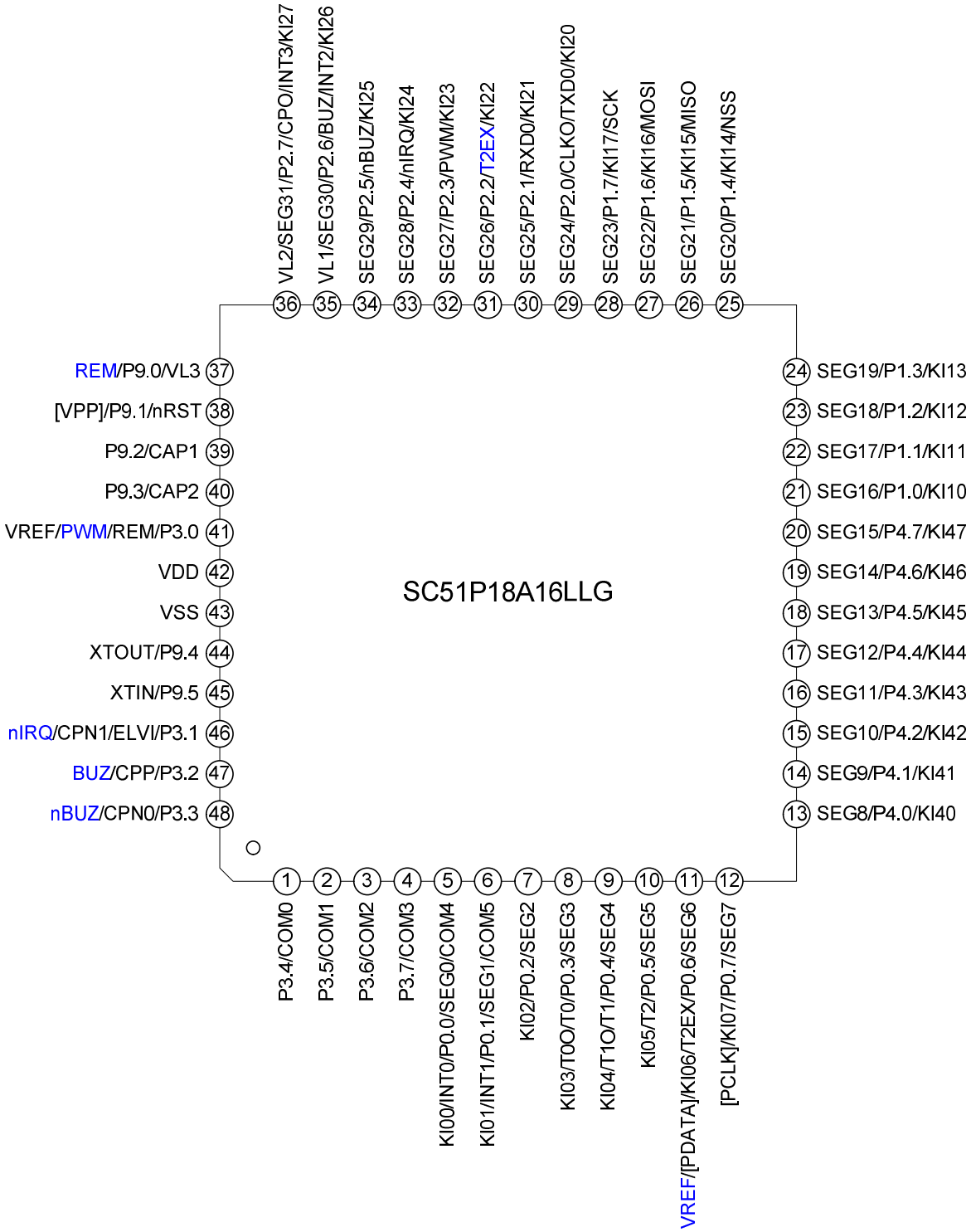
PIN CONFIGURATION

LQFP-44:SC51P18A16LAG



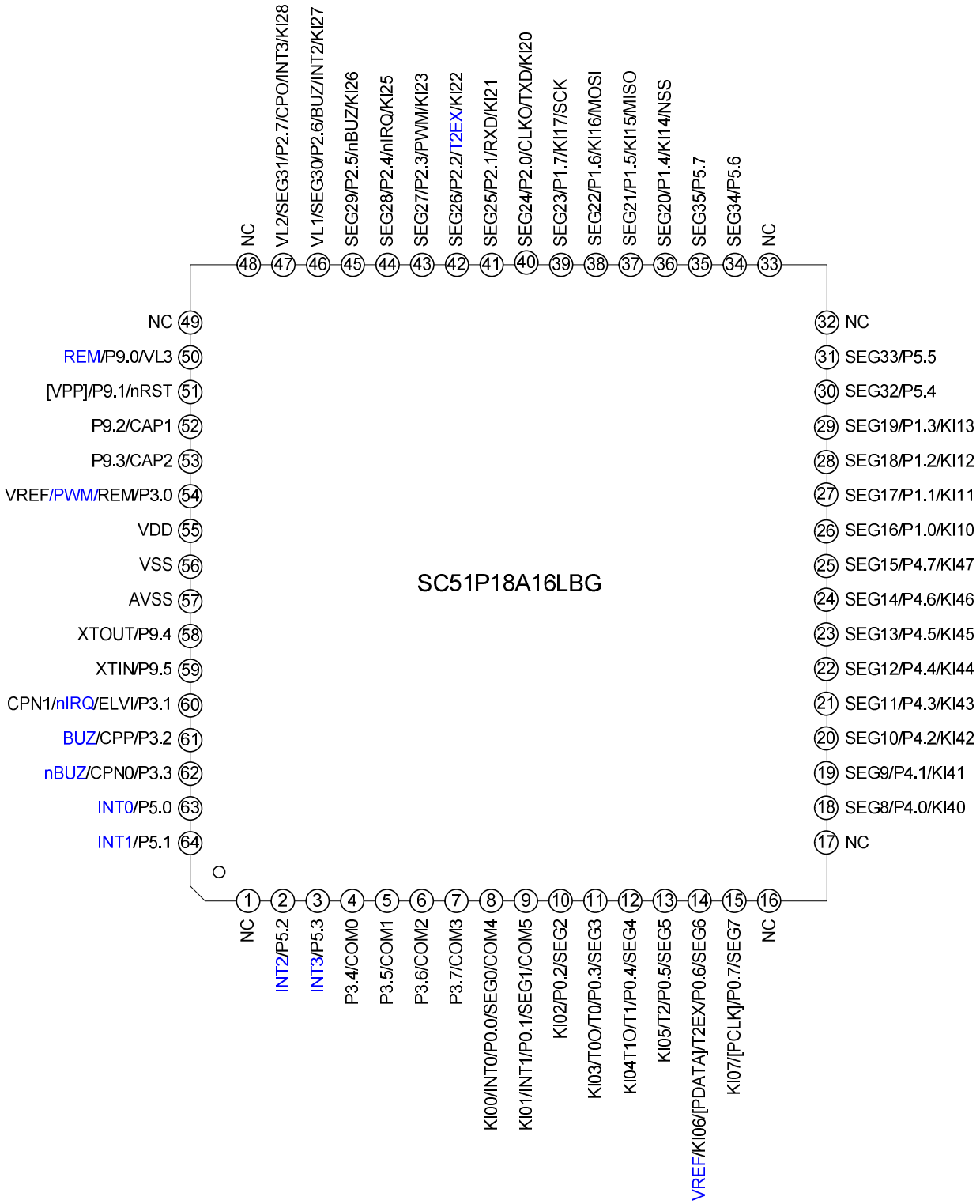
Note：Pin in blue needs remap.

LQFP-48: -SC51P18A16LLG:



Note：Pin in blue needs remap.

LQFP-64:SC51P18A16LBG:



Note：Pin in blue needs remap.

PIN DESCRIPTION

Pin multiplex

I/O	5V	Pin No.			System	Timer	Keyboard interrupt	Comm. interface	Comparator	LCD driver
		-LA	-LL	-LB						
P0.0	√	5	5	8	INT0	--	KI00	--	--	SEG0/ COM4
P0.1	√	6	6	9	INT1	--	KI01	--	--	SEG1/ COM5
P0.2	√	7	7	10	--	--	KI02	--	--	SEG2
P0.3	√	8	8	11	--	T0/ T0O	KI03	--	--	SEG3
P0.4	√	9	9	12	--	T1/ T1O	KI04	--	--	SEG4
P0.5	√	10	10	13	--	T2	KI05	--	--	SEG5
P0.6	√	11	11	14	VREF/ [PDATA]	T2EX	KI06	--	--	SEG6
P0.7	√	12	12	15	[PCLK]	--	KI07	--	--	SEG7
P1.0	√	17	21	26	--	--	KI10	--	--	SEG16
P1.1	√	18	22	27	--	--	KI11	--	--	SEG17
P1.2	√	19	23	28	--	--	KI12	--	--	SEG18
P1.3	√	20	24	29	--	--	KI13	--	--	SEG19
P1.4	√	21	25	36	--	--	KI14	NSS	--	SEG20
P1.5	√	22	26	37	--	--	KI15	MISO	--	SEG21
P1.6	√	23	27	38	--	--	KI16	MOSI	--	SEG22
P1.7	√	24	28	39	--	--	KI17	SCK	--	SEG23
P2.0	√	25	29	40	CLKO	--	KI20	TXD0	--	SEG24
P2.1	√	26	30	41	--	--	KI21	RXD0	--	SEG25
P2.2	√	27	31	42	--	T2EX	KI22	--	--	SEG26
P2.3	√	28	32	43	--	PWM	KI23	--	--	SEG27
P2.4	√	29	33	44	--	nIRQ	KI24	--	--	SEG28
P2.5	√	30	34	45	--	nBUZ	KI25	--	--	SEG29
P2.6	√	31	35	46	INT2	BUZ	KI26	--	--	SEG30/ VL1
P2.7	√	32	36	47	INT3	--	KI27	--	CPO	SEG31 VL2
P3.0	×	37	41	54	VREF	REM/ PWM	--	--	--	--
P3.1	×	42	46	60	ELVI	nIRQ	--	--	CPN1	--
P3.2	×	43	47	61	--	BUZ	--	--	CPP	--
P3.3	×	44	48	62	--	nUZ	--	--	CPN0	--

I/O	5V	Pin No.			System	Timer	Keyboard interrupt	Comm. interface	Comparator	LCD driver
		-LA	-LL	-LB						
P3.4	√	1	1	4	--	--	--	--	--	COM0
P3.5	√	2	2	5	--	--	--	--	--	COM1
P3.6	√	3	3	6	--	--	--	--	--	COM2
P3.7	√	4	4	7	--	--	--	--	--	COM3
P4.0	√	13	13	18	--	--	KI40	--	--	SEG8
P4.1	√	14	14	19	--	--	KI41	--	--	SEG9
P4.2	√	15	15	20	--	--	KI42	--	--	SEG10
P4.3	√	16	16	21	--	--	KI43	--	--	SEG11
P4.4	√	--	17	22	--	--	KI44	--	--	SEG12
P4.5	√	--	18	23	--	--	KI45	--	--	SEG13
P4.6	√	--	19	24	--	--	KI46	--	--	SEG14
P4.7	√	--	20	25	--	--	KI47	--	--	SEG15
P5.0	×	--	--	63	INT0	--	--	--	--	--
P5.1	×	--	--	64	INT1	--	--	--	--	--
P5.2	×	--	--	2	INT2	--	--	--	--	--
P5.3	×	--	--	3	INT3	--	--	--	--	--
P5.4	√	--	--	30	--	--	--	--	--	SEG32
P5.5	√	--	--	31	--	--	--	--	--	SEG33
P5.6	×	--	--	34	--	--	--	--	--	SEG34
P5.7	×	--	--	35	--	--	--	--	--	SEG35
P9.0	√	33	37	50	--	REM	--	--	--	VL3
P9.1	√	34	38	51	nRST/ [VPP]	--	--	--	--	--
P9.2	√	35	39	52	--	--	--	--	--	CAP1
P9.3	√	36	40	53	--	--	--	--	--	CAP2
P9.4	×	40	44	58	XTOUT	--	--	--	--	--
P9.5	×	41	45	59	XTIN	--	--	--	--	--
VDD		38	42	55	--	--	--	--	--	--
VSS		39	43	56	--	--	--	--	--	--
AVSS		39	--	57	--	--	--	--	--	--
NC		--	--	1,16, 17, 32, 33,48 ,49	--	--	--	--	--	--

Note: pin in blue needs remap.

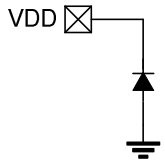
Pin Description

Pin Name	Pin Type	Function description
PORT		
P0.0-P0.7	I/O	8-bit bidirectional I/O ports, bit operation available
P1.0-P1.7	I/O	8-bit bidirectional I/O ports, bit operation available
P2.0-P2.7	I/O	8-bit bidirectional I/O ports, bit operation available
P3.0-P3.7	I/O	8-bit bidirectional I/O ports, bit operation available
P4.0-P4.7	I/O	8-bit bidirectional I/O ports, bit operation inavailable
P9.0-P9.5	I/O	6-bit bidirectional I/O ports, bit operation inavailable
In-System-Programming(ISP)		
[VPP]	P	High voltage programming port
[PCLK]	I	Programming clock Input
[PDATA]	I/O	Programming data Input/output
System		
nRST	P	External reset input, low voltage active
CLKO	O	Clock output
INT0~INT3	I/O	External interrupt input 0~3
ELVI	I	External input voltage for LVD
Timer		
T0	I	Timer/counter 0 external counting clock input
T1	I	Timer/counter 1 external counting clock input
T0O	O	Timer/counter 0 output
T1O	O	Timer/counter 1 output
T2EX	I	T2 external counting input
REM	O	CRT output
PWM	O	PWM output
nIRQ	O	WT IRQ output
BUZ	O	Buzzer signal positive output
nBUZ	O	Buzzer signal inverted output
KBI		
KI00~KI07	I	8-bit Keyboard interrupt wakeup input at P0
KI10~KI17	I	8-bit Keyboard interrupt wakeup input at P1
KI20~KI27	I	8-bit Keyboard interrupt wakeup input at P2
KI40~KI47	I	8-bit Keyboard interrupt wakeup input at P4
Communication interface		
NSS	I/O	SPI enable pin
MISO	I/O	SPI master input/slave output
MOSI	I/O	SPI master output/slave input
SCK	I/O	SPI clock pin

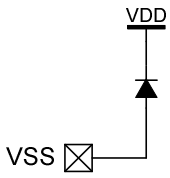
Pin Name	Pin Type	Function description
TXD0	O	UART0 data output
RXD0	I	UART0 data input
Analog comparator		
CPP	I	Analog comparator positive input
CPN0	I	Analog comparator negative input 0
CPN1	I	Analog comparator negative input 1
CPO	O	Analog comparator output
LCD driver		
SEG0~SEG31	O	LCD Segment output
COM0~COM5	O	LCD Com output
CAP1	P	Connecting LCD bias capacitor
CAP2	P	Connecting LCD bias capacitor
VL1	P	LCD power
VL2	P	LCD power
VL3	P	LCD power
Power supply		
VDD	P	Power supply
VSS	P	Ground

Note: For Pin Type: “P” denotes Power pins, “I/O” denotes normal input/output pins, “I” denotes input pins, “O” denotes output pins.

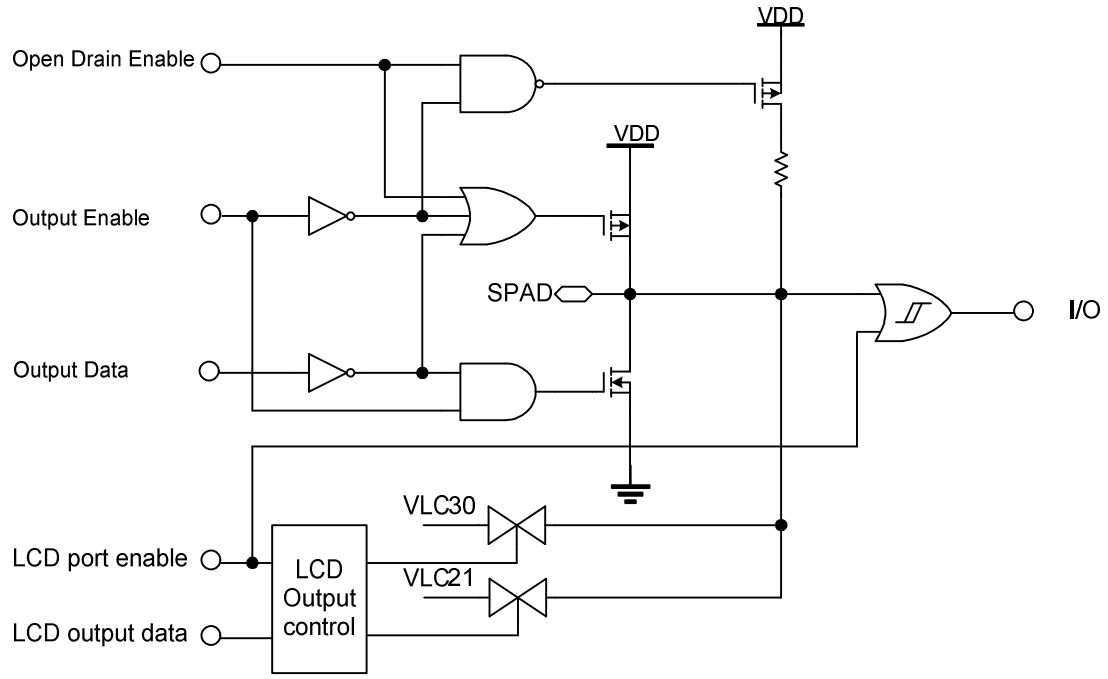
PIN STRUCTURE



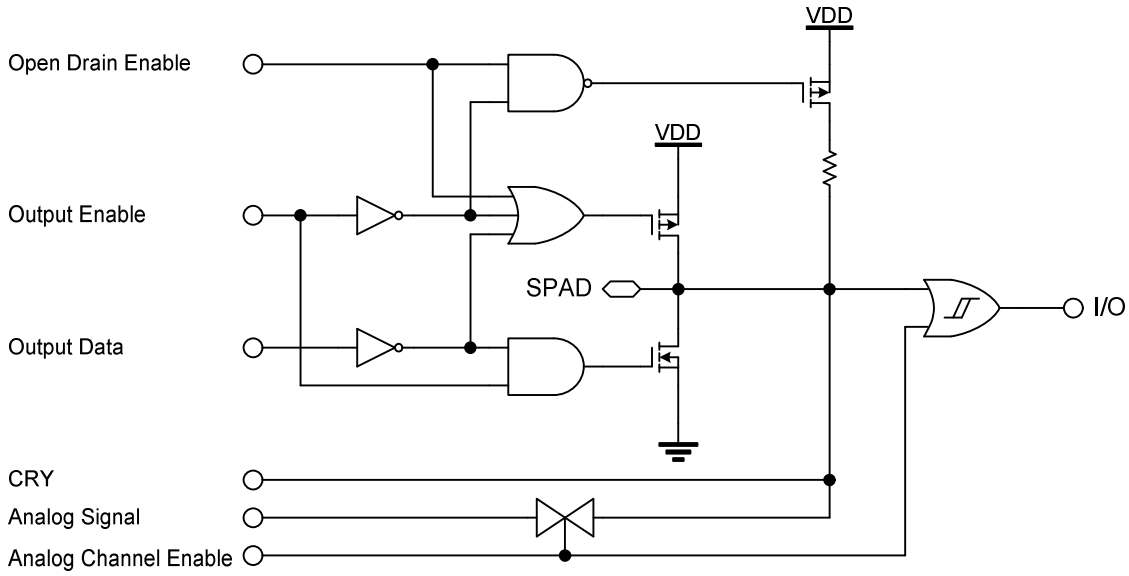
Pin Structure P1



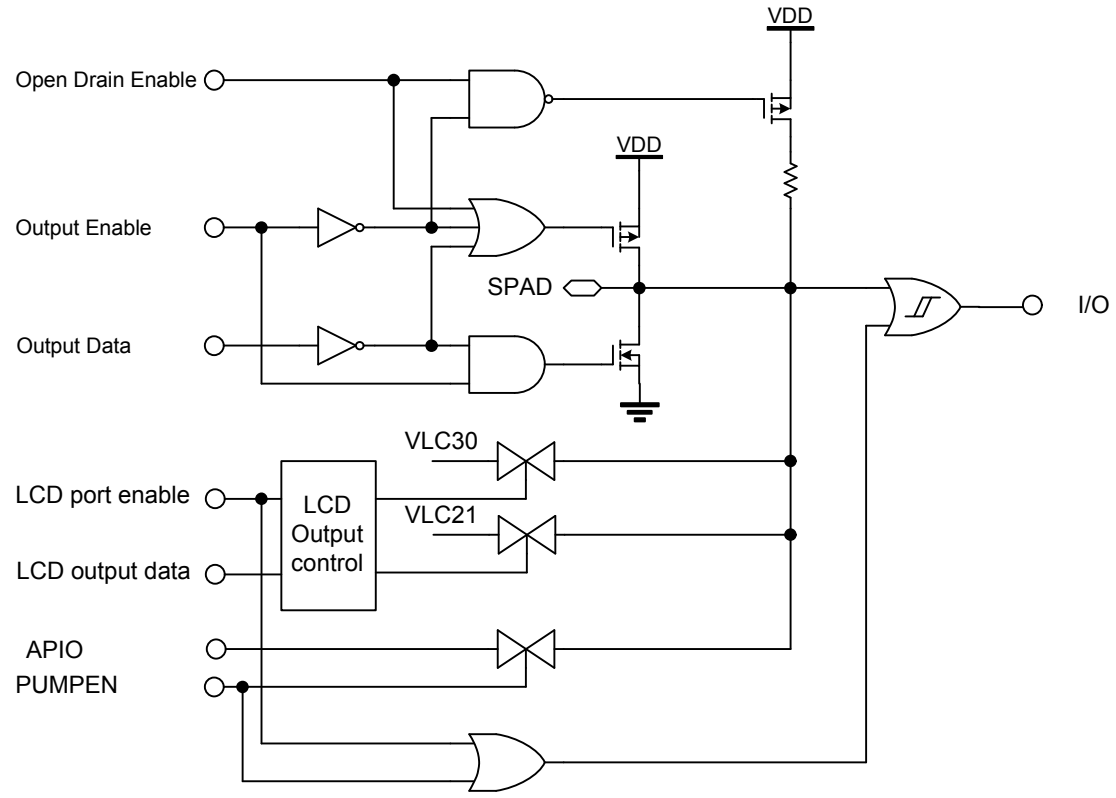
Pin Structure P0



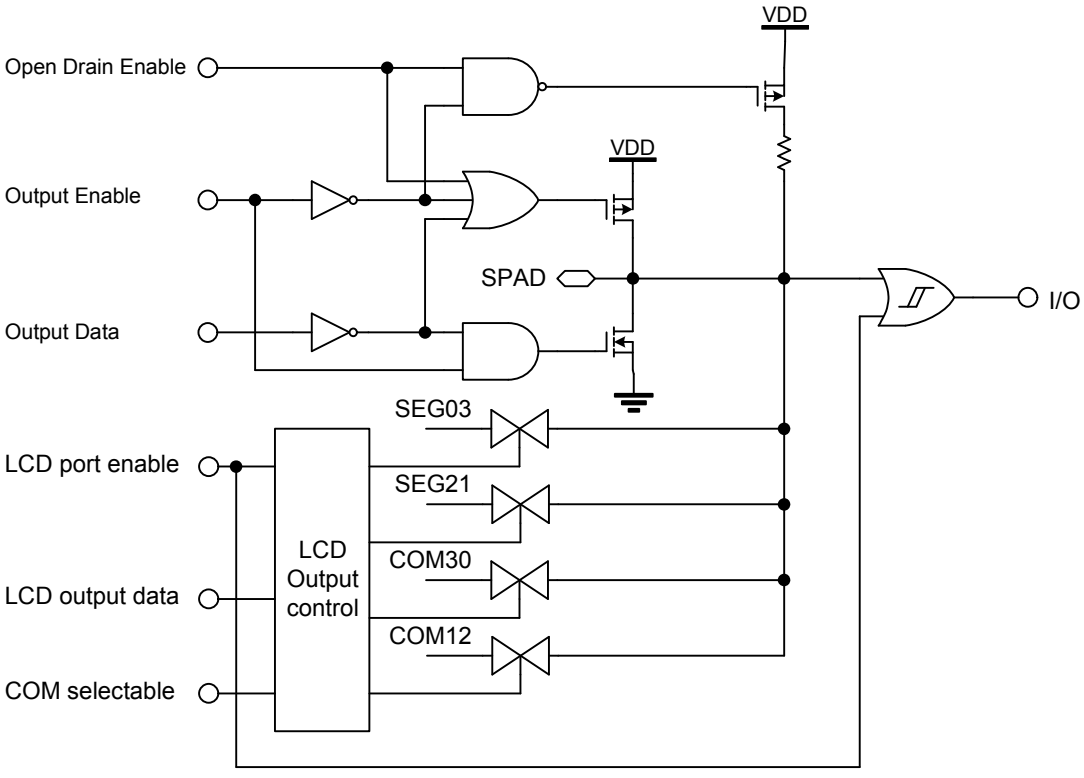
A：reused with LCD Pin Structure



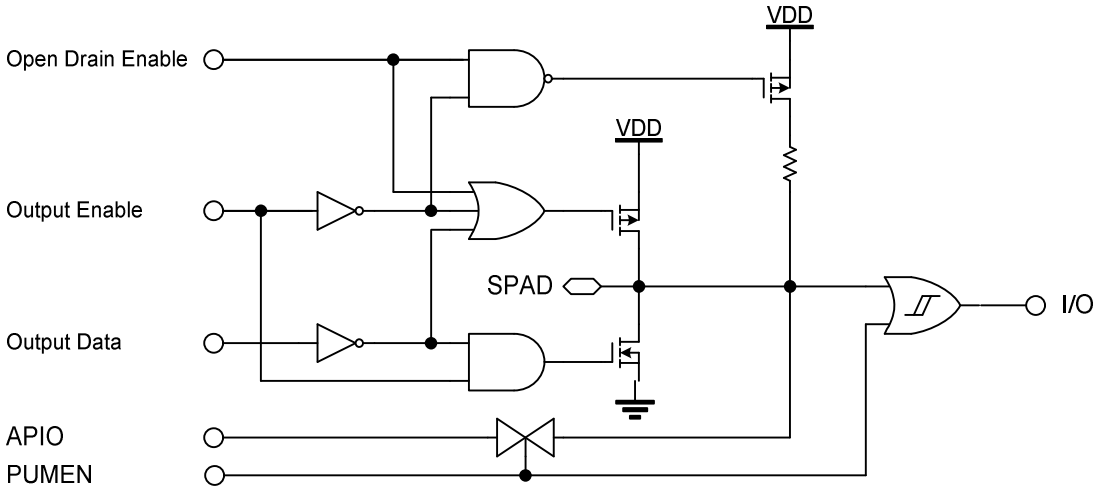
B：reused with Crystal oscillator or analog Pin Structure



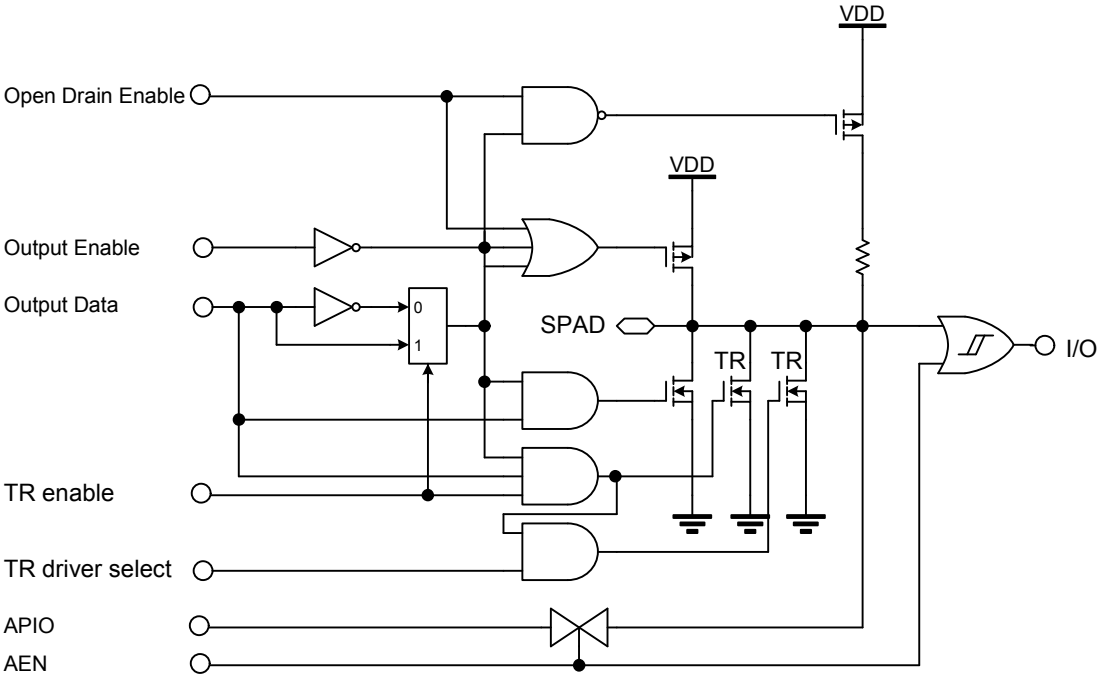
C：reused with LCD or charge pump Pin Structure



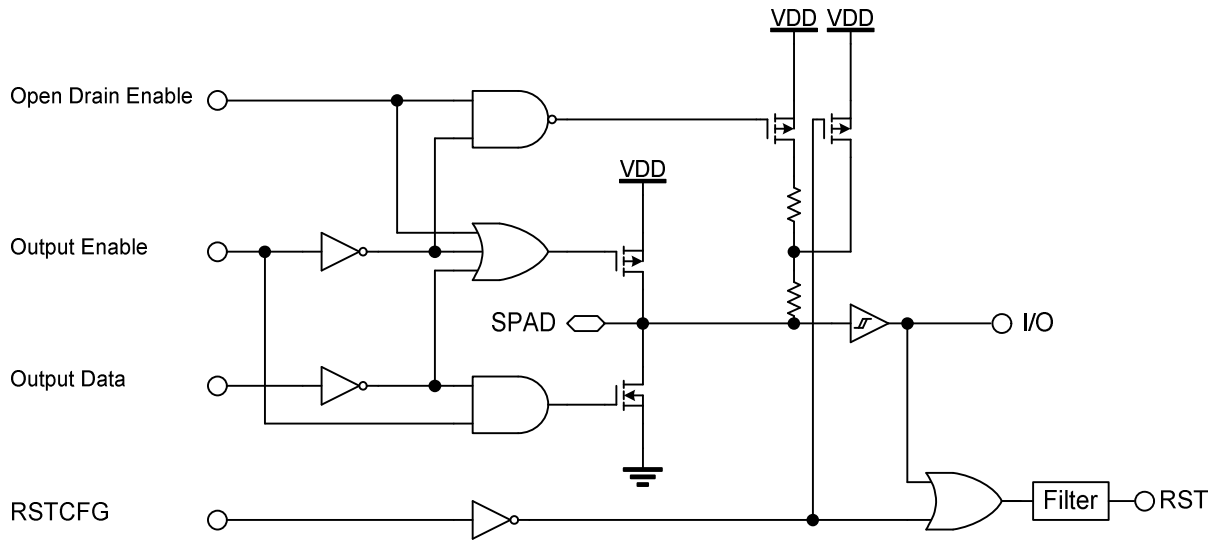
D：reused with LCD seg or com Pin Structure



E：reused with charge pump Pin Structure



F：reused with TR Pin Structure



G：reused with RST Pin Structure

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed as “absolute maximum rating” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability,

Voltage characteristics

Ratings	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-	-0.3	-	5.4	V
Input voltage	V_{IN}	P0.5	-0.3	-	6.75	
		IO except for P0.5	-0.3	-	V_{DD}+0.3	

Note: unless otherwise specified, all voltages are referenced to V_{SS}.

Current characteristics

Ratings	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total current into VDD power lines	I_{VDD}	-	-	-	80	mA
Total current out of VSS ground lines	I_{VSS}	Built-in TR not included	-	-	80	
Injected current	I_{INJ}	$V_{IN}>V_{DD}$ or $V_{IN}<V_{SS}$	-4	-	4	
		$V_O>V_{DD}$ or $V_O<V_{SS}$	-4	-	4	
Total injected current	ΣI_{INJ}	-	-20	-	20	

Thermal characteristics

Ratings	Symbol	Conditions	Min.	Typ.	Max.	Unit
Ambient temperature	T_A	-	-40	-	85	°C
Storage temperature	T_{STG}	-	-55	-	125	
Junction temperature	T_J	-	-	-	150	
Thermal resistance	θ_{JA}	LQFP-48	-	78	-	°C /W
		LQFP-64	-	76	-	
Power dissipation	P_D	-	-	-	800	mW

Note: thermal resistance is related with package form, PCB, working environment and power dissipation.

ESD Protection and static Latch-up Immunity

Ratings	Symbol	Conditions	Min.	Typ.	Max.	Unit
HBM	V_{HBM}	MIL-STD-883H	±2000	-	-	V
MM	V_{MM}	JESD22-A115	±200	-	-	
CDM	V_{CDM}	JESD22-C101E	±1000	-	-	
Latch-up trigger current	I_{LAT}	JEDEC standard NO.78D 2011.11	±100	-	-	mA
VDD overstress	V_{LAT}		5.4	-	-	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	-	1.8	3.3	3.6	V
CPU clock frequency	F_{CPU}	VDD=1.8~3.6V	-	-	4	MHz
		VDD=2.4~3.6V	-	-	8	
POR re-arm voltage	V_{PORR}	-	-	0.3	-	V
POR release delay	t_{PWRT}	-	1	-	-	ms
VDD rise time rate	S_{VDD}	Ensure POR is active	0.1	-	-	V/ms
RAM retention voltage	V_{DR}	TA=-40~85°C	0.8	-	-	V

DC ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE SPECIFIED, V_{DD}=3V, T_{AMB}=25°C)

Note: typical data are given only as design guidelines and are not tested on production.

Power supply characteristics

The MCU is placed under the following conditions:

- All IO pins in input mode with a static value at V_{DD} or V_{SS}, or in output 0 mode(no load);
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Table 1: Power supply

Characteristics	Symbol	Test condition		Min.	Typ.	Max.	Unit
Operating Current	I_{DD}	MCLK=1MHz, from RCH/8		-	0.56		mA
		MCLK=2MHz, from RCH/4		-	0.77		
		MCLK=4MHz, from RCH/2		-	1.2		
		MCLK=8MHz, from RCH/1		-	2.0		
		MCLK=1MHz, from CRY8M/8, max gain		-	1.2		
		MCLK=2MHz, from CRY8M/4, max gain		-	1.4		
		MCLK=4MHz, from CRY8M/2, max gain		-	1.8		
		MCLK=8MHz, from CRY8M/1, max gain		-	2.8		
		MCLK=1MHz, from CRY4M/4, max gain		-	0.82		
		MCLK=4MHz, from CRY4M/1, max gain		-	1.5		
		MCLK=32KHz, from CRY32K/1, max gain		-	120		µA
Idle current	I_{IDLE}	MCLK=1MHz, from RCH/8		-	0.29		mA
		MCLK=2MHz, from RCH/4		-	0.33		
		MCLK=4MHz, from RCH/2		-	0.43		
		MCLK=8MHz, from RCH/1		-	0.6		
		MCLK=8MHz, from CRY8M/1, max gain		-	1.26		
		MCLK=4MHz, from CRY4M/1, max gain		-	0.8		
		MCLK=32KHz, from CRY32K/1, max gain		-	18		µA
Stop current	I_{STOP}	Capacitor-type, 1/3 bias	VLL3=V_{DD}	-	3.5		µA
			VLL2=V_{DD}	-	3.5		
		Built-in reference capacitor-type, Vref=1.0V		-	TBD		
		All module disabled		-	0.1		

IO characteristics

Table 2: IO characteristics

Characteristics	Symbol	Test condition		Min.	Typ.	Max.	Unit
High input voltage	V_{IH}	All port		0.7*V_{DD}	-	V_{DD}	V
Low input voltage	V_{IL}	All port except for P9.1		0	-	0.4*V_{DD}	V
		P9.1(used as GPIO)		0	-	0.3*V_{DD}	
		P9.1(used as nRST)		0	-	0.2*V_{DD}	
Input hysteresis	$V_{HYS\ (IO)}$	All port except for P9.1		-	150	-	mV
		P9.1(used as nRST)		-	200	-	mV
		P9.1(used as GPIO)			300		mV
V_{DD}=3.0V							
Output source current	I_{OH}	V_{DD}=3V，V_{OH}=0.9*V_{DD}	All port except for P3.0 and 9.0	-	4	-	mA
			P3.0/P9.0	-	12.0	-	
Output sink current	I_{OL}	V_{DD}=3V，V_{OL}=0.1*V_{DD}	All port	-	8.0	-	mA
			TR (low level)	-	200	-	
			TR (high level)	-	230	-	
Total current	Itotal	-	All ports	-	-	60	mA
Pull-up resistor	Rpu	V_{IN}=0V	All port except for P9.1	100	150	200	kΩ
			P9.1(used as GPIO)	100	150	200	
			P9.1(used as nRST)	10	30	50	
Leakage current (high temperature)	I_{IL}	V_{SS}＜V_{PIN}＜V_{DD}, T_A=85°C		-	±20	±100	nA
Effective pulse width (filtering)	T_{PW}(IO)	External reset pin		-	2	4	Us

Note : typical value is sampled result, not tested in production.

System monitoring and reset characteristics

Table 3: System monitoring and reset

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Bandgap voltage	V_{BG}	1.8~3.6V, -40～85°C	1.18	1.205	1.22	V
Low reset voltage	V_{LVR}	LVRS=0	1.65	1.7	1.75	V
		LVRS=1	2.5	2.6	2.7	
LVR release hysteresis voltage	$V_{HYS(LVR)}$	-	-	50	-	mV
LVR module operating current	I_{LVR}	Enabled in IDLE mode	-	20	-	μA
LVD voltage	V_{LVD}	LVLS= 000	1.95	2.0	2.05	V

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
		LVLS = 001	2.05	2.1	2.15	
		LVLS = 010	2.15	2.2	2.25	
		LVLS = 011	2.25	2.3	2.35	
		LVLS = 100	2.35	2.4	2.45	
		LVLS = 101	2.45	2.5	2.55	
		LVLS = 110	2.65	2.7	2.75	
		LVLS = 111	2.95	3.0	3.05	
LVD release hysteresis voltage	$V_{HYS(LVD)}$	$V_{DD}\geqslant 2.7$	-	200	-	mV
		$V_{DD}<2.7$	-	150	-	
LVD module operating current	I_{LVD}	IDLE mode	-	40	-	μA

Note : typical value is sampled result, not tested in production.

Oscillation and clock characteristics

Table 4: Oscillation and clock characteristics

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Internal RCH after calibration*	F_{RCH}	1.8~3.6V, -10～50°C	7.92	8.00	8.08	MHz
		1.8~3.6V，-40～85°C	7.84	8.00	8.16	
RCH operating current*	I_{RCH}	3.0V, 25°C	-	100	-	μA
Internal RCL	F_{RCL}	1.8~3.6V, -40～85°C	6	32	60	KHz
RCL operating current	I_{RCL}		-	0.3	1.0	μA

Note : typical value is sampled result, not tested in production.

Analog comparator characteristics

Table 5: Electrical characteristics of ACMP

Characteristics		Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=3.0V, temperature=25°C, Vcm=V_{DD}/2.							
Input offset voltage* (CPP rising edge)		Vos	-	-50	0	50	mV
Input common mode voltage		Vcm	Response time <200ns	0	-	V_{DD}	V
			Response time <1μs	0	-	V_{DD}	V
Common Mode Rejection Ratio		CMRR	Ambient temperature 25°C	-	2	-	mV/V
Comparator hysteresis voltage (CPP falling edge with hysteresis)		Vhyster		-	40	-	mV
Start-up delay time		Tstr		-	0.6	2.0	μs
Respons e time	Rising edge	Trt	Vcm=0~VDD	-	100	200	ns
	Falling edge		Overdrive voltage±0.1V	-	100	200	ns
Operating current		Icmp	-	-	45	-	μA

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
CVREF Stabilization time	Tscvr	-	-	1	-	μs

Note : all data of comparator based on characterization results, not tested in production.

LCD driver characteristics

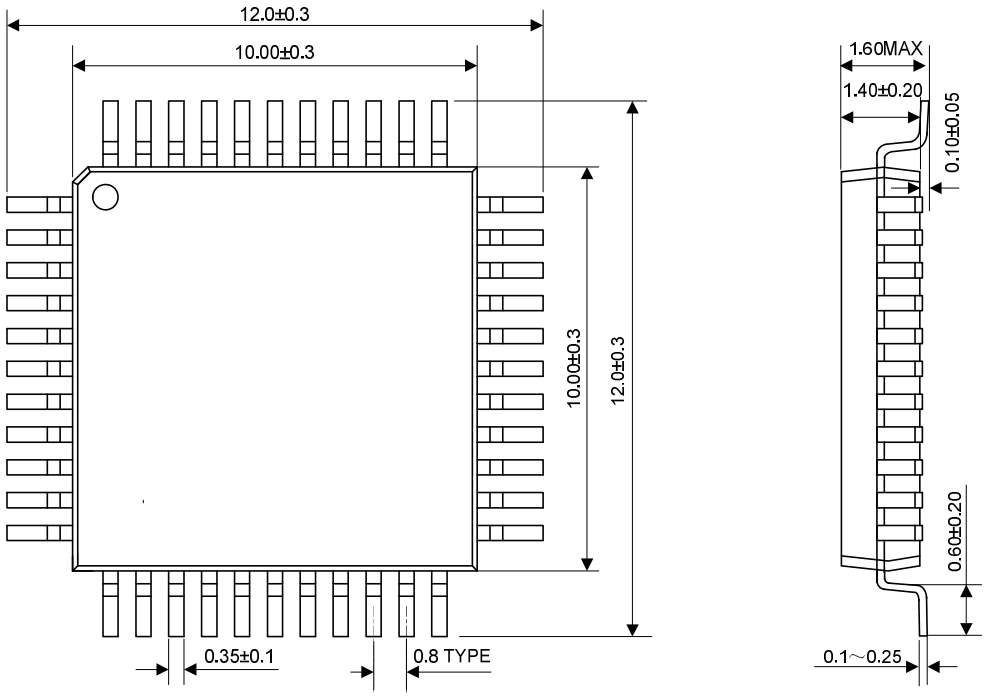
Table 6:LCD driver Electrical characteristics

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Typical condition: V_{DD}=3.0V, temperature=25°C.						
LCD driver current	I_{lcd}	Resistor- type	-	3	-	μA
		Capacitor- type with built-in reference	-	TBD	-	
		Capacitor-bias type	-	1	-	
LCD reference voltage	V_{ivr}	IVRCFG=0	-	1.018	-	V
LCD selectable reference voltage	V_{ivr}	IVRCFG=1，VOUTSEL=00	-	1.7	-	
		IVRCFG=1，VOUTSEL=01	-	1.5	-	
		IVRCFG=1，VOUTSEL=10	-	1.3	-	
		IVRCFG=1，VOUTSEL=11	-	1.1	-	

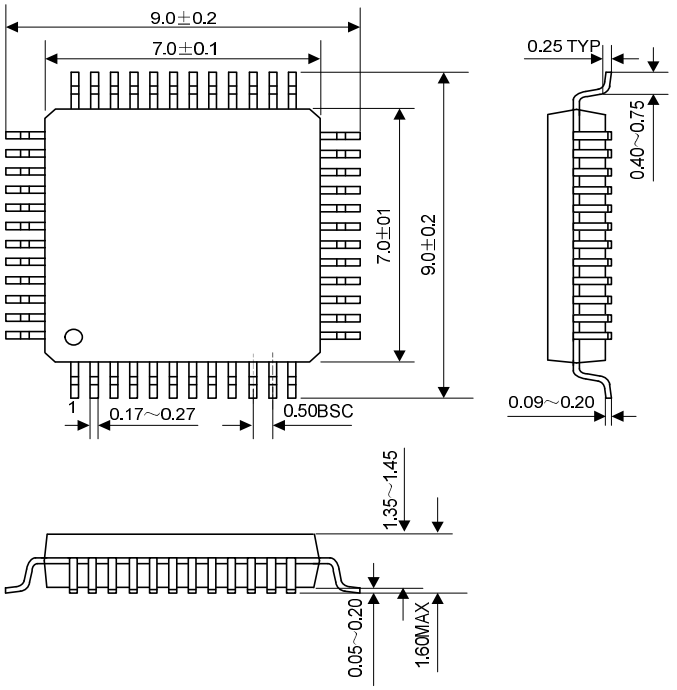
Note : all data of LCD based on characterization results, not tested in production.

PACKAGE OUTLINE

LQFP-44-10×10-0.8 UNIT: mm

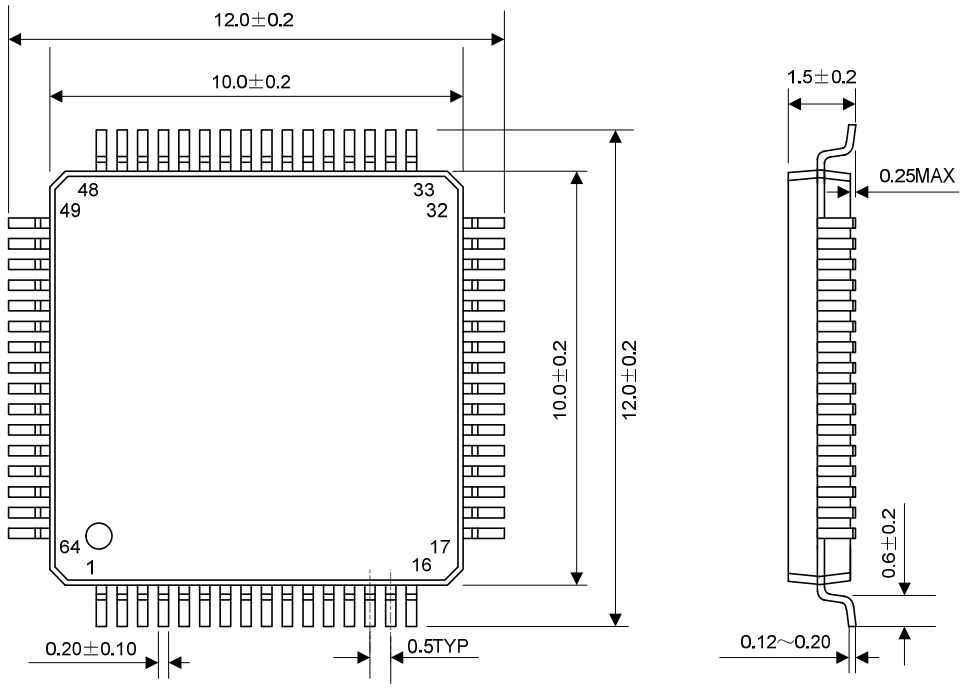


LQFP-48-7×7-0.5 UNIT: mm



PACKAGE OUTLINE(CONTINUED)

LQFP-64-10×10-0.5 UNIT: mm



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

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1. First Release