

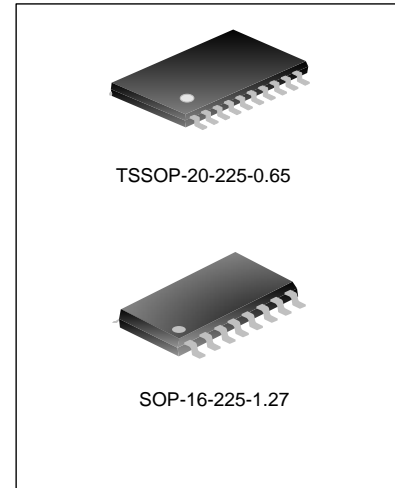
LOW VOLTAGE LOW POWER I/O TYPE MCU WITH BUILT-IN HIGH PRECISION OSCILLATOR AND E²PROM

DESCRIPTION

SC51P2320 is a 3V I/O type 8-bit low power MCU. It bases on powerful SC51 CPU core and embeds 20K-byte OTP, 768-byte RAM and 1K-byte E²PROM. It integrates comparator, voltage detector, carrier modulation and demodulation module and three configurable timers, which is very suitable for self-learning remote control. It supports three kinds of low power modes and peripheral clock gating, which is very suitable for battery-powered systems.

APPLICATION

- ◆ Self-learning remote control
- ◆ Universal remote control



FEATURES

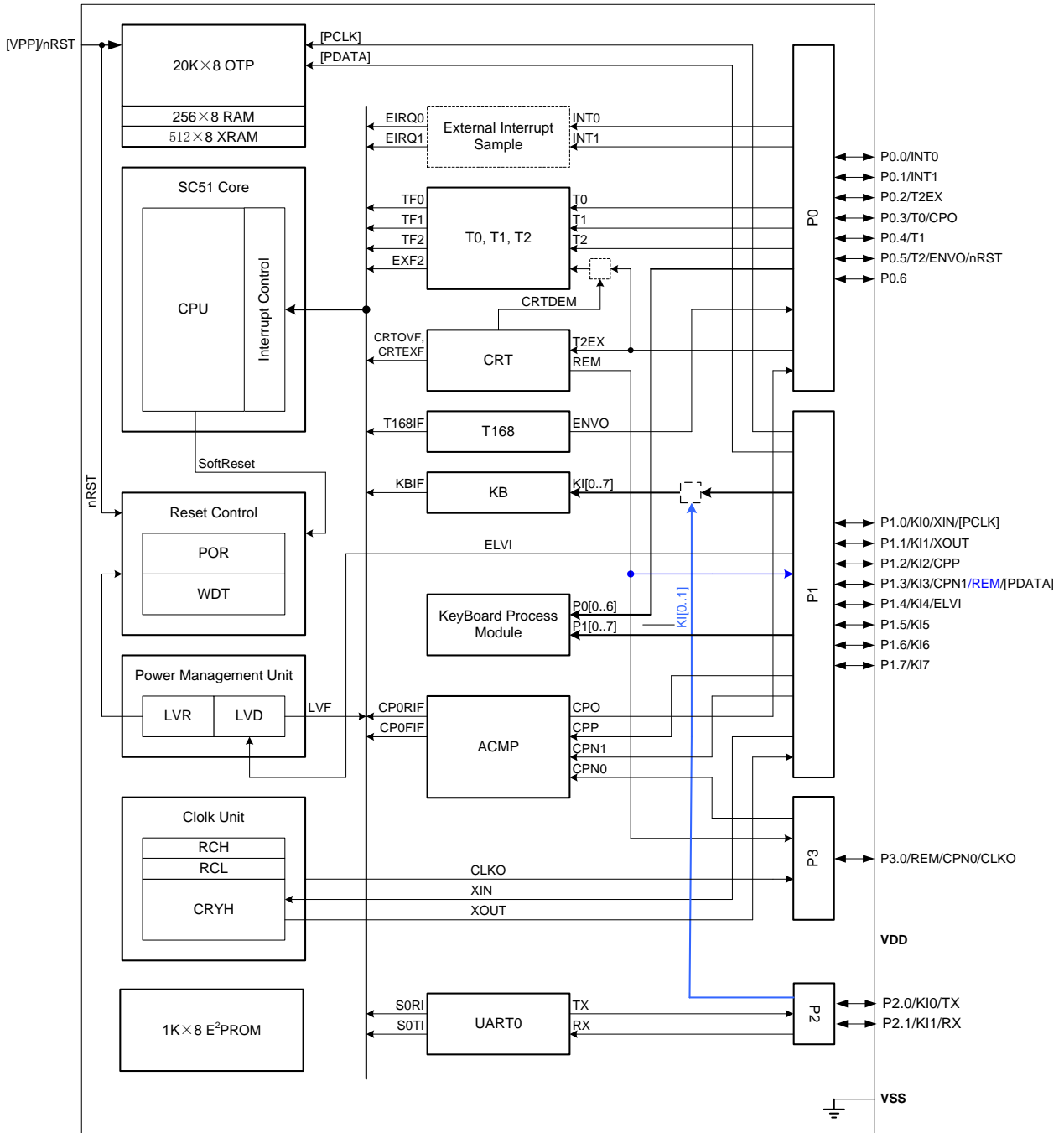
- ◆ 8 bit SC51 CPU
 - Compatible with MCS51 instructions, dual DPTR; support software reset instruction.
 - Improved instruction structure, the execution time of 90% instructions is two to four clock cycles.
 - Programmable system clock pre-divider: 1/2/8/64.
- ◆ On-Chip Memory
 - 20K-byte OTP, data retention time > 10 years.
 - 256-byte RAM, 512-byte XRAM.
 - 1K-byte E²PROM.
 - Data retention time > 10 years@85° , 20000 cycles.
 - Endurance > 100,000.
- ◆ Programming
 - Support In-System-Programming (ISP), only 5-pins are needed (including VDD/VSS).
 - Support Parallel Programming (CPP) Interface.
 - Support Multi-Time-Programming (MTP):4K×5 / 8K×2 / 20K×1.
 - Support OTP page encryption, page size: 4K.
- ◆ Integrated power monitor circuits
 - Built-In Power-On-Reset (POR).
 - Built-In Low-Voltage-Reset (LVR) with 2 levels selectable: 1.7V and 1.9V.
 - Built-In Low-Voltage-Detect (LVD) with 16 levels selectable.
- ◆ Operating Frequency Range
 - Built-In 20KHz low power Oscillator (RCL).
 - Built-In 4MHz high precision Oscillator (RCH) with ±1% frequency variation @ -10~50°C, V_{DD}=1.8~3.6V.
 - External 1~8MHz crystal oscillator.
 - CPU maximum operating frequency: 6MHz @ V_{DD}=1.8~3.6V.

- ◆ Support 12 Interrupts, including
 - 2 channel external interrupt INT0, INT1 with polarity configurable.
 - Polarity Keyboard-Interrupt (KBI) wakeup interrupt on P1 port with polarity configurable.
 - Carrier Envelope generator interrupt.
 - Carrier Timer interrupt.
 - T0/T1/T2 interrupts.
 - LVD interrupt.
 - ACMP rising edge and falling edge interrupt.
 - UART transmission interrupt.
- ◆ I/O
 - Support up to 18 I/O Ports.
 - Built-in high current open-drain output transistor, $I_{OL}=180\text{mA}$ or 250mA @ $V_{OL}=0.3\text{V}$, $V_{DD}=3\text{V}$.
- ◆ Peripherals
 - Standard 8051 T0/ T 1.
 - 16-bit T2.
 - Carrier Timer for carrier modulation and demodulation (CRT).
 - Internal Carrier envelope generator (T168).
 - One Analog Comparator (ACMP).
 - Keyboard interrupt controller (KBI).
 - Built-In Watchdog-Timer (WDT).
 - Universal Asynchronous Receiver/ Transmitter
- ◆ Support three low power operation Modes
 - IDLE Mode.
 - STOP Mode.
 - Low Voltage Stop Mode.
- ◆ Package Type
 - SOP-16-225-1.27.
 - TSSOP-20-225-0.65

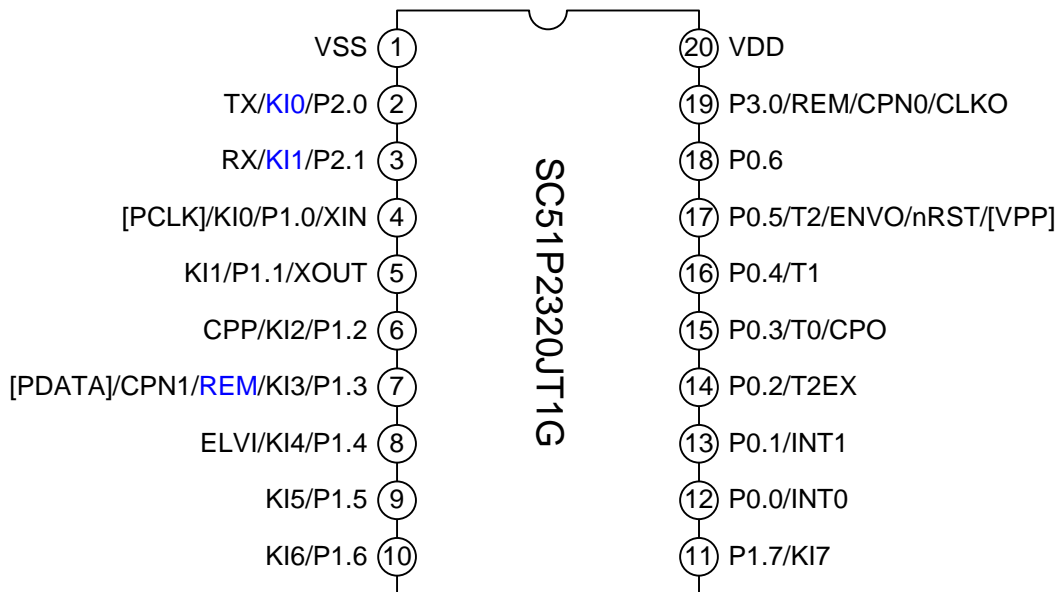
ORDERING INFORMATION

| Part No. | Package | Marking | Material | Packing |
|-----------------|-------------------|---------------|--------------|-------------|
| SC51P2320SC1G | SOP-16-225-1.27 | SC51P2320SC1G | Halogen free | tube |
| SC51P2320SC1GTR | | SC51P2320SC1G | Halogen free | Tape & Reel |
| SC51P2320JT1G | TSSOP-20-225-0.65 | 2320JT1G | Halogen free | tube |
| SC51P2320JT1GTR | | 2320JT1G | Halogen free | Tape & Reel |

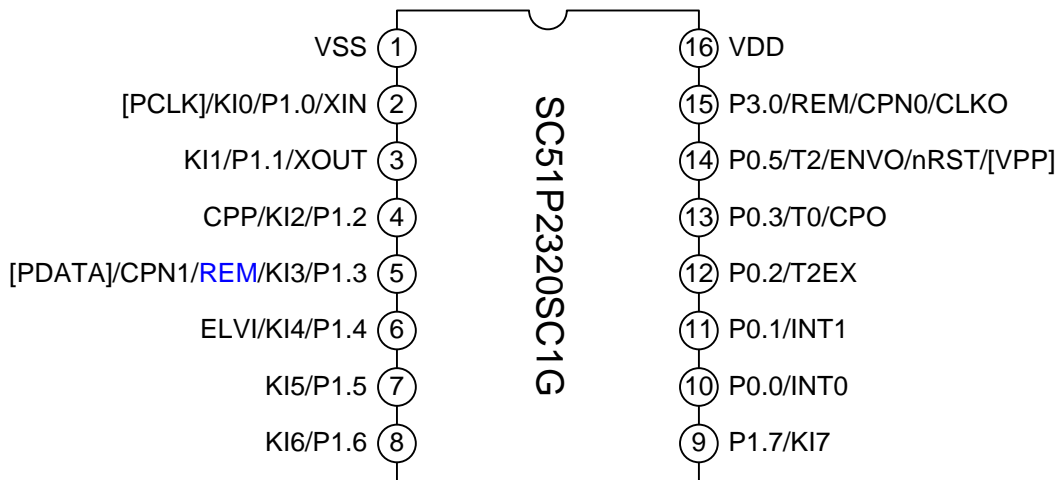
BLOCK DIAGRAM



PIN CONFIGURATION



Note1: the pins marked in blue can be remapped by software
Note2: the pins enclosed by square brackets is used for programming



Note1: the pins marked in blue can be remapped by software
Note2: the pins enclosed by square brackets is used for programming

PIN DESCRIPTION

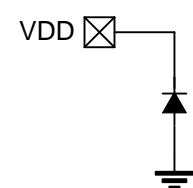
| Pin Name | Pin number | | Pin Type | Pin Structure | Function description |
|------------------------------------|------------|------|----------|---------------|----------------------|
| | -JT1 | -SC1 | | | |
| Power supply | | | | | |
| VDD | 20 | 16 | P | P1 | Power supply |
| VSS | 1 | 1 | P | P0 | Ground |
| In-System-Programming (ISP) | | | | | |

| Pin Name | Pin number | | Pin Type | Pin Structure | Function description |
|---------------------------|------------|------|----------|---------------|--|
| | -JT1 | -SC1 | | | |
| [VPP] | 17 | 14 | P | A | OTP Programming high voltage input |
| [PCLK] | 4 | 2 | I | B | OTP Programming clock Input |
| [PDATA] | 7 | 5 | I/O | B | OTP Programming data |
| System | | | | | |
| XIN | 4 | 2 | I | B& | External Crystal input |
| XOUT | 5 | 3 | O | B& | External Crystal output |
| nRST | 17 | 14 | I | A | External reset input, active low |
| CLKO | 19 | 15 | O | C | Clock output |
| ELVI | 8 | 6 | A | B | External input for LVD detect |
| I/O | | | | | |
| P0.0 | 12 | 10 | I/O | B | Normal input/output I/O, bit operation available |
| P0.1 | 13 | 11 | I/O | B | |
| P0.2 | 14 | 12 | I/O | B | |
| P0.3 | 15 | 13 | I/O | B | |
| P0.4 | 16 | - | I/O | B | |
| P0.5 | 17 | 14 | I/O | A | Input/output I/O, not support push pull output |
| P0.6 | 18 | - | I/O | B | Normal input/output I/O, bit operation available |
| P1.0 | 4 | 2 | I/O | B& | |
| P1.1 | 5 | 3 | I/O | B& | |
| P1.2 | 6 | 4 | I/O | B | |
| P1.3 | 7 | 5 | I/O | B | |
| P1.4 | 8 | 6 | I/O | B | |
| P1.5 | 9 | 7 | I/O | B | |
| P1.6 | 10 | 8 | I/O | B | |
| P1.7 | 11 | 9 | I/O | B | |
| P2.0 | 2 | - | I/O | B | Normal input/output I/O, bit operation available |
| P2.1 | 3 | - | I/O | B | |
| P3.0 | 19 | 15 | I/O | C | Normal input/output I/O, bit operation available |
| External Interrupt | | | | | |
| INT0 | 12 | 10 | I | B | External interrupt 0 input |
| INT1 | 13 | 11 | I | B | External interrupt 1 input |
| Keyboard Interrupt | | | | | |
| KI0 | 4 | 2 | I | * | Keyboard interrupt wakeup input |
| KI1 | 5 | 3 | I | * | |
| KI2 | 6 | 4 | I | B | |
| KI3 | 7 | 5 | I | B | |
| KI4 | 8 | 6 | I | B | |
| KI5 | 9 | 7 | I | B | |

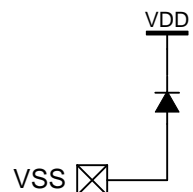
| Pin Name | Pin number | | Pin Type | Pin Structure | Function description |
|--|------------|------|----------|---------------|--|
| | -JT1 | -SC1 | | | |
| KI6 | 10 | 8 | I | B | |
| KI7 | 11 | 9 | I | B | |
| Timer (T0,T1,T2) | | | | | |
| T0 | 15 | 13 | I | B | T0/T1/T2 external counting clock input |
| T1 | 16 | - | I | B | |
| T2 | 17 | 14 | I | A | |
| T2EX | 14 | 12 | I | B | T2 external capture input |
| Analog comparator (ACMP) | | | | | |
| CPP | 6 | 4 | A | B | Analog comparator positive input |
| CPN0 | 19 | 15 | A | * | Analog comparator negative input |
| CPN1 | 7 | 5 | A | * | Analog comparator negative input |
| CPO | 15 | 13 | O | B | Analog comparator output |
| Carrier Envelope generator (T168) | | | | | |
| ENVO | 17 | 14 | O | A | Carrier Envelope generator output |
| Carrier Timer (CRT) | | | | | |
| REM | 19,7 | 15,5 | O | * | Carrier output |
| Universal Asynchronous Receiver/Transmitte (UART) | | | | | |
| TX | 2 | - | O | B | UART data output |
| RX | 3 | - | I | B | UART data input |

Note: For Pin Type: "P" denotes Power pins, "I/O" denotes normal input/output pins, "I" denotes input pins, "O" denotes output pins; For Pin Structure: "B&" denotes the pad structure is similar to "B" type pad structure, "*" denotes the pad structure is depends on remap pin position

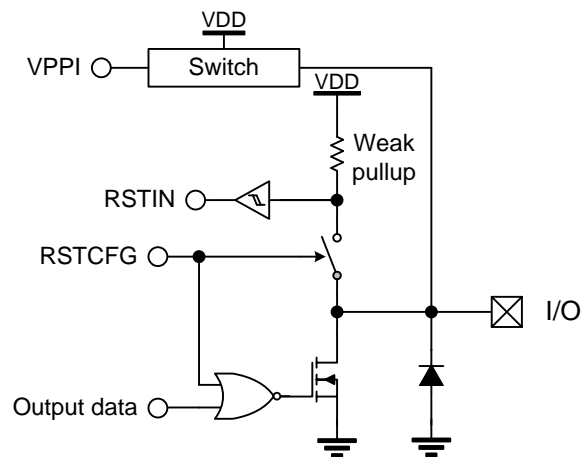
PIN STRUCTURE



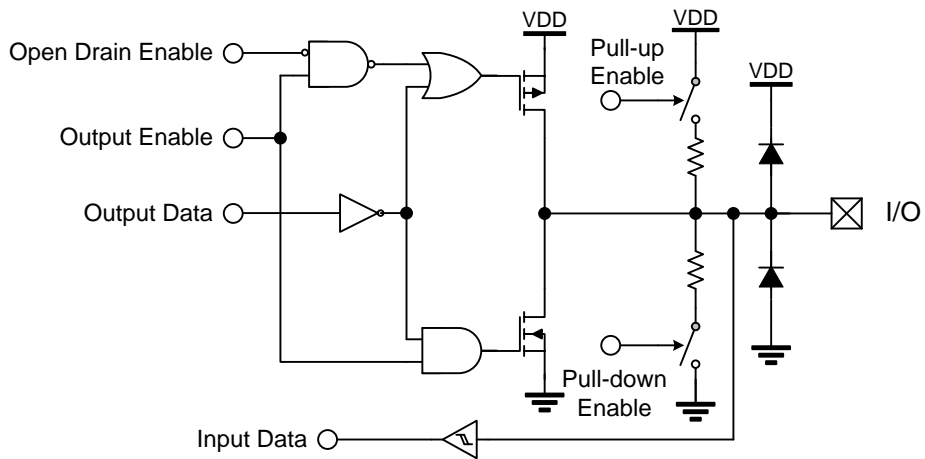
Pin Structure P1



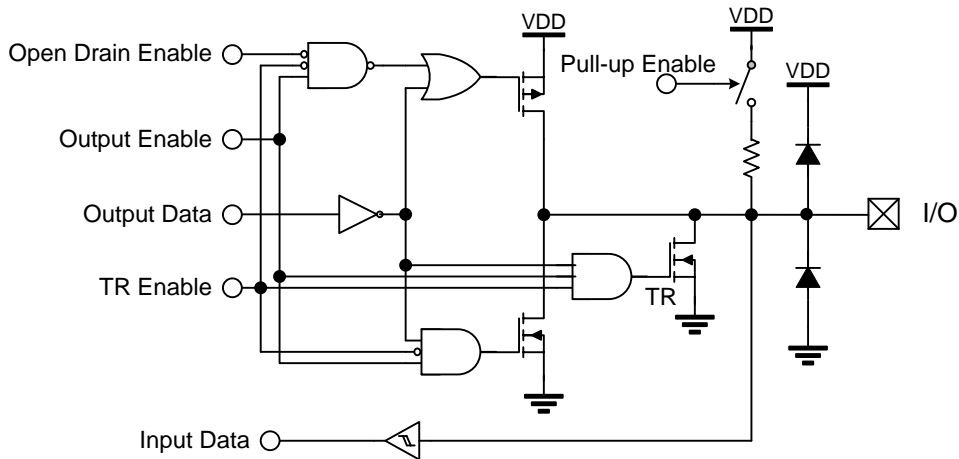
Pin Structure P0



Pin Structure A



Pin Structure B



Pin Structure C

Note: pull-up and pull-down won't be simultaneously enabled by internal logic.

Absolute Maximum Ratings

| Characteristics | Symbol | Range | Unit |
|-----------------------------|-----------|---------------------|------|
| Supply voltage | V_{DD} | -0.3 ~ +5.5 | V |
| Input voltage | V_I | -0.3 ~ $V_{DD}+0.3$ | V |
| Storage temperature Range | T_{STG} | -55 ~ +125 | °C |
| Operating temperature Range | T_{OPR} | -40 ~ +85 | °C |

DC ELECTRICAL CHARACTERISTICS (unless otherwise specified, $V_{DD}=3V$, $T_{AMB}=25^{\circ}C$)

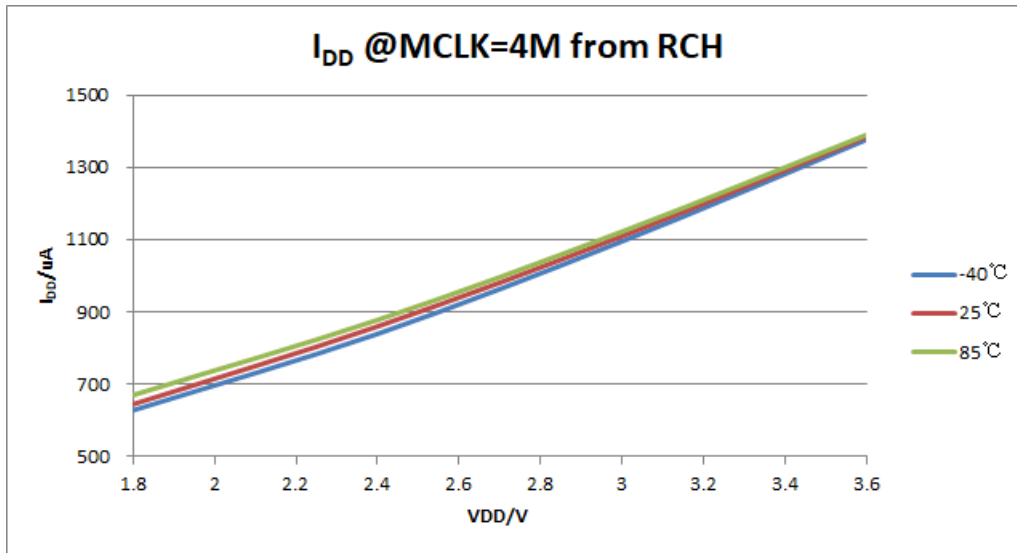
| Characteristics | Symbol | Test condition | | Min | Typ | Max | Unit | |
|---------------------|-----------|--|---|---------------|-----|--------------|------------|-----|
| Operating voltage | V_{DD} | - | | 1.8 | - | 3.6 | V | |
| Operating Current | I_{DD} | Normal Mode | Internal RCH, $F_{MCLK}=4MHz$ | - | 1.1 | 1.5 | mA | |
| | | | Internal RCH, $F_{MCLK}=500KHz$ | - | 0.4 | 0.5 | | |
| | | | External 4MHz Crystal, $F_{MCLK}=4MHz$ | - | 1.5 | 2.2 | | |
| | | IDLE Mode | Internal RCH, $F_{MCLK}=62.5KHz$ | - | 220 | 260 | μA | |
| | | | External 4MHz Crystal, $F_{MCLK}=4MHz$ | - | 750 | 1400 | | |
| | | STOP Mode | With RCL | - | 2 | 3 | μA | |
| Without RCL | - | | 1 | 2 | | | | |
| External Crystal | F_{OSC} | - | | 1 | - | 8 | MHz | |
| Internal RCH | F_{RC} | $V_{DD}=1.8\sim 3.6V$, $T_{AMB}=-10\sim 50^{\circ}C$ | | 3.96 | - | 4.04 | MHz | |
| | | $V_{DD}=1.8\sim 3.6V$, $T_{AMB}=-20\sim 70^{\circ}C$ | | 3.94 | - | 4.06 | | |
| | | $V_{DD}=1.8\sim 3.6V$, $T_{AMB}=-40\sim 85^{\circ}C$ | | 3.90 | - | 4.10 | | |
| Internal RCL | F_{TRC} | $V_{DD}=1.8\sim 3.6V$, $T_{AMB}=-40\sim 85^{\circ}C$ (Typical: $V_{DD}=3V$, $T_{AMB}=25^{\circ}C$) | | 6 | 20 | 40 | KHz | |
| Input high voltage | V_{IH} | P0.5 | | $0.7*V_{DD}$ | - | V_{DD} | V | |
| | | GPIO except for P0.5 | | $0.8*V_{DD}$ | - | V_{DD} | | |
| Input low voltage | V_{IL} | P0.5 | | 0 | - | $0.1*V_{DD}$ | V | |
| | | GPIO except for P0.5 | | 0 | - | $0.2*V_{DD}$ | | |
| Output high current | I_{OH} | $V_{OH}=2.4V$ | P3.0 | - | 15 | - | mA | |
| | | $V_{OH}=2.7V$ | P0[0..4], P0.6/P1/P2 | - | 4 | - | | |
| Output low current | I_{OL} | $V_{OL}=0.3V$ | P0/P1/P2/P3.0 (except P0.5) | - | 10 | - | mA | |
| | | | P0.5 | - | 5 | - | | |
| TR sink current | I_{OL} | $V_{OL}=0.3V$ | low level (TRDS=0) | - | 200 | - | mA | |
| | | | high level (TRDS=1) | - | 250 | - | | |
| Pull-up resistor | R_{PU} | $V_{IN}=0V$ | P0.5 | 100 | 150 | 200 | k Ω | |
| | | | P 3.0 | RPUS[2:0]=000 | 30 | 40 | | 50 |
| | | | | RPUS[2:0]=001 | 40 | 50 | | 60 |
| | | | | RPUS[2:0]=010 | 50 | 60 | | 70 |
| | | | | RPUS[2:0]=011 | 60 | 70 | | 80 |
| | | | | RPUS[2:0]=100 | 70 | 80 | | 90 |
| | | | | RPUS[2:0]=101 | 75 | 90 | | 105 |
| | | | | RPUS[2:0]=110 | 85 | 100 | | 115 |

| Characteristics | Symbol | Test condition | | Min | Typ | Max | Unit |
|-----------------------|------------------|----------------------------------|-------------------------------|------|------|------|------|
| | | | RPUS[2:0]=111 | 95 | 110 | 125 | |
| | | | GPIO except for P0.5 and P3.0 | 100 | 145 | 200 | |
| Pull-down resistor | R _{PD} | V _{IN} =V _{DD} | V _{DD} =1.8~3.6V | 50 | 75 | 100 | kΩ |
| LVR detecting voltage | V _{LVR} | LVRS=0 | | 1.65 | 1.70 | 1.78 | V |
| | | LVRS=1 | | 1.85 | 1.90 | 2.0 | |
| LVR hysteresis | VHYS (LVR) | - | | - | 20 | - | mV |
| Low voltage detect | V _{LVD} | LVDS=0000 | V _{DD} falling | 1.77 | 1.81 | 1.85 | V |
| | | | V _{DD} rising | 1.79 | 1.88 | 1.97 | |
| | | LVDS=0001 | V _{DD} falling | 1.84 | 1.90 | 1.97 | |
| | | | V _{DD} rising | 1.91 | 1.99 | 2.07 | |
| | | LVDS=0010 | V _{DD} falling | 1.95 | 2.01 | 2.08 | |
| | | | V _{DD} rising | 2.00 | 2.09 | 2.17 | |
| | | LVDS=0011 | V _{DD} falling | 2.00 | 2.10 | 2.21 | |
| | | | V _{DD} rising | 2.11 | 2.19 | 2.27 | |
| | | LVDS=0100 | V _{DD} falling | 2.12 | 2.21 | 2.29 | |
| | | | V _{DD} rising | 2.16 | 2.29 | 2.44 | |
| | | LVDS=0101 | V _{DD} falling | 2.23 | 2.30 | 2.39 | |
| | | | V _{DD} rising | 2.33 | 2.40 | 2.49 | |
| | | LVDS=0110 | V _{DD} falling | 2.32 | 2.40 | 2.50 | |
| | | | V _{DD} rising | 2.38 | 2.50 | 2.63 | |
| | | LVDS=0111 | V _{DD} falling | 2.39 | 2.50 | 2.62 | |
| | | | V _{DD} rising | 2.50 | 2.60 | 2.70 | |
| | | LVDS=1000 | V _{DD} falling | 2.49 | 2.60 | 2.73 | |
| | | | V _{DD} rising | 2.57 | 2.70 | 2.84 | |
| | | LVDS=1001 | V _{DD} falling | 2.58 | 2.70 | 2.84 | |
| | | | V _{DD} rising | 2.67 | 2.80 | 2.93 | |
| | | LVDS=1010 | V _{DD} falling | 2.70 | 2.80 | 2.90 | |
| | | | V _{DD} rising | 2.78 | 2.90 | 3.05 | |
| | | LVDS=1011 | V _{DD} falling | 2.79 | 2.90 | 3.04 | |
| | | | V _{DD} rising | 2.88 | 3.00 | 3.15 | |
| | | LVDS=1100 | V _{DD} falling | 2.85 | 2.99 | 3.13 | |
| | | | V _{DD} rising | 2.96 | 3.10 | 3.26 | |
| | | LVDS=1101 | V _{DD} falling | 2.96 | 3.08 | 3.23 | |
| | | | V _{DD} rising | 3.06 | 3.20 | 3.35 | |
| | | LVDS=1110 | V _{DD} falling | 3.04 | 3.17 | 3.32 | |
| | | | V _{DD} rising | 3.15 | 3.29 | 3.44 | |

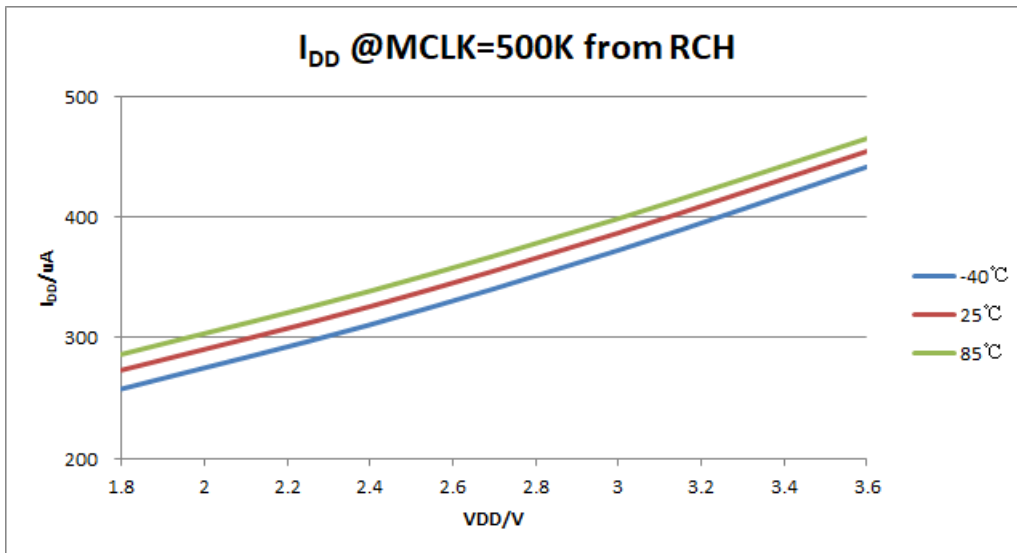
| Characteristics | Symbol | Test condition | Min | Typ | Max | Unit | |
|-----------------|--------|----------------|-------------------------|------|------|------|--|
| | | LVDS=1111 | V _{DD} falling | 3.14 | 3.27 | 3.43 | |
| | | | V _{DD} rising | 3.26 | 3.39 | 3.54 | |

Note: the type vale is characteristic result, not test in production.

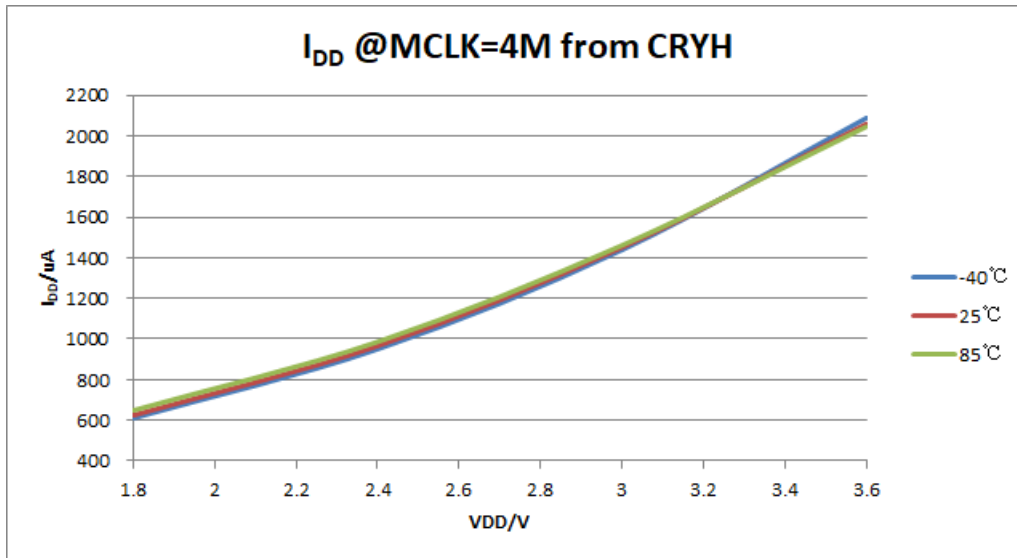
DC and AC characteristics figure



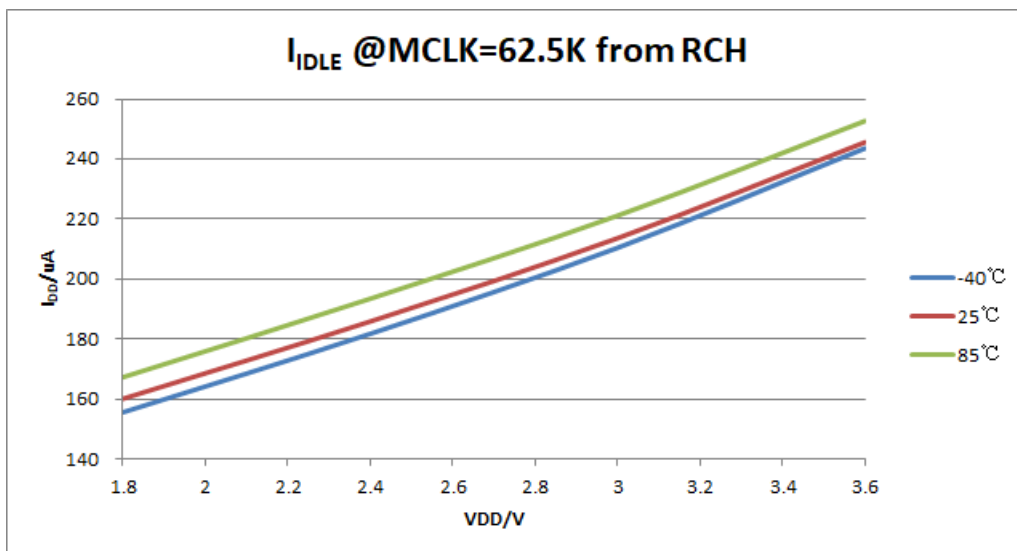
I_{DD} @MCLK=4MHz, from RCH



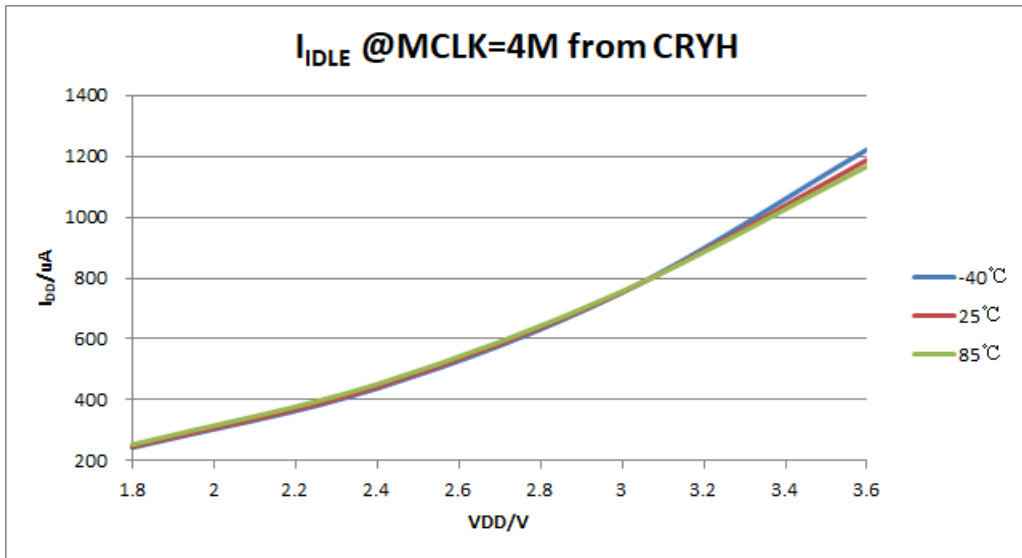
I_{DD} @MCLK=500KHz, from RCH



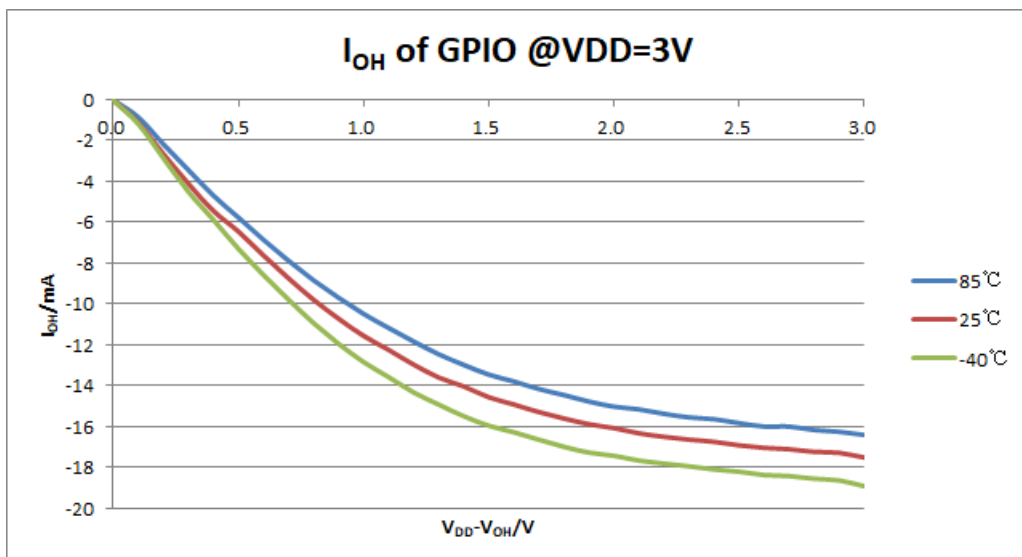
I_{DD} @MCLK=4MHz, from CRYH



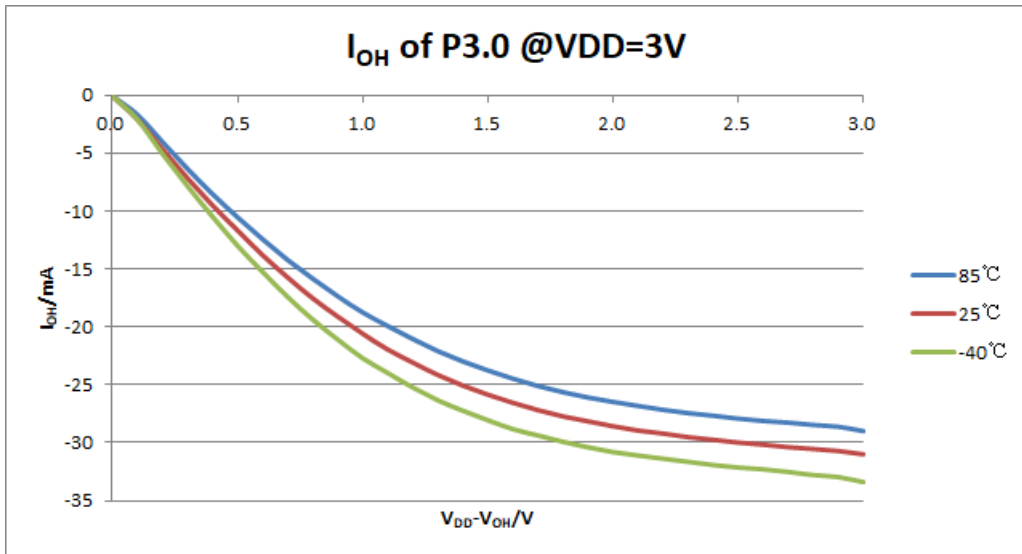
I_{IDLE} @MCLK=62.5KHz, from RCH



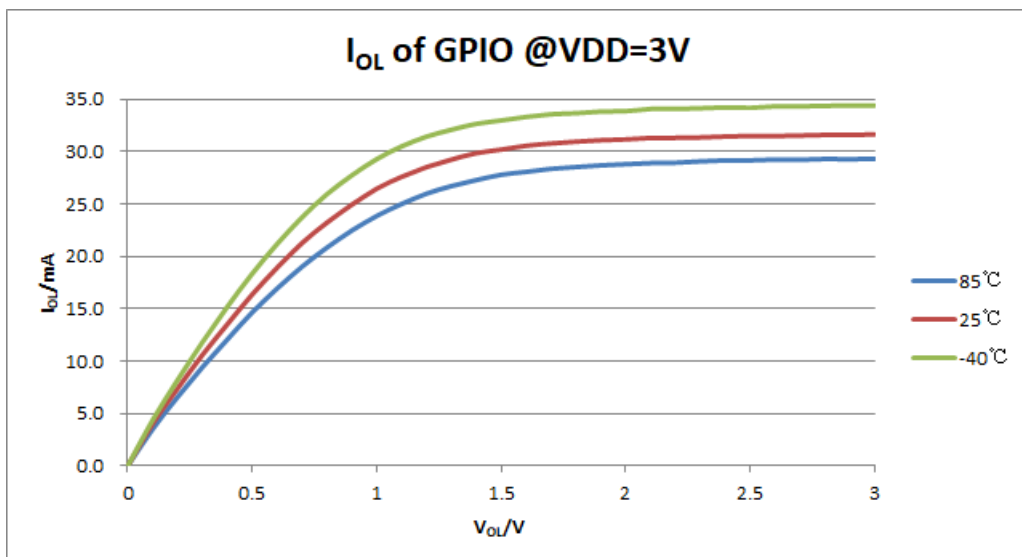
I_{IDLE} @MCLK=4MHz, from CRYH



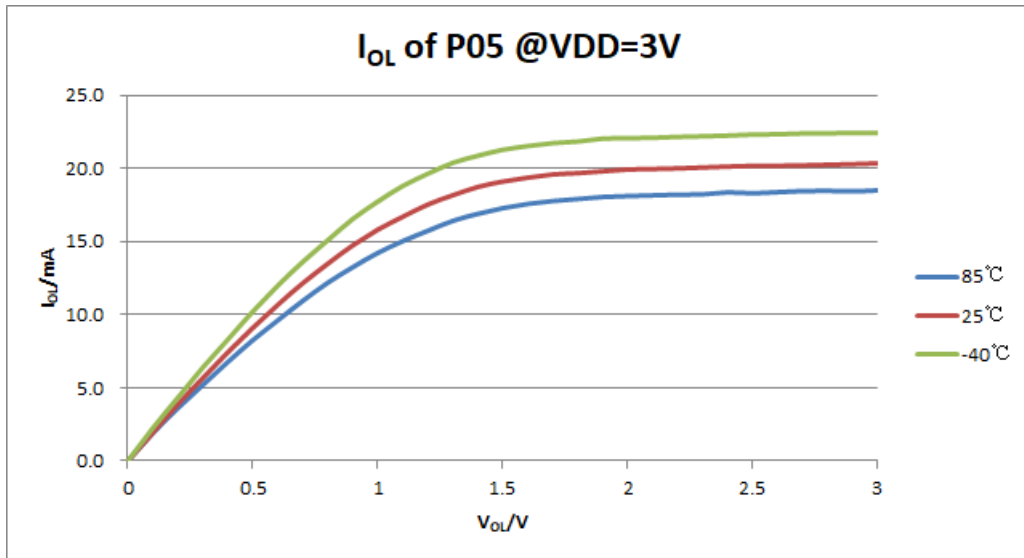
Source current of GPIO



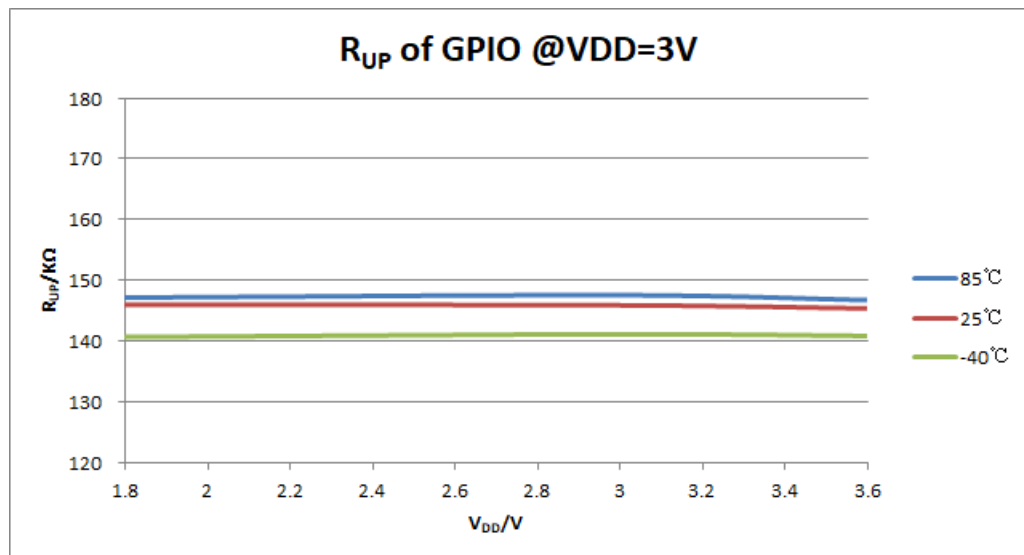
Source current of REM/P3.0



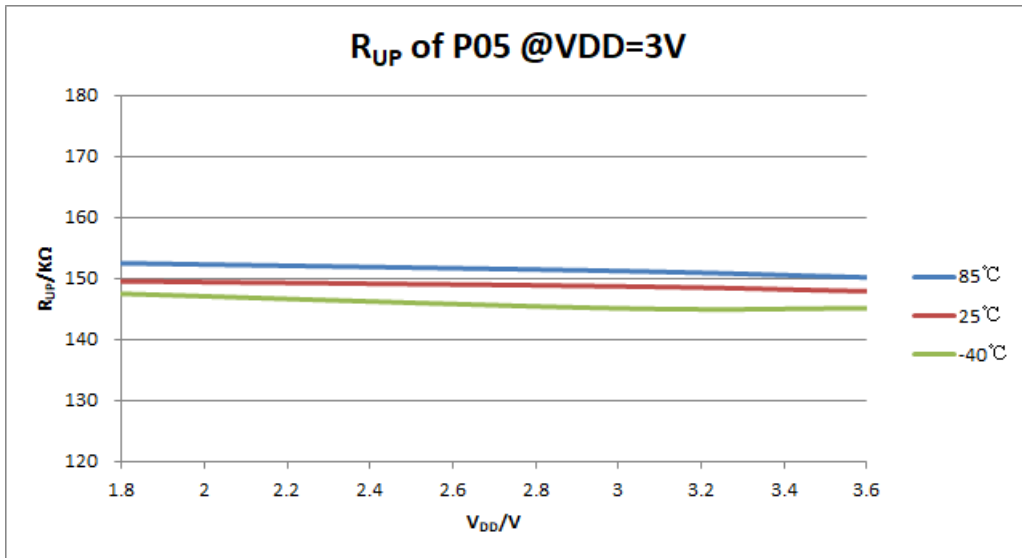
Sink current of GPIO



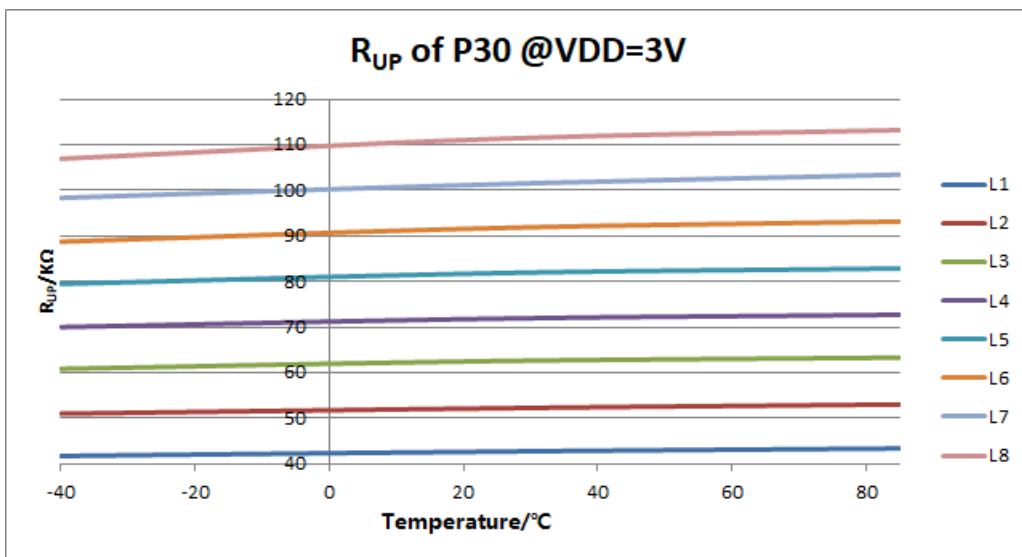
Sink current of nRST/P0.5



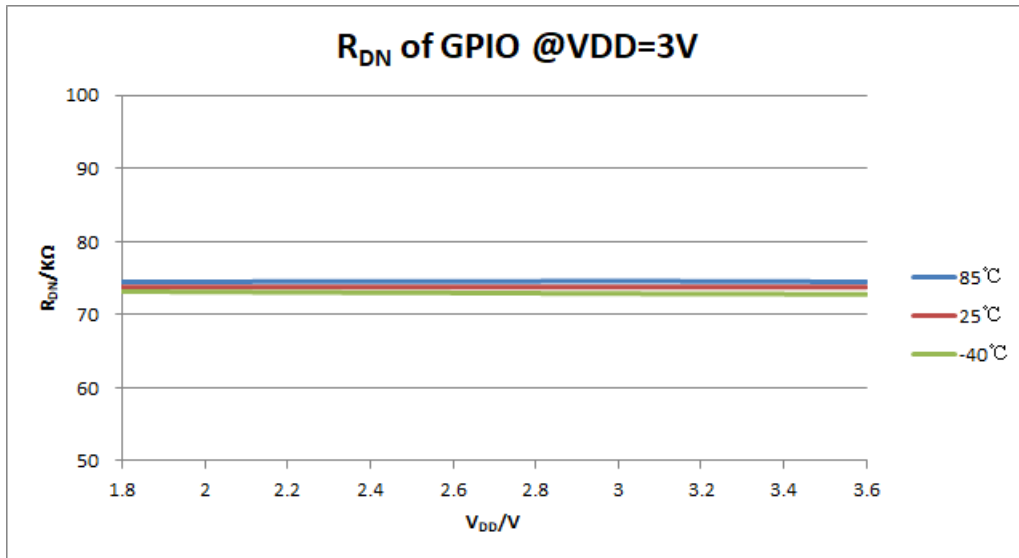
Pull-up resistor of GPIO



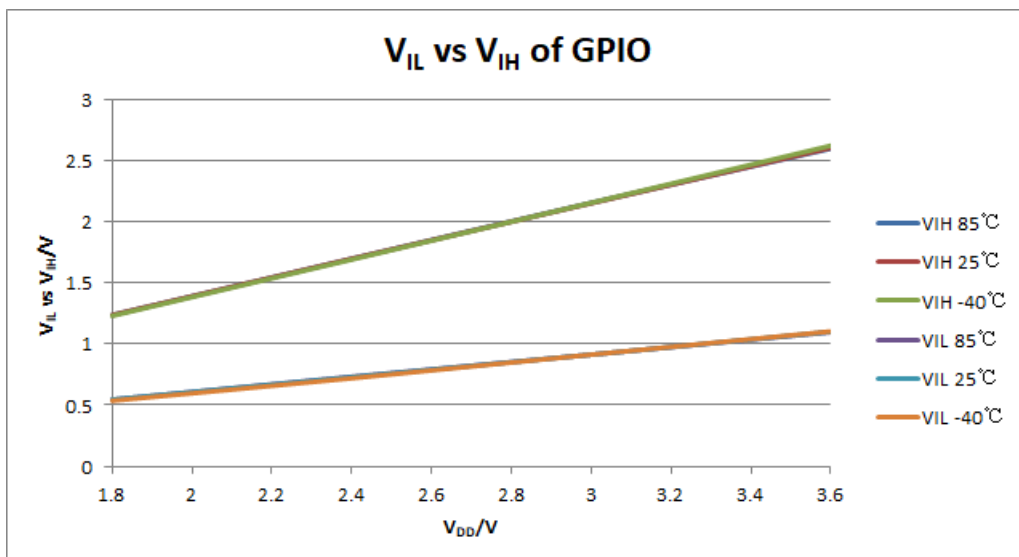
Pull-up resistor of nRST/P0.5



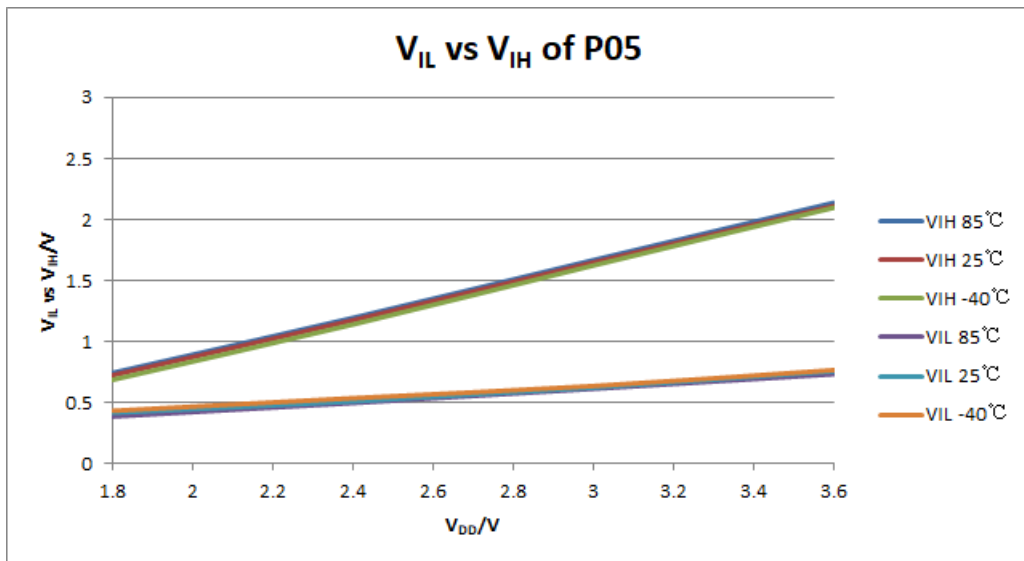
Pull-up resistor of REM/P3.0



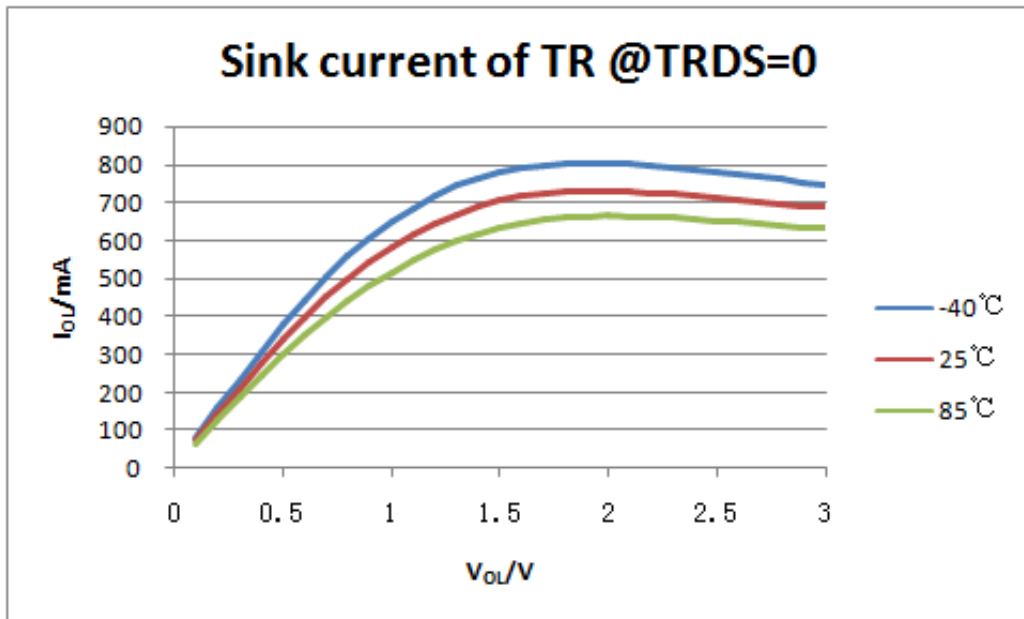
Pull-down resistor of GPIO



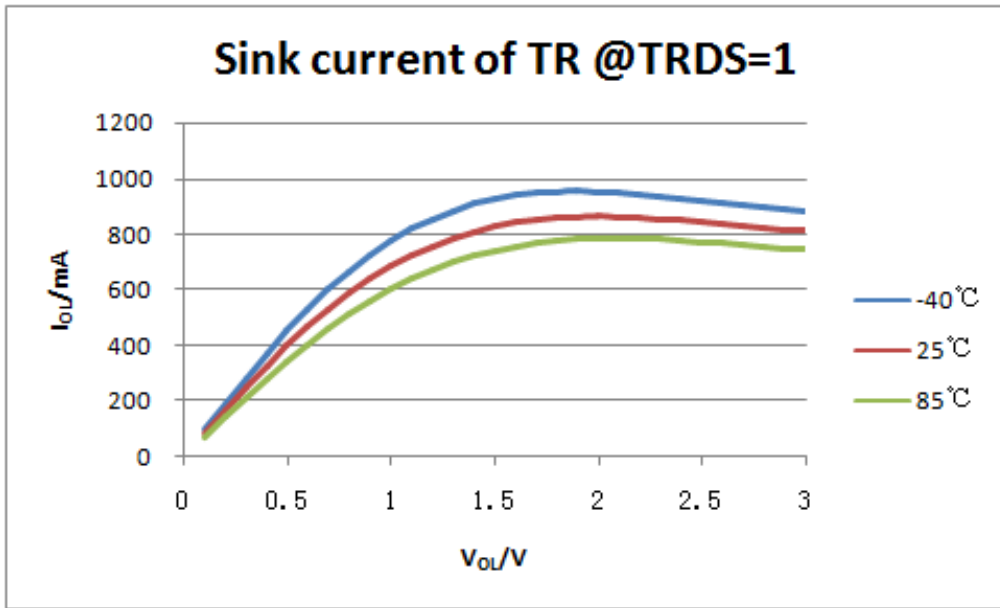
V_{IL} vs V_{IH} of GPIO



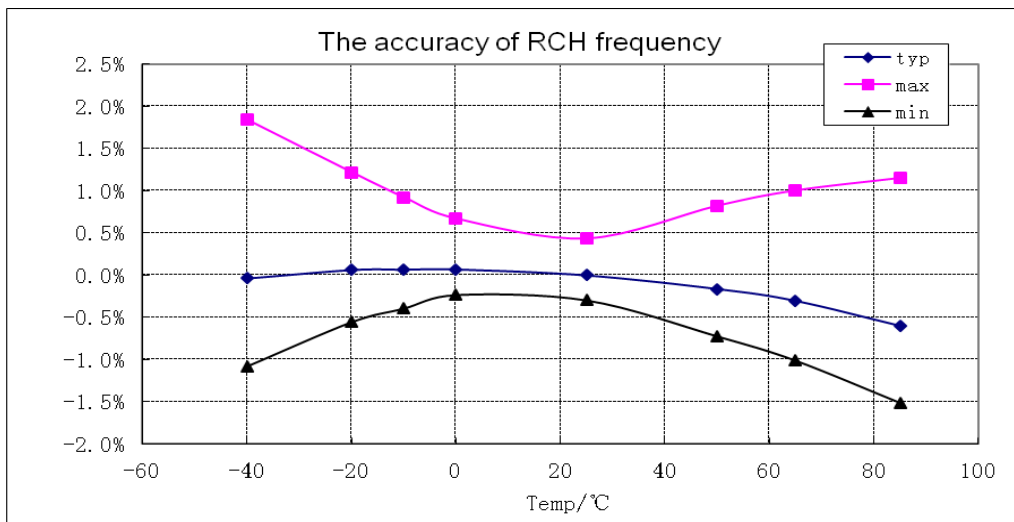
V_{IL} vs V_{IH} of nRST/P0.5



Sink current of TR low level



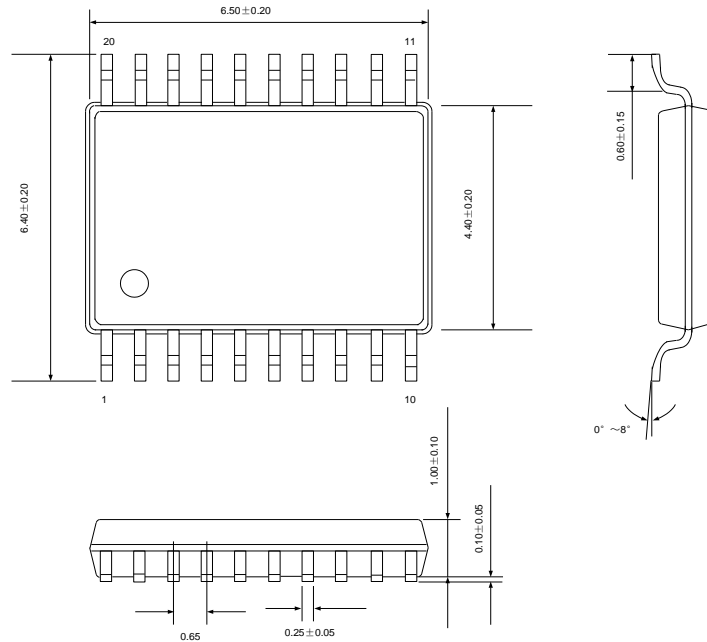
Sink current of TR high level



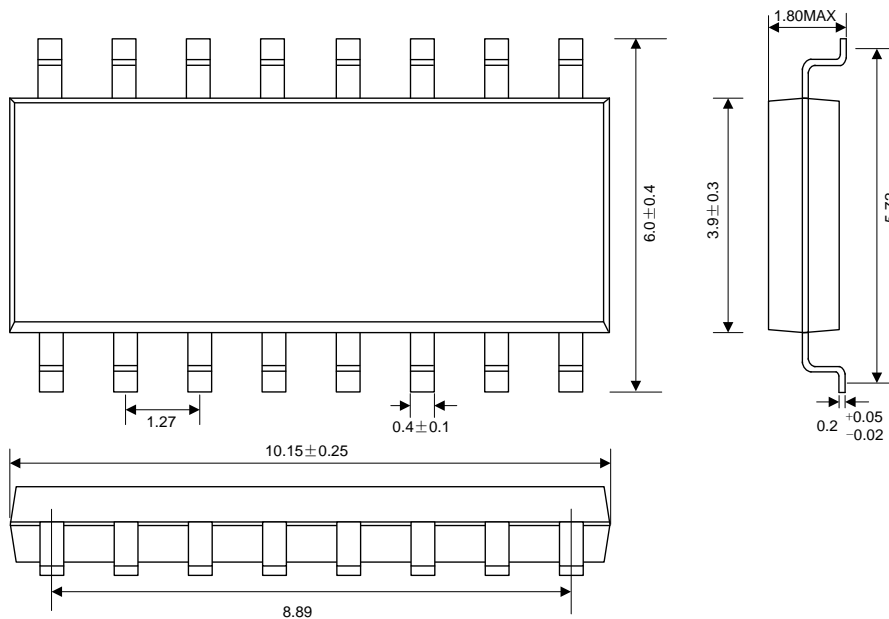
The accuracy of RCH frequency

PACKAGE OUTLINE

TSSOP-20-225-0.65 **UNIT: mm**



SOP-16-225-1.27 **UNIT: mm**





MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Disclaimer :

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without prior notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!

Part No.: SC51P2320 Document Type: Datasheet
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Rev.: 1.2

Revision History:

1. Modify the DC ELECTRICAL CHARACTERISTICS of P3.0
-

Rev.: 1.1

Revision History:

1. Modify pin structure
-

Rev.: 1.0

Revision History:

1. First release
-