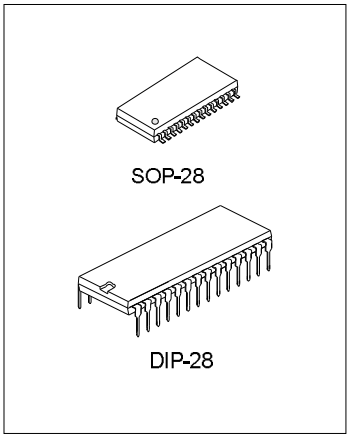
4-CH STEREO AUDIO PROCESSOR

DESCRIPTION

The SC5313 is a digital controlled stereo audio processor with loudness and tone, built-in volume, treble/bass tone, left/right balance and loudness. Selectable input gain and external loudness function are provided. Control is accomplished by serial bus microprocessor interface.

The AC signal settings is obtained by resistor networks and switches combined with operational amplifiers.



FEATURES

* All functions programmable via serial Bus
* 4 independent speakers control, Independent mute function
* 3 stereo inputs
* Volume control in 1.25dB steps
* Treble and bass control
* Loudness function

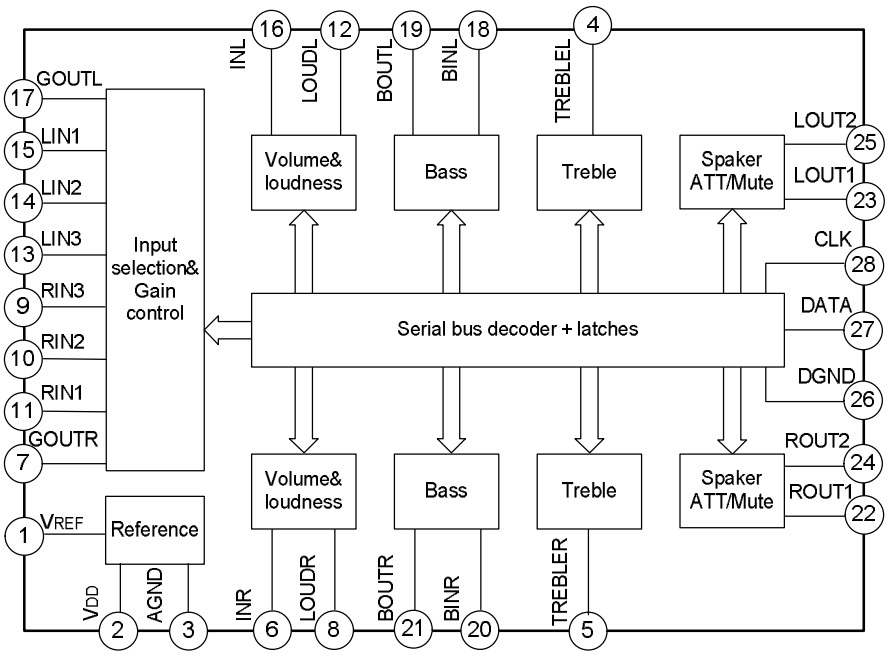
ORDERING INFORMATION

Device	Package
SC5313	DIP-28-600-2.54
SC5313S	SOP-28-375-1.27

APPLICATIONS

* Car audio
* CD
* Hi-Fi audio system

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Ratings	Unit
Supply Voltage	V_S	10.2	V
Operating Temperature	T_{opr}	-40 ~ +85	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_{amb}=25°C,V_S=9.0V,R_L=10kΩ, R_G=600Ω, all controls flat(G=0), f=1kHz, unless otherwise specified)

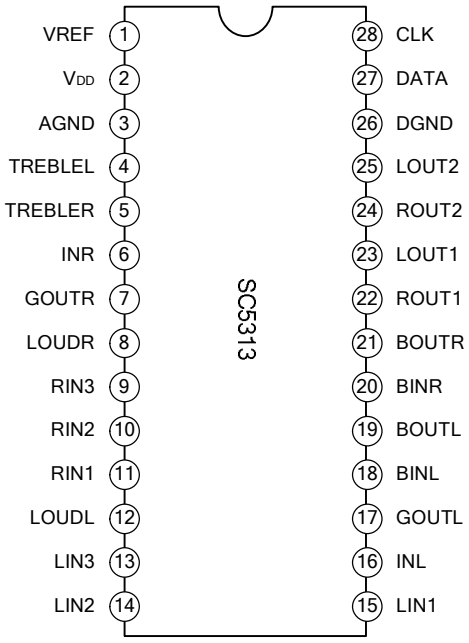
Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
Operating Supply Voltage	V_S		6	9	10.0	V
Operating Supply Current	I_S			20.0	35.0	mA
Ripple Rejection Of Supply Voltage	SVR		60	80		dB
INPUTS SELECTORS						
Input Resistance	R_{II}	Input 1, 2, 3	35	50	70	kΩ
Clipping Level	V_{CL}		2	2.5		Vrms
Input Separation	SIN		80	100		dB
Output Load Resistance	R_L	Pin7,17	4			kΩ
Minimum Input Gain	GIN(MIN)		-1	0	1	dB
Maximum Input Gain	GIN(MAX)			11.25		dB
Step Resolution	GSTEP			3.75		dB
VOLUME CONTROL						
Input Resistance	RIV		20	33	50	kΩ
Control Range	Crange		70	75	80	dB
Minimum Attenuation	AV(min)		-1	0	1	dB
Maximum Attenuation	AV(max)		70	75	80	dB
Step Resolution	ASTEP		0.5	1.25	1.75	dB
SPEAKER ATTENUATORS						
Control Range	Crange		35	37.5	40	dB
Step Resolution	SSTEP		0.5	1.25	1.75	dB
Output Mute Attenuation	AMUTE		80	100		dB
BASS CONTROL						
Control Range	GB	Maximum boost/cut	±12	±14	±16	dB
Step Resolution	BSTEP		1	2	3	dB
Internal Feedback Resistance	RB		34	44	58	kΩ
TREBLE CONTROL						
Control Range	Gt	Maximum boost/cut	±13	±14	±15	dB
Step Resolution	TSTEP		1	2	3	dB

(To be continued)

(Continued)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
AUDIO OUTPUTS						
Clipping Level	V_{OCL}	THD=0.3%	2	2.5		Vrms
Output Load Resistance	R_L		4			kΩ
Output Load Capacitance	C_L				10	nF
Output Resistance	R_{OUT}		30	75	120	Ω
DC Voltage Level	V_{OUT}		4.2	4.5	4.8	V
GENERAL						
Signal To Nnoise Ratio	S/N	All gains=0dB; V_O=1Vrms		106		dB
Distortion	THD	Av=0,V_{IN}=10mV		0.01	0.1	%
		Av=-20dB, V_{IN}=1Vrms		0.09	0.3	%
		Av=-20dB,V_{IN}=0.3Vrms		0.04		%
Channel Separation Left/Right	S_C		80	103		dB
BUS INPUTS						
Input Low Voltage	V_{IL}				1	V
Input High Voltage	V_{IH}		3			V
Input Current	I_{IN}		-5		+5	μA
Output Voltage DATA Acknowledge	V_O	I_O=1.6mA			0.4	V

PIN CONFIGURATIONS



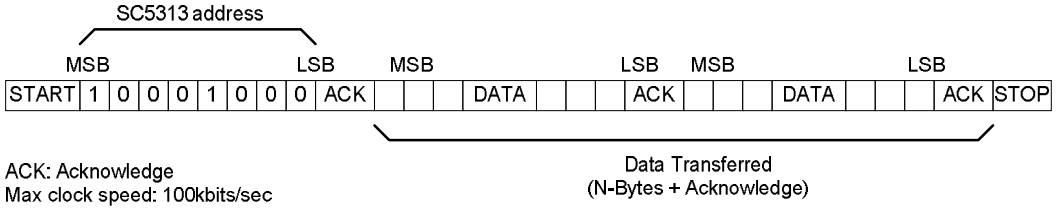
PIN DESCRIPTION

Pin No.	Symbol	Description
1	VREF	Reference voltage
2	VDD	Power supply.
3	AGND	Analog ground
4	TREBLEL	Treble control (L)
5	TREBLER	Treble control (R)
6	INR	Volume control input (R)
7	GOUTR	Input selection and gain control output (R)
8	LOUDR	Loudness control (R)
9	RIN3	Right channel input 3
10	RIN2	Right channel input 2
11	RIN1	Right channel input 1
12	LOUDL	Loudness control (L)
13	LIN3	Left channel input 3
14	LIN2	Left channel input 2
15	LIN1	Left channel input 1
16	INL	Volume control input (L)
17	GOUTL	Input selection and gain control output (L)
18	BINL	Bass control input (L)
19	BOUTL	Bass control output (L)
20	BINR	Bass control input (R)
21	BOUTR	Bass control output (R)
22	ROUT1	Right channel output1
23	LOUT1	Left channel output1
24	ROUT2	Right channel output2
25	LOUT2	Left channel output2
26	DGND	Digital ground
27	DATA	Control data input
28	CLK	Control clock input

BUS INTERFACE PROTOCOL

1. The interface protocol comprises:

* A start conditions
* Address code,
* Data code (N-bytes + acknowledge)
* A stop condition

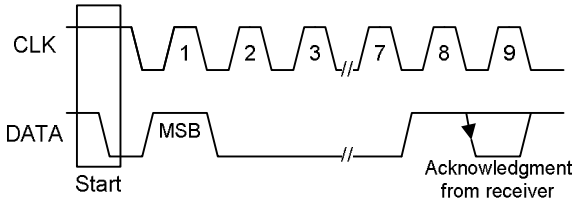


2. A start condition is a HIGH to LOW transition of the DATA line while CLK is HIGH.

The stop condition is a LOW to HIGH transition of the DATA line while CLK is HIGH.

3. The microprocessor puts a resistive HIGH level on the DATA line during the acknowledge clock pulse.

The SC5313 that acknowledges has to pull-down the DATA line during the acknowledge clock pulse, so that the DATA line is stable LOW during this clock pulse. The SC5313 which has been addressed has to generate an acknowledge after the reception of each byte , otherwise the DATA line remain at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.



4. Chips address

1 (MSB)	0	0	0	1	0	0	0 (LSB)

5. Data bytes

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	0	0	B1	B0	A2	A1	A0	Left channel output2 control
1	0	1	B1	B0	A2	A1	A0	Right channel output2 control
1	1	0	B1	B0	A2	A1	A0	Left channel output1control
1	1	1	B1	B0	A2	A1	A0	Right channel output1 control
0	1	0	G1	G0	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

Note: A=1.25dB steps=10dB steps=2dB steps=3.75dB steps

DETAILED DESCRIPTION OF DATA BYTES

1. Volume

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

For example, a volume of –56.25dB is given by: 00101101

2. Speaker attenuators

MSB							LSB	Function
1	0	0	B1	B0	A2	A1	A0	Left channel output2 control
1	0	1	B1	B0	A2	A1	A0	Right channel output2 control
1	1	0	B1	B0	A2	A1	A0	Left channel output1 control
1	1	1	B1	B0	A2	A1	A0	Right channel output1 control
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	MUTE

For example, attenuation of 27.5dB on Left channel output1 is given by: 11010110

3. Audio switch

MSB							LSB	Function
0	1	0	G1	G0	S2	S1	S0	Audio switch
						0	0	Stereo 1
						0	1	Stereo 2
						1	0	Stereo 3
						1	1	--
					0			Loudness ON
					1			Loudness OFF
			0	0				+11.25dB
			0	1				+7.5dB
			1	0				+3.75dB
			1	1				0dB

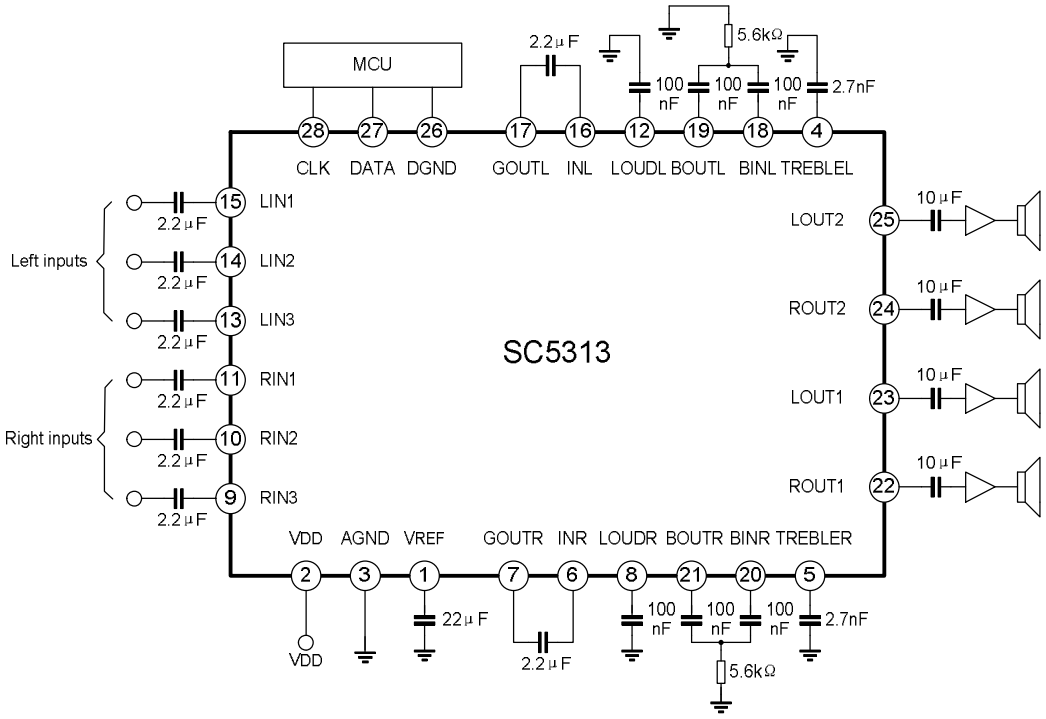
For example, to select the stereo 3 input with a gain of +3.75dB Loudness ON the 8bit string is: 01010010

4. Bass and treble

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

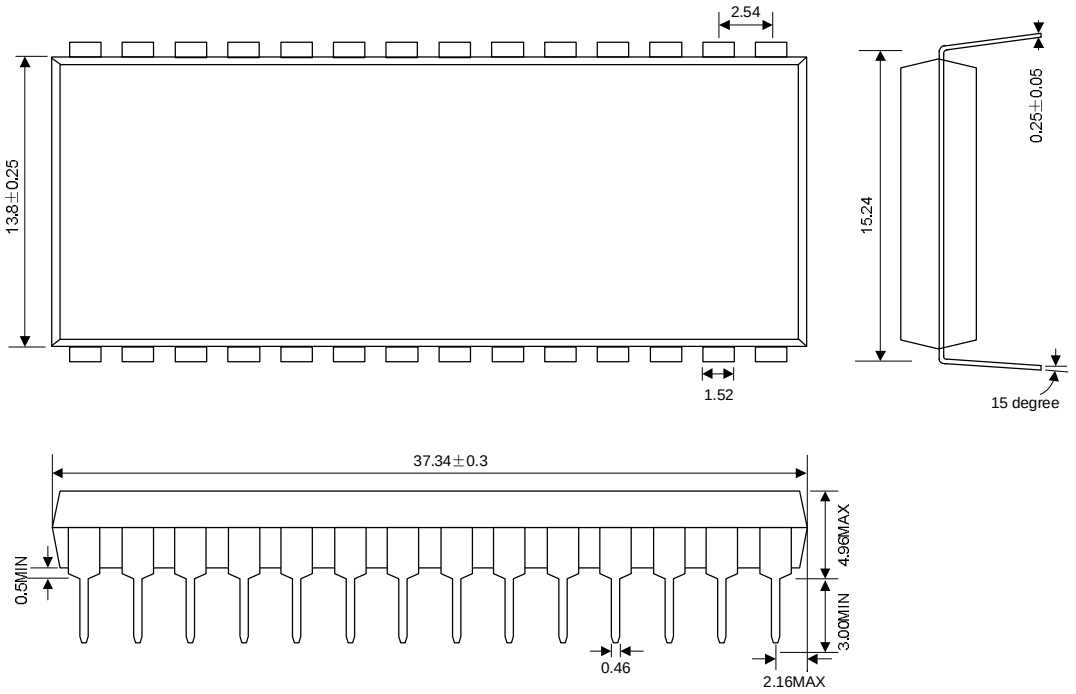
C3=Sign; For Example, treble at –8dB is obtained by the following 8bit string is: 01110011.

TYPICAL APPLICATION CIRCUIT

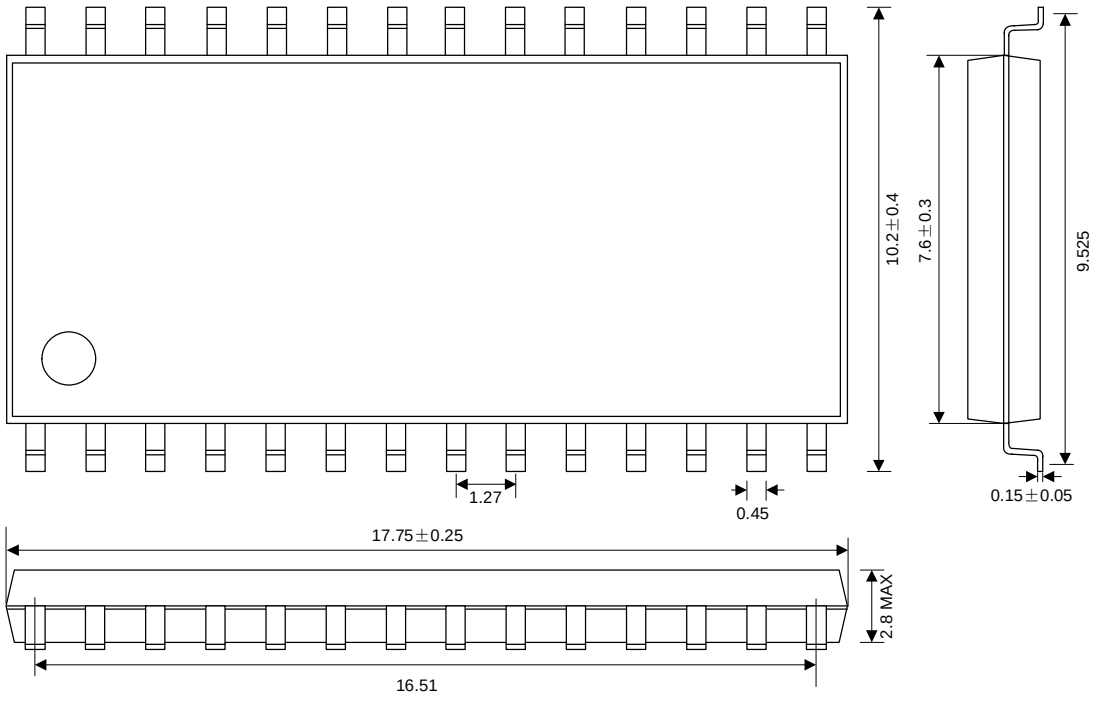


PACKAGE OUTLINE

DIP-28-600-2.54 UNIT: mm



SOP-28-375-1.27 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.