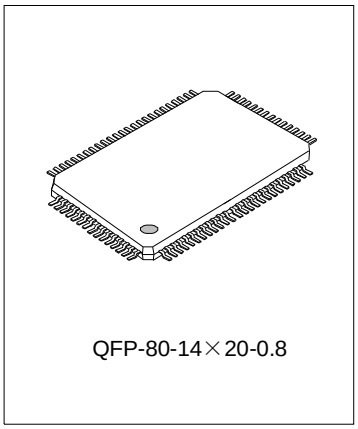
AUDIO CONTROL SYSTEM WITH BUILT-IN 4-BIT MCU

DESCRIPTION

The SC63C0316 single-chip CMOS microcontroller is designed for very high performance. With an up-to-14-digit LCD direct drive capability, 4-channel A/D converter, 8-bit timer/counter, PLL frequency synthesizer. The SC63C0316 offers you an excellent design solution for a wide variety of applications, especially those requiring DTS support.

Up to 56 pins of the 80-pin QFP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the SC63C0316's advanced CMOS technology ensures low power consumption and a wide operating voltage range.



QFP-80-14×20-0.8

FEATURES

Memory

* 512-nibble RAM
* 16K-byte ROM

I/O Pins

* Input only: 4 pins
* Output only: 28 pins
* I/O: 24 pins

LCD Controller/Driver

* Maximum 14-digit LCD direct drive capability
* 28 segment x 4 common signals
* Display modes: Static, 1/2 duty (1/2 bias)
  1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

8-Bit Basic Timer

* Programmable interval timer functions
* Watch-dog timer function

8-Bit Timer/Counter

* Programmable 8-bit timer
* External event counter
* Arbitrary clock frequency output
* External clock signal divider
* Serial I/O interface clock generator

8-Bit Serial I/O Interface

* 8-bit transmit/receive mode
* 8-bit receive mode
* Data direction selectable (LSB-first or MSB-first)
* Internal or external clock source

ORDERING INFORMATION

Device	Package
SC63C0316	QFP-80-14 x 20-0.8

A/D Converter

* 4-channels with 8-bit resolution

Bit Sequential Carrier Buffer

* Support 16-bit serial data transfer in arbitrary format

PLL Frequency Synthesizer

* Level = 300 mVp-p (min)
* AMVCO range = 0.5 MHz to 30 MHz
* FMVCO range = 30 MHz to 150 MHz

16-Bit Intermediate Frequency (IF) Counter

* Level = 300 mVp-p (min)
* AMIF range = 100 kHz to 1 MHz
* FMIF range =5MHz to 15 MHz

Watch Timer

* Time interval generation
  0.5 s, 3.9 ms at 32.768 kHz
* Frequency outputs to BUZ pin
* Clock source generation for LCD

Interrupts

* Four internal vectored interrupts
* Four external vectored interrupts
* Two quasi-interrupts

Memory-Mapped I/O Structure

* Data memory bank 15

Three Power-Down Modes

* Idle: Only CPU clock stops
* Stop1: Main system or subsystem clock stops
* Stop2: Main system and subsystem clock stop
* CE low: PLL and IFC stop

Oscillation Sources

* Crystal or ceramic oscillator for main system clock
* Crystal for subsystem clock
* Main system clock frequency: 4.5 MHz (Typ)
* Subsystem clock frequency: 32.768 kHz (Typ)
* CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

* 0.9, 1.8, 14.2 µs at 4.5 MHz
* 122 µs at 32.768 kHz (subsystem)

Operating Temperature

* – 40 °C to 85 °C

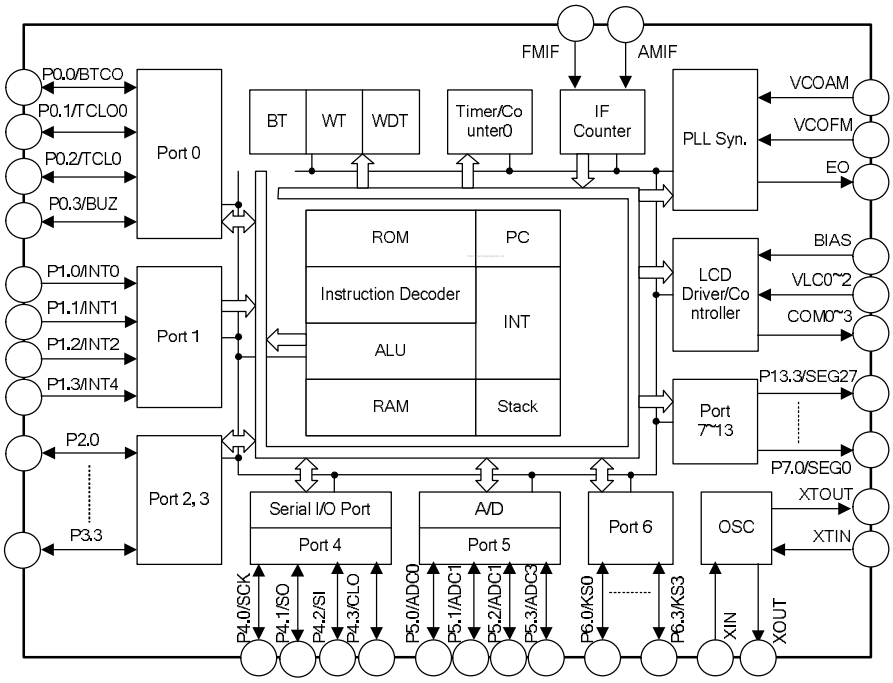
Operating Voltage Range

* 1.8 V to 5.5 V at 3MHz
* PLL/IFC operation: 2.5V to 3.5V or 4.0V to 5.5V

APPLICATIONS

* Auto audio system
* Other audio system

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Tamb=25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 - 6.5	V
Input Voltage	V_{I1}	-0.3 - V_{DD} +0.3	V
	V_{I2}	-0.3 - V_{DD} +0.3	
Output Voltage	V_O	-0.3 - V_{DD} +0.3	V
Output Current High	I_{OH}	-15	mA
		-30	

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Characteristics	Symbol	Value	Unit
Output Current Low	IOL	+30（Peak value）	mA
		+100（Peak value）	
Operating Temperature	Tamb	-40 ~ 85	°C
Storage Temperature	Tstg	-65~150	°C

DC CHARACTERISTICS (Tamb=-40°C to +85°C, VDD=3.5V to 6.0V)

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input High Voltage	VIH1	All input pins except those specified below for VIH2-VIH4	0.7VDD	---	VDD	V
	VIH2	Port 0, 1, 6, 7, and $\overline{\text{RESET}}$	0.8VDD		VDD	
	VIH3	Ports 4, 5, 7 and 8 with pull-up resistors assigned	0.7VDD		VDD	
		Ports 4, 5, 7 and 8 are open-drain	0.7VDD		9	
	VIH4	Xin, Xout and Xtin	VDD -0.5		VDD	
Input Low Voltage	VIL1	All input pins except those specified below for CIL2-Vil3	---	---	0.3VDD	V
	VIL2	Ports 0, 1, 6, 7, 9, 10 and $\overline{\text{RESET}}$			0.2VDD	
	VIL3	Xin, Xout and XTin			0.4	
Output High Voltage	VOH1	VDD=4.5V to 6.0V, IOH=-1mA, Ports 0, 2-10	VDD -1.0	---	---	V
		IOH=-100μA	VDD -0.5			
	VOH2	VDD=4.5V to 6.0V, IOH=-100μA, Ports 11-13 only	VDD -2.0			
		IOH=-30μA	VDD -1.0			
Output Low Voltage	VOL1	VDD=4.5V to 6.0V, IOL=1.6mA, Ports 4,5,7 and 8only	---	0.8	2	V
		IOL=-1.6mA, Ports 0,2,3,6,9,10, EO1, and Eo2 only		---	0.4	
		IOL=400μA, Ports 0, 2, 3, 6, 9, 10, EO1 and EO2 only			0.2	
	VOL2	VDD=4.5V to 6.0V, IOL=100μA, Port 11, 12 and 13 only			1	
		IOL=50μA			1	
Input High Leakage Current	ILIH1	VI=VDD, all input pins except $\overline{\text{RESET}}$ and those specified below for ILIH2-ILIH3	---	---	3	μA

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Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input High Leakage Current	I_{LIH2}	$V_I=V_{DD}$, Xin, Xout, Xtin only			25	μA
	I_{LIH3}	V_I=9V, Ports 4,5,7 and 8 are open-drain			20	μA
Input Low Leakage Current	I_{LIL1}	V_I=0V, all input pins except Xin, Xout, XTin and $\overline{RESET}$	---	---	-3	μA
	I_{LIL2}	V_I=0V, Xin, Xout, and XTin only			-20	
Output High Leakage Current	I_{LOH1}	$V_O=V_{DD}$, all output pins except for ports 4, 5, 7 and 8	---	---	3	μA
	I_{LOH2}	V_O=9V, Ports 4, 5, 7 and 8 are open-drain			20	
Output Low Leakage Current	I_{LOL}	V_O=0V	---	---	3	μA
Pull-up Resistor	R_{L1}	V_I=0V; V_{DD}=5V±10%, Port 0-3, 6, 9, and 10 (except P1.3)	15	46	80	kΩ
		V_{DD}=3V±10%,	30	90	200	
	R_{L2}	$V_O=V_{DD}$-2V, V_{DD}=5V±10%, Ports 4, 5, 7 and 8 only	15	40	70	
		V_{DD}=3V±10%,	10		60	
	R_{L3}	V_I=0V; V_{DD}=5V±10%, $\overline{RESET}$	100	230	400	
		V_{DD}=3V±10%,	200	490	800	
LCD Drive Voltage	V_{LCD}	--	2.5		VDD	V
LCD Voltage Dividing Resistor	R_{LCD}	--	50	100	140	kΩ
COM Output Impedance	R_{COM}	V_{DD}=5V±10%,	---	3	6	kΩ
		V_{DD}=3V±10%,		10	15	
SEG Output Impedance	R_{SEG}	V_{DD}=5V±10%,	---	3	20	kΩ
		V_{DD}=3V±10%,		10	60	
Supply Current (1)	I_{DD1} (2)	V_{DD}=5V±10%,(3), 4.5MHz crystal oscillator, C1=C2=22pF, CE high; PLL operates	---	12	25	mA
	I_{DD2}	Idle mode; V_{DD}=5V±10%, 4.5MHz crystal oscillator, CPU clock =fxx/4, CE low; PLL stops.		1.4	1.8	
		V_{DD}=3V±10%, CPU clock =fxx/64		0.23	1.0	
	I_{DD3} (4)	V_{DD}=3V±10%, 32kHz crystal oscillator, CE low; PLL stops.	---	25	120	μA
	I_{DD4} (5)	Idle mode; V_{DD}=3V±10%, 32kHz crystal oscillator.		20	30	

DC CHARACTERISTICS (concluded) (T_{amb}=-40°C to +85°C, V_{DD}=2.7V to 6.0V)

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Supply Current (cont)	I_{DD5}	Stop 1 mode; XTin=0V V_{DD}=5V±10%, CPU clock=fxx/4, CE low; PLL stops	---	0.6	5	µA
		V_{DD}=3V±10%, CPU clock=fxx/64		0.2	3	
	I_{DD6}	V_{DD}=5V±10%, 4.5MHz crystal oscillator, CPU clock=fxx/4, CE low; PLL stops		4.2	8	mA
		V_{DD}=3V±10%, CPU clock=fxx/64		0.7	1.2	
	I_{DD7} (2)	Stop 2 mode; Xtin=0V, V_{DD}=5V±10%, CPU clock=fxx/4, CE low; PLL stops		0.12	2.0	µA

NOTES:

1. Currents in the following circuits are not included; on-chip pull-up resistors, output port drive currents, internal LCD voltage dividing resistors and A/D converter.
2. IDD1 and IDD7 are guaranteed in T_{amb} = – 20 °C to + 85 °C
3. Data includes power consumption for subsystem clock oscillation.
4. For high-speed controller operation, the power control register (PCON) must be set to 0011B.
5. For low-speed controller operation, the power control register (PCON) must be set to 0000B.
6. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.

MAIN SYSTEM OSCILLATOR CHARACTERISTICS (T_{amb}=-40°C to +85°C, V_{DD}=2.7V to 6.0V)

Oscillator	Characteristics	Test condition	Min	Typ	Max	Units
Ceramic Oscillator	Oscillation frequency (1)	--	0.4	--	5.0	MHz
	Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the mini mum oscillator voltage range	--	--	4	ms
Crystal Oscillator	Oscillation frequency (1)	--	0.4	4.5	6.0	MHz
	Stabilization (2)	V_{DD}=4.5V~6.0V	--	--	10	ms
		V_{DD}=2.7V~4.5V	--	--	30	
External Clock	XIN input frequency (1)	--	0.4	--	4.5	MHz
	XIN input high and low level width	--	111	--	1250	ns

NOTES:

1. Oscillation frequency and Xin input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when Stop mode is terminated.

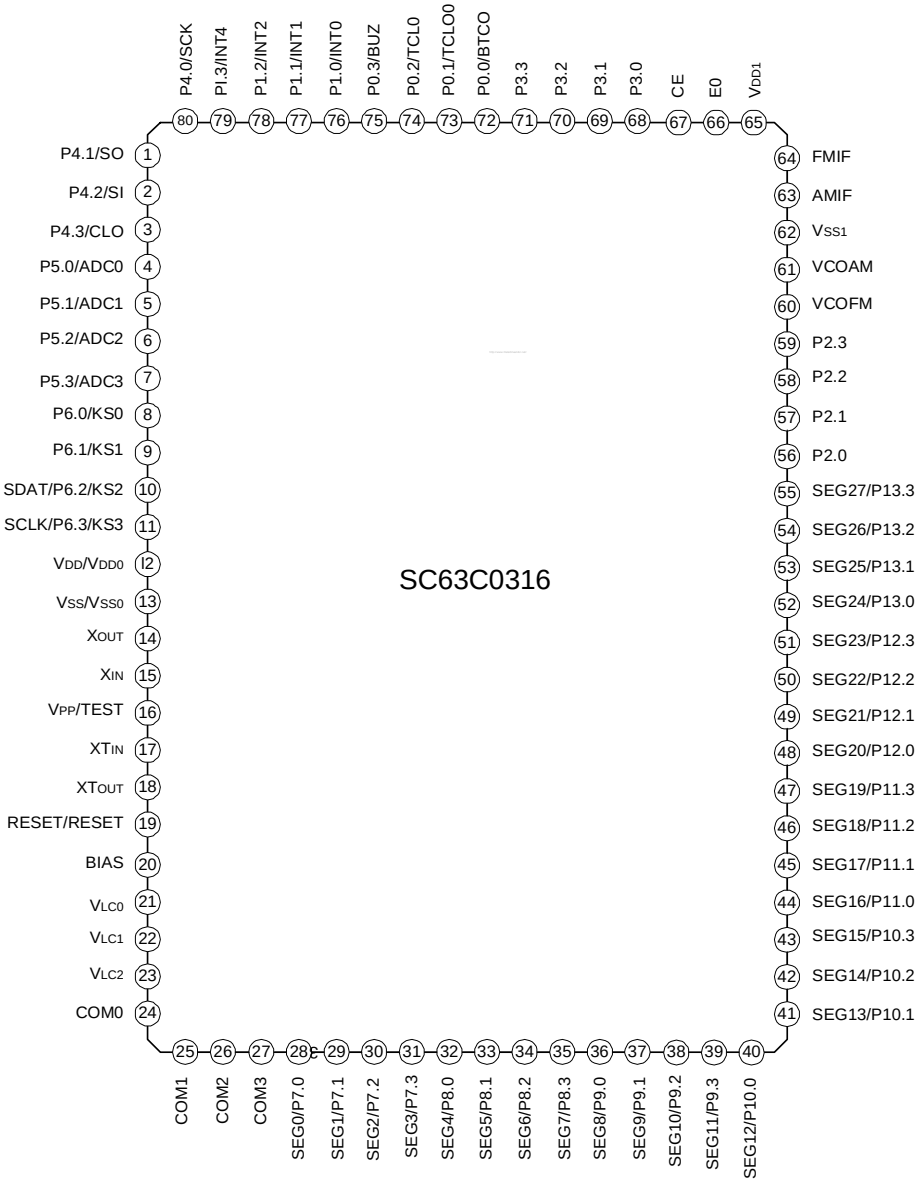
SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS

Oscillator	Characteristics	Test condition	Min	Typ	Max	Units
Crystal Oscillator	Oscillation frequency(1)	--	32	32.768	35	kHz
	Stabilization time (2)	V_{DD}=4.5V~5.5V	--	1.0	2	s
		V_{DD}=1.8V~4.5V	--	--	10	
External clock	XTIN input frequency (1)	--	32	--	100	kHz
	XTIN input high and low level width (tXH, tXL)	--	5	--	15	μs

Note:1. Oscillation frequency and XTIN input frequency data are for oscillator characteristics only.

2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs.

PIN CONFIGURATIONS



PIN DESCRIPTION

Pin No.	Symbol	Description
72 73 74 75	P0.0 P0.1 P0.2 P0.3	4-bit I/O port. 1-bit or 4-bit read, write, and test are possible. Pull-up resistors can be configured by software.
76 77 78 79	P1.0 P1.1 P1.2 P1.3	4-bit input port. 1-bit or 4-bit read and test are possible. Pull-up resistors can be configured by software.
56-59 68-71	P2.0~ P2.3 P3.0~P3.3	4-bit I/O ports. 1-bit, 4-bit or 8-bit read, write and test are possible. Pull-up resistors can be configured by software. Ports 2 and 3 can be paired to support 8-bit data transfer.
80 1 2 3	P4.0 P4.1 P4.2 P4.3	4-bit I/O ports. 1-bit, 4-bit or 8-bit read, write and test are possible. Pull-up resistors can be configured by software.
4 5 6 7	P5.0 P5.1 P5.2 P5.3	Ports 4 and 5 can be paired to support 8-bit data transfer.
8 9 10 11	P6.0 P6.1 P6.2 P6.3	4-bit I/O port. 1-bit, 4-bit or 8-bit read, write and test are possible. Pull-up resistors can be configured by software.
28 29 30 31	P7.0 P7.1 P7.2 P7.3	1-bit or 4-bit output port. Alternatively used for LCD segment output.
32 33 34 35	P8.0 P8.1 P8.2 P8.3	1-bit or 4-bit output port. Alternatively used for LCD segment output.
36 37 38 39	P9.0 P9.1 P9.2 P9.3	1-bit or 4-bit output port. Alternatively used for LCD segment output.
40 41 42 43	P10.0 P10.1 P10.2 P10.3	1-bit or 4-bit output port. Alternatively used for LCD segment output.

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Pin No.	Symbol	Description
44 45 46 47	P11.0 P11.1 P11.2 P11.3	1-bit or 4-bit output port. Alternatively used for LCD segment output.
48 49 50 51	P12.0 P12.1 P12.2 P12.3	1-bit or 4-bit output port. Alternatively used for LCD segment output.
52 53 54 55	P13.0 P13.1 P13.2 P13.3	1-bit or 4-bit output port. Alternatively used for LCD segment output.
24-27	COM0-COM3	Common signal output for LCD display
20	BIAS	LCD power control
21 22 23	VLC0 VLC1 VLC2	LCD power supply. Voltage dividing resistors are assignable by software
12	VDD0	Main power supply
13	VSS0	Main Ground
19	RESET	System reset pin
14 15	XOUT XIN	Crystal, or ceramic oscillator pin for main system clock. (For external clock input, use XIN and input XIN's reverse phase to XOUT)
18 17	XTOUT XTIN	Crystal oscillator pin for subsystem clock. (For external clock input, use XTIN and input XTIN's reverse phase to XTOUT)
16	TEST	Test signal input (must be connected to VSS for normal operation)
67	CE	Input pin for checking device power. Normal operation is high level and PLL/IFC operation is stopped at low level.
60 61	VCOFM VCOAM	External VCOFM/AM signal inputs.
66	EO	PLL's phase error output
64 63	FMIF AMIF	FM/AM intermediate frequency signal inputs.
65	VDD1	PLL/IFC power supply
62	VSS1	PLL/IFC ground
72	BTCO	Basic timer overflow output signal
73	TCLO0	Timer/counter 0 clock output signal
74	TCL0	External clock input for timer/counter 0
75	BUZ	2,4,8 or 16 kHz frequency output for buzzer sound for 4.19 MHz main system clock or 32.768 kHz subsystem clock

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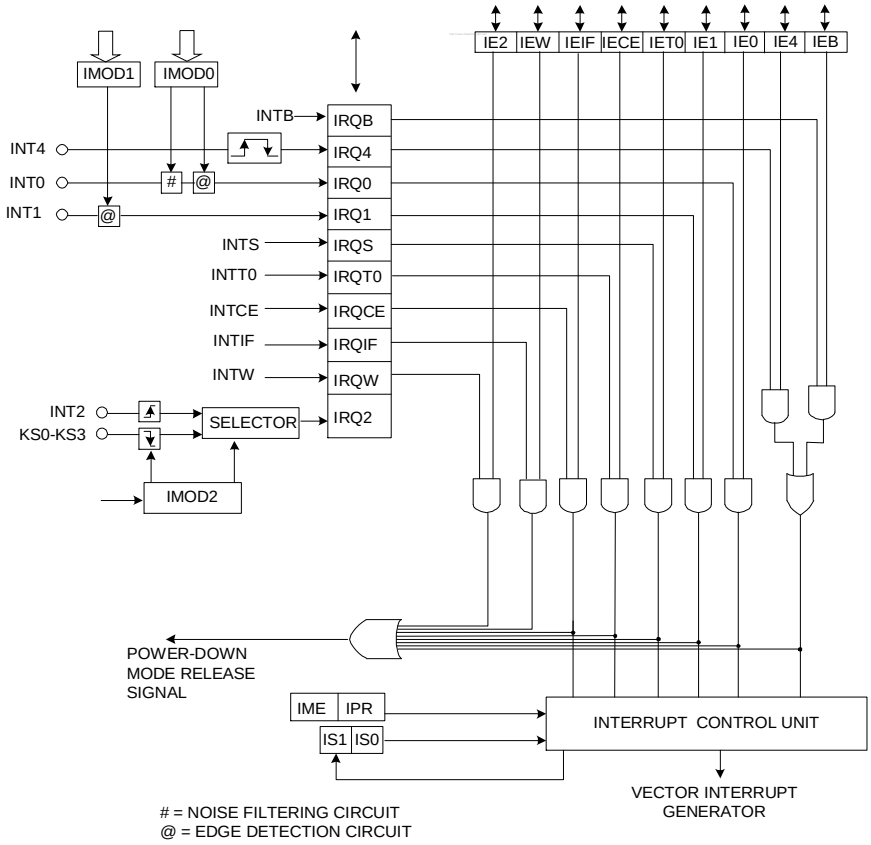
Pin No.	Symbol	Description
76 77	INT0 INT1	External interrupt. The triggering edges (rising/falling) are selectable. Only INT0 is synchronized with system clock.
78	INT2	Quasi-interrupt with detection of rising edge signal.
79	INT4	External interrupt input with detection of rising or falling edges.
80	SCK	SIO interface clock signal
1	SI	SIO interface data input signal
2	SO	SIO interface data output signal
3	CLO	CPU clock output
8-11	KS0-KS3	Quasi-interrupt input with falling edge detection
4-7	ADC0-ADC3	ADC input ports.
28-55	SEG0-SEG27	LCD segment signal output.

FUNCTION DESCRIPTION

INTERRUPTS

The SC63C0316 has four external interrupts, four internal interrupts and two quasi-interrupts. Table 1 shows the conditions for interrupt generation. The request flags that allow these interrupts to be generated are cleared by hardware when the service routine is vectored. The quasi-interrupt's request flags must be cleared by software.

Figure 1. Interrupt Control Circuit Diagram



Note : INT0 can release idle mode only when fxx/64 is selected as a asmpling clock

TABLE1. Interrupt request flag conditions and priorities

Interrupt source	Internal/ External	Condition for IRQx flag setting	Interrupt priority	Request flag name
INTB	I	Reference time interval signal from basic timer	1	IRQB
INT4	E	Both rising and falling edges detected at INT4	1	IRQ4
INT0	E	Rising or falling edge detected at INT0 pin	2	IRQ0
INT1	E	Rising or falling edge detected at INT1 pin	3	IRQ1
INTS	I	Completion signal for serial transmit-and-receive or receive-only operation	4	IRQS
INTT0	I	Signals for TCNT0 and TREF0 retgisters match	5	IRQT0
INTCE	E	When falling edge is detected at CE pin	6	IRQCE
INTIF	I	When gate closes	7	IRQIF
INT2*	E	Rising edge detected at INT2 or else a falling edge is detected at any of the KS0-KS3 pins	--	IRQ2
INTW	I	Time interval of 0.5s or 3.19ms	--	IRQW

* The quasi-interrupt INT2 is only used for testing incoming signals.

INTERRUPT ENABLE FLAGS (IEx)

IEx flags, when set to "1", enable specific interrupt requests to be serviced. When the interrupt request flag is set to "1", an interrupt will not be serviced until its corresponding IEx flag is also enabled. The IPR register contains a global disable bit, IME, which disables all interrupt at once.

INTERRUPT PRIORITY

Each interrupt source can also be individually programmed to high levels by modifying the IPR register. When IS1 = 0 and IS0 = 1, a low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt.

If you clear the interrupt status flags (IS1 and IS0) to "0" in a interrupt service routine, a high-priority interrupt can be interrupted by low-priority interrupt (multi-level interrupt). Before the IPR can be modified by 4-bit write instructions, all interrupts must first be disabled by a DI instruction.

When all interrupts are low priority (the lower three bits of the IPR register are "0"), the interrupt requested first will have high priority. Therefore, the first-requested interrupt cannot be superseded by any other interrupt.

If two or more interrupt requests are received simultaneously, the priority level is determined according to the standard interrupt priorities, where the default priority is assigned by hardware when the lower three IPR bits = "0".

In this case, the higher-priority interrupt request is serviced and the other interrupt is inhibited. Then, when the high-priority interrupt is returned from its service routine by an IRET instruction, the inhibited service routine is started.

Table 2. Interrupt Priority Register Settings

IPR.2	IPR.1	IPR.0	Result of IPR Bit Setting
0	0	0	Process all interrupt requests at default priority settings.
0	0	1	INTB and INT4 at highest priority.
0	1	0	INT0 at highest priority.
0	1	1	INT1 at highest priority.
1	0	0	INTS at highest priority.
1	0	1	INTT0 at highest priority.
1	1	0	INTCE at highest priority.
1	1	1	INTIF at highest priority.

Table 3. Default Priorities

Source	Default Priority
INTB, INT4	1
INT0	2
INT1	3
INTS	4
INTT0	5
INTCE	6
INTIF	7

The interrupt controller can service multiple interrupts in two ways: as two-level interrupts, where either all interrupt requests or only those of highest priority are serviced (see Figure 2), or as multi-level interrupts, when the interrupt service routine for a lower-priority request is accepted during the execution of a higher priority routine. (See Figure 3)

Figure 2: Two-level Interrupt handling

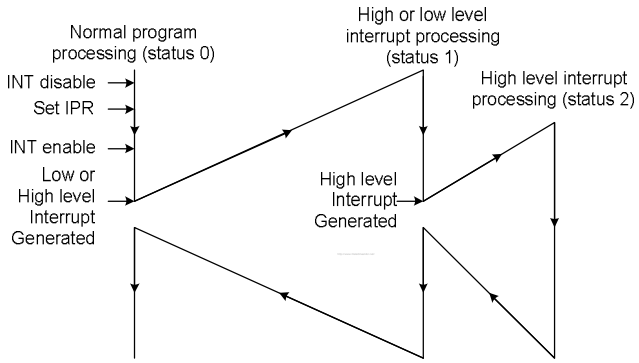
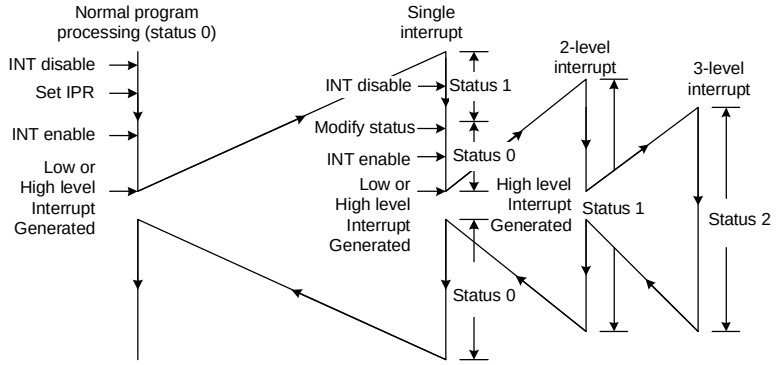


Figure 3: Multi-level Interrupt handling



NOTE: If more than four interrupts are being processed at one time, you can avoid possible loss of working register data by using the PUSH RR instruction to save register contents to the stack before the service routines are executed in the same register bank. When the routines have executed successfully, you can restore the register contents from the stack to working memory using the POP instruction.

Interrupt execute flowchart

A vectored interrupt is generated when the following flags and register settings, corresponding to the specific interrupt (INTn) are set to logic one:

— Interrupt enable flag (IEx)

— Interrupt master enable flag (IME)

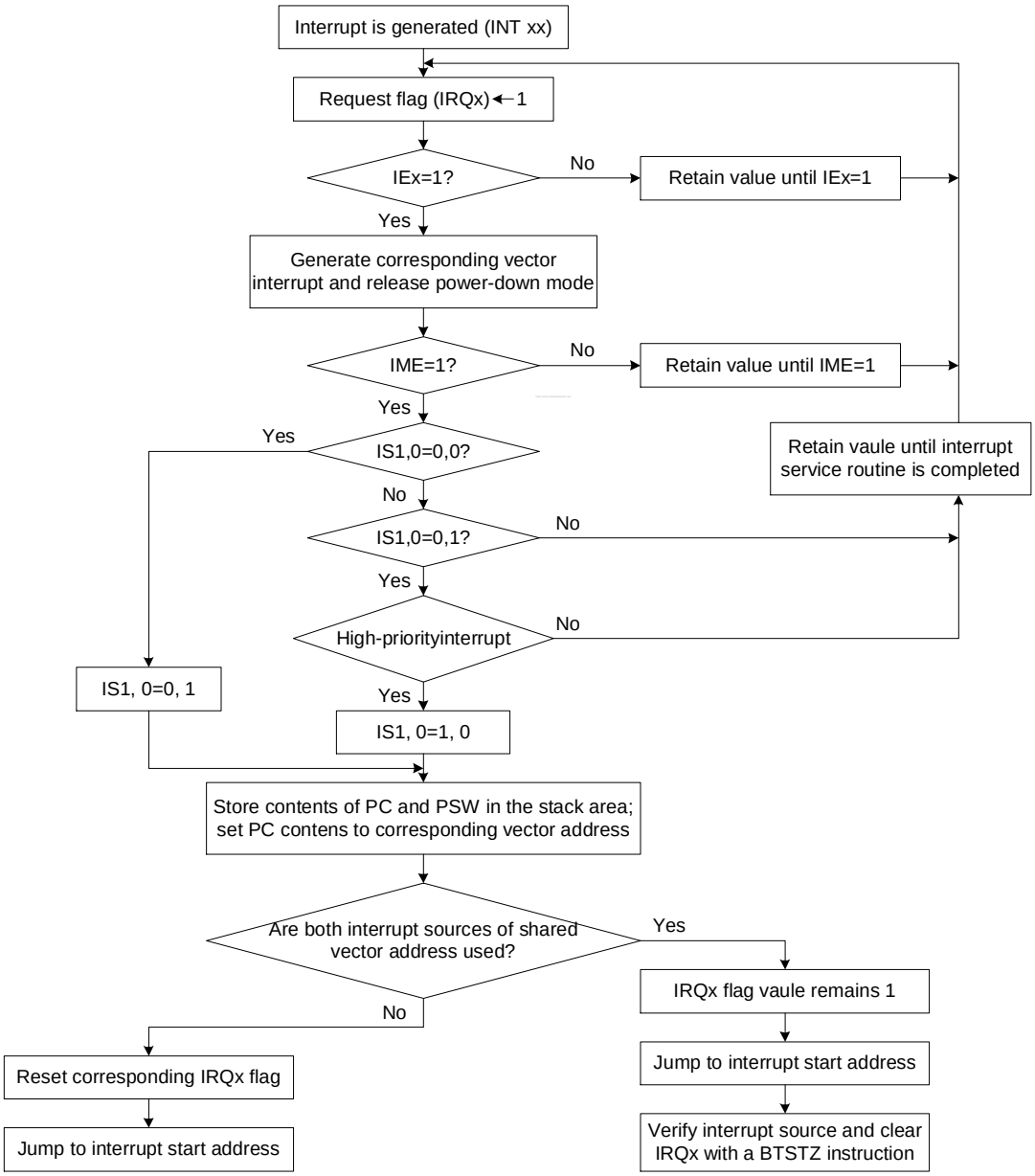
— Interrupt request flag (IRQx)

— Interrupt status flags (IS0, IS1)

— Interrupt priority register (IPR)

If all conditions are satisfied for the execution of a requested service routine, the start address of the interrupt is loaded into the program counter and the program starts executing the service routine from this address.

Figure 4 Interrupt execution flowchart



EXTERNAL INTERRUPTS

The external interrupt mode registers IMOD0 and IMOD1 are used to control the triggering edge of the input signal at INT0 and INT1, respectively. The INT4 interrupt is an exception because its input signal generates an interrupt request on both rising and falling edges.

When a sampling clock rate of fxx/64 is used for INT0, an interrupt request flag must be cleared before 16 machine cycles have elapsed. Since the INT0 pin has a clock-driven noise filtering circuit built into it, please take the following precautions when you use it:

— To trigger an interrupt, the input signal width at INT0 must be at least two times wider than the pulse width of the clock selected by IMOD0. This is true even when the INT0 pin is used for general-purpose input.

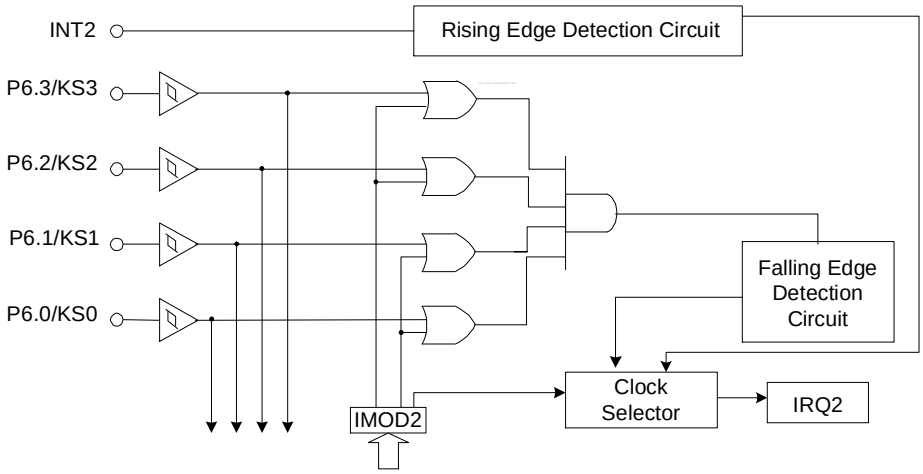
— Because the INT0 input sampling clock does not operate during Stop or Idle mode, you cannot use INT0 to release power-down mode.

EXTERNAL INTERRUPT MODE REGISTER

The external interrupt 2 (INT2) mode register, IMOD2, is used to select INT2 and KSn pins as interrupt input. If a rising edge is detected at the INT2 pin, or when a falling edge is detected at any one of the pins (KS0–KS3), the IRQ2 flag is set to "1" and a release signal for power-down mode is generated.

If one or more of the pins which are configured as key Interrupt (KS0–KS7) are in Low input or Low output state, the key Interrupt can not be occured.

Figure 5.



Note: To generate a key interrupt on a falling edge at KS0-KS3, all KS0-KS3 pins must be configured to input mode.

I/O PORTS

The SC63C0316 has 14 ports. There are total of 4 input pins, 28 output pins, 16 configurable I/O pins, and 8 nchannel open-drain I/O pins, for a maximum number of 56 I/O pins.

Pin addresses for all ports except ports 7-13 are mapped in bank 15 of the RAM. Ports 7-13 pin addresses are in bank 1 of the RAM. The contents of I/O port pin latches can be read, written, or tested at the corresponding address using bit manipulation instructions.

PORT MODE FLAGS (PM FLAGS)

Port mode flags (PM) are used to configure I/O ports to input or output mode by setting or clearing the corresponding I/O buffer. If a PM bit is "0", the corresponding I/O pin is set to input mode. If the PM bit is "1", the pin is set to output mode. PM flags are addressable by 8-bit write instructions only.

PULL-UP RESISTOR MODE REGISTER (PUMOD)

The pull-up resistor mode register, PUMOD, is an 8-bit register used to assign internal pull-up resistors by software to specific I/O ports. When a PUMOD bit is "1", a pull-up resistor is assigned to the corresponding I/O port: When a configurable I/O port pin is used as an output pin, its assigned pull-up resistor is automatically disabled, even though the pin's pull-up is enabled by a corresponding PUMOD bit setting.

PUMOD is addressable by 8-bit write instructions only. A system reset clears PUMOD values to logic zero, automatically disconnecting all software-assignable port pull-up resistors.

Table 4. Pull-Up Resistor Mode Register (PUMOD) Organization

PUMOD ID	Address	Bit3	Bit2	Bit1	Bit0
PUMOD	FDCH	PUR3	PUR2	PUR1	PUR0
	FDDH	"0"	PUR6	PUR5	PUR4

Table 5. Port Mode Group Flags (8-Bit W)

PM Group ID	Address	Bit3/7	Bit2/6	Bit1/5	Bit0/4
PMG0	FE6H	PM0.3	PM0.2	PM0.1	PM0.0
	FE7H	“0”	“0”	“0”	“0”
PMG1	FE8H	PM2.3	PM2.2	PM2.1	PM2.0
	FE9H	PM3.3	PM3.2	PM3.1	PM3.0
PMG2	FEAH	PM4.3	PM4.2	PM4.1	PM4.0
	FEBH	PM5.3	PM5.2	PM5.1	PM5.0
PMG3	FECH	PM6.3	PM6.2	PM6.1	PM6.0
	FEDH	“0”	“0”	“0”	“0”

N-CHANNEL OPEN-DRAIN MODE REGISTER(PNE)

The N-channel, open-drain mode register, PNE, is used to configure port 7 to 13 to N-channel open-drain modes or push-pull modes.

When a bit in the PNE register is set to “1”, the corresponding output pin is configured to N-channel open-drain; when set to “0”, the output pin is configured to push-pull mode.

The PNE register consists of an 8-bit register, as shown below, PNE can be addressed by 8-bit write instructions only.

Table 6. N-channel open drain mode register (PNE) setting

ID	Address	Bit 3/7	Bit 2/6	Bit1/5	Bit0/4
PNE	FD6H	PNE10	PNE9	PNE8	PNE7
	FD7H	“0”	PNE13	PNE12	PNE11

A/D CONVERTER

To operate the A/D converter, one of the four analog input channels is selected by writing the appropriate value to the ADC mode register.

To start the converter, the ADSTR flag in the control register AFLAG must be set to "1". Conversion speed is determined by the oscillator frequency and the CPU clock. When the A/D operation is complete, the EOC flag must be tested in order to verify that the conversion was successful. When the EOC value is "0", the converted digital values stored in the data register ADATA can be read.

Figure 6. A/D Converter Circuit Diagram

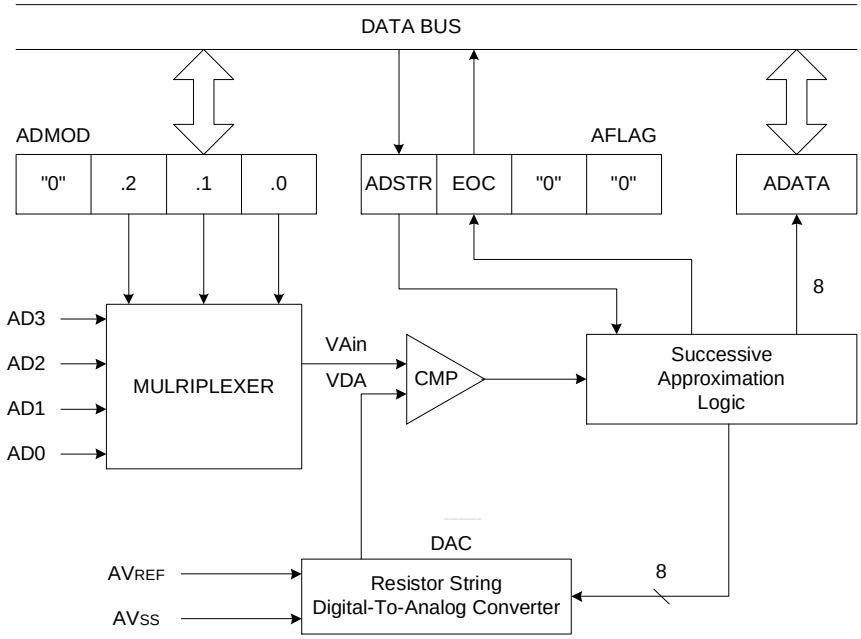
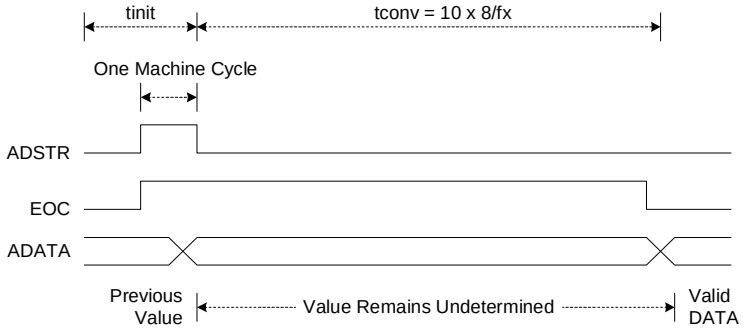


Figure 7. A/D Converter Timing Diagram



ADC DIGITAL-TO-ANALOG CONVERTER (DAC)

The 8-bit digital-to-analog converter (DAC) generates analog voltage reference values for the comparator.

The DAC is a 256-step resistor string type digital-to-analog converter that uses successive approximation logic to convert digital input into the reference analog voltage, VDA. The VDA values are input from the DAC to the comparator where they are compared to the multiplexed external analog source voltage, VAin. Since the DAC has 8-bit resolution, it generates the 256-step analog reference voltage.

ADC DATA REGISTER (ADATA)

The A/D converter data register, ADATA, is an 8-bit register in which digital data values are stored as an A/D conversion operation is completed. Digital values stored in ADATA are retained until another conversion operation is initiated. ADATA is addressable by 8-bit read instructions only.

ADC MODE REGISTER (ADMOD)

The analog-to-digital converter mode register, ADMOD, is used to select one of four analog channels as the analog data input source. Bit 3 in the ADMOD register is always "0".

Table 7. A/D Converter Mode Register Settings (1, 4-Bit R/W)

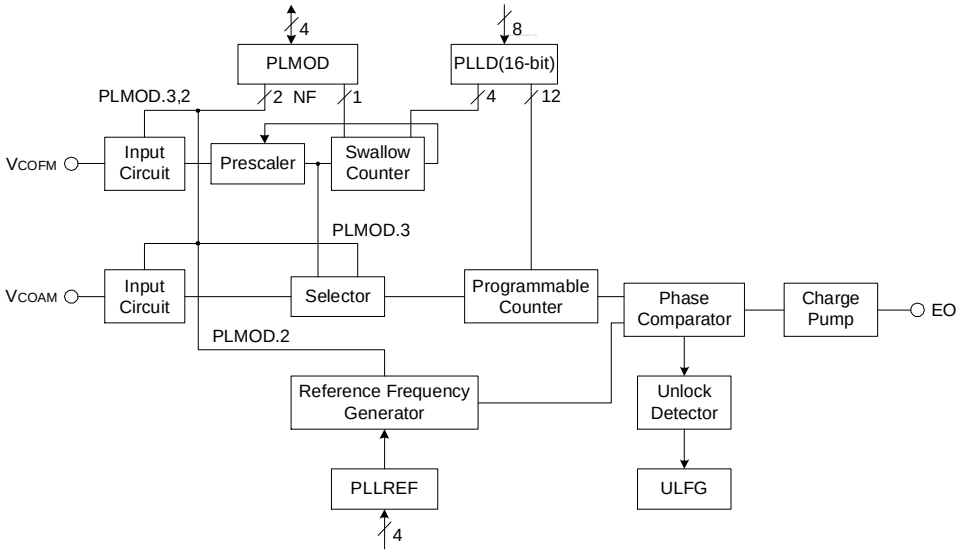
ADMOD.2	ADMOD.1	ADMOD.0	Effect of ADMOD Bit Setting
1	0	0	Select input channel AD0
0	0	1	Select input channel AD1
0	1	0	Select input channel AD2
0	1	1	Select input channel AD3

NOTE: If ADMOD.2–ADMOD.0 = 0, disable analog input channel selection.

PLL FREQUENCY SYNTHESIZER

The phase locked loop (PLL) frequency synthesizer locks medium frequency (MF), high frequency (HF), and very high frequency (VHF) signals to a fixed frequency using a phase difference comparison system.

Figure 8. PLL Frequency Synthesizer Block Diagram



PLL FREQUENCY SYNTHESIZER FUNCTIONS

The PLL frequency synthesizer divides the signal frequency at the VCOAM or VCOFM pin using the programmable divider. It then outputs the phase difference between the divided frequency and reference frequency at the EO pins.

NOTE

The PLL frequency synthesizer operates only when the CE pin is high level; it enters the disable mode when the CE pin is low.

PHASE DETECTOR, CHARGE PUMP, AND UNLOCK DETECTOR

The phase comparator compares the phase difference between divided frequency (fN) output from the programmable divider and the reference frequency (fr) output from the reference frequency generator.

The charge pump outputs the phase comparator's output from error output pins EO. The relation between the error output pin output, divided frequency fN, and reference frequency fr is shown below:

fr > f_N = Low level output

fr < f_N = High level output

fr = f_N = Floating level

When PLL operation is started by setting PLMOD register, PLL unlock flag (ULFG) in the PLL flag register (PLLREG) has unlock state information between the reference frequency and divided frequency. The unlock detector detects the unlock state of the PLL frequency synthesizer. The unlock flag in the PLLREG register is set to "1" in unlock state. If ULFG = "0", the PLL lock state is selected.

PLLREG

ULFG	CEFG	IFCFG	0

ULFG is set continuously at a period of reference frequency f r by unlock detector. You must therefore read ULFG flag in the PLLREG register at periods longer than 1/f r of the reference frequency. ULFG is reset when it is read. PLLREG register can be read by 1-bit or 4-bit RAM control register instructions.

PLL operation is decided by CE (chip enable) pin state. The PLL frequency synthesizer is disabled and the error output pin is set to floating state while the CE pin is low. When CE pin is high level, PLL is operating normally.

The chip enable flag (CEFG) in the PLLREG register has information about CE pin state. When the CE pin changes its low state to high, CEFG flag is set to logic one and CE reset operation occurs. When the CE pin changes its high state to low, CEFG flag is set to logic zero and CE interrupt is generated.

INTERMEDIATE FREQUENCY COUNTER

The SC63C0316 uses an intermediate frequency counter (IFC) to count the frequency of the AM or FM signal at FMIF or AMIF pin. The IFC block consists of a 1/2 divider, gate control circuit, IFC mode register (IFMOD) and a 16-bit binary counter.

During gate time, the 16-bit IFC counts the input frequency at the FMIF or AMIF pins. The FMIF or AMIF pin input signal for the 16-bit counter is selected by IFMOD register. The 16-bit binary counter (IFCNT1–IFCNT0) can be read by 8-bit RAM control instructions only.

When the FMIF pin input signal is selected, the signal is divided by 2. When the AMIF pin input signal is directly connected to the IFC, it is not divided.

By setting the IFMOD register, the gate is opened for 1-ms, 4-ms, or 8-ms periods. During the open period of the gate, input frequency is counted by the 16-bit counter. When the gate is closed, the counting operation is complete, and an interrupt is generated.

Figure 9. IF Counter Block Diagram

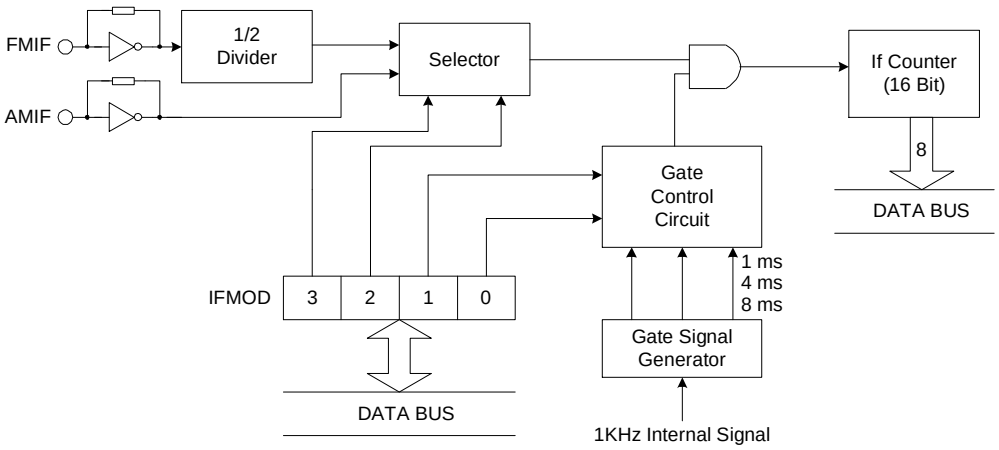


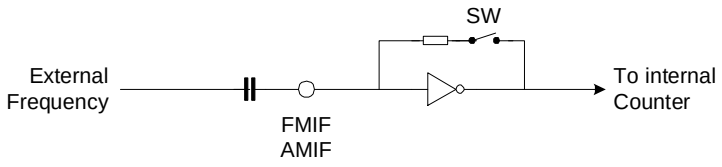
Table 8. IF Counter Frequency Ranges

Pin	Voltage Level	Frequency Range
AMIF	300mVpp(min)	0.1MHz to 1MHz
FMIF	300mVpp(min)	5MHz to 15MHz

INPUT PIN CONFIGURATION

The AMIF and FMIF pins have built-in AC amplifiers (see Figure 32). The DC component of the input signal must be stripped off by the external capacitor. When the AMIF or FMIF pin is selected for the IFC function and the switch is turned on voltage of each pin increases to approximately 1/2 VDD after sufficiently long time. If the pin voltage does not increase to approximately 1/2 VDD , the AC amplifier exceeds its operating range, possibly causing an IFC malfunction. To prevent this from occurring, you should program a sufficiently long time delay interval before starting the count operation.

Figure 10. AMIF and FMIF Pin Configuration



LCD CONTROLLER/DRIVER

The SC63C0316 microcontroller can directly drive 4 com x 28-segment LCD panel. Data written to the LCD display RAM can be transferred to the segment signal pins automatically without program control.

When a subsystem clock is selected as the LCD clock source, the LCD display is enabled even during the Stop1 and Idle power-down modes.

LCD RAM ADDRESS AREA

RAM addresses 1E4H–1FFH are used as LCD data memory. These locations can be addressed by 1-bit or 4-bit instructions. When the bit value of a display segment is "1", the LCD display is turned on; when the bit value is "0", the display is turned off.

Display RAM data are sent out through segment pins SEG0–SEG27 using a direct memory access (DMA)

method that is synchronized with the fLCD signal.

RAM addresses in this location that are not used for LCD display can be allocated to general-purpose use.

Figure 11. LCD Display Data RAM Organization

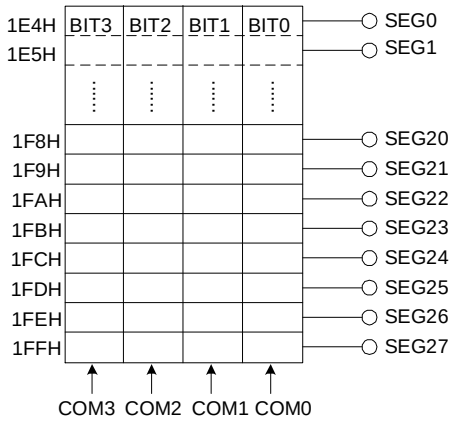
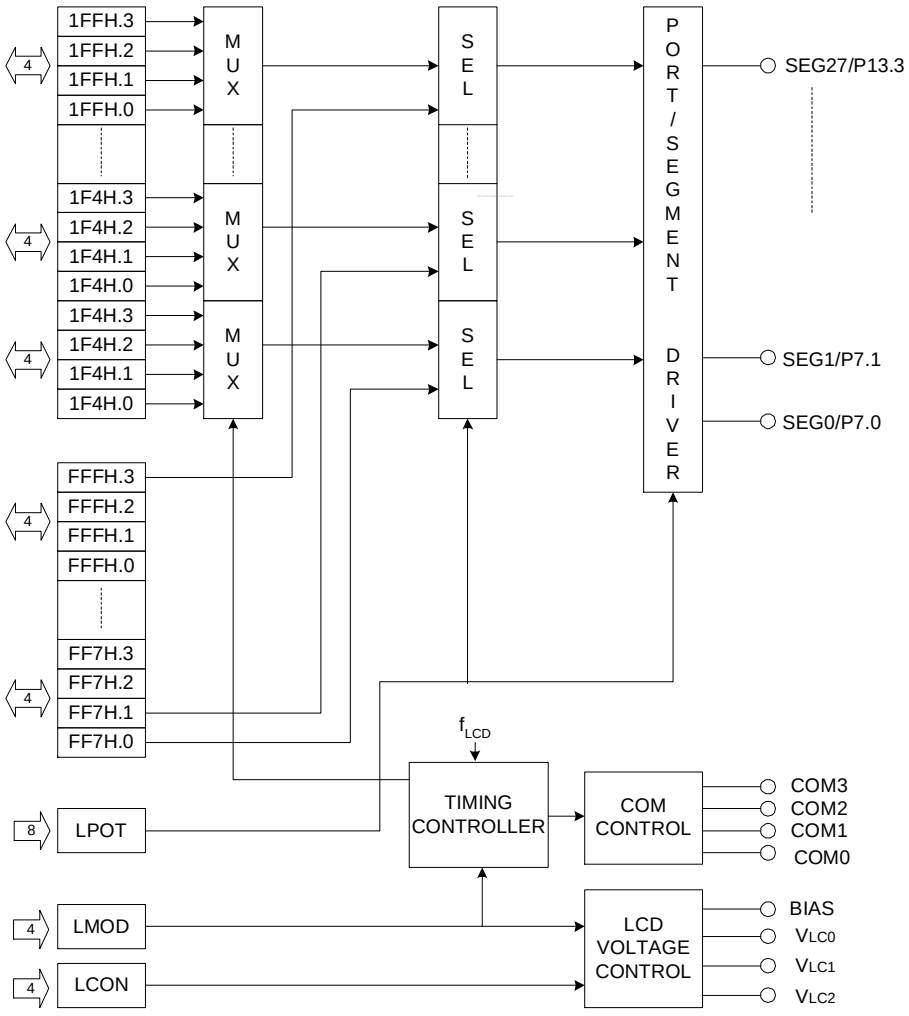


Figure 12. LCD Circuit Diaram



LCD CONTROL REGISTER (LCON)

The LCON register is used to turn the LCD display on and off and to control the flow of current to dividing resistors in the LCD circuit. When LCON.0 is logic zero, the LCD display is turned off and the current to the dividing resistors is cut off, regardless of the current LMOD.3 value.

Table 9. LCD Control Register (LCON) Organization (4-Bit W)

LCON Bit	Setting	Description
LCON.3	0	Always set to logic zero.
LCON.2	0	Always set to logic zero.
LCON.1	0	Port 6 input enable
	1	Port 6 input disable
LCON.0	0	LCD output low, cut off current to dividing resistor
	1	When LMOD.3=”0”: turn display off. When LMOD.3=”1”: COM and SEG output in display mode.

Table 10 Relationship of LCON.0 and LMOD.3 Bit Settings

LCON.0	LMOD.3	COM0–COM3	SEG0–SEG31	P11.0–P13.3
0	x	Output low; LCD display off	Output low; LCD display off	LCD display off , cut off current to dividing resistors
1	0	LCD display off	LCD display off	LCD display off
	1	COM output corresponds to display mode	SEG output corresponds to display mode	LCD display on

NOTE:'x' means 'don't care.'

LCD MODE REGISTER (LMOD)

The LCD mode control register LMOD is used to control display mode; LCD clock, segment or port output, and display on/off. The LCD clock signal, LCDCK, determines the frequency of COM signal scanning of each segment output. This is also referred to as the 'frame frequency.

Because LCDCK is generated by dividing the watch timer clock (fw), the watch timer must be enabled when the LCD display is turned on. The LCD display can continue to operate during Idle and Stop modes if a subsystem clock is used as the watch timer source.

Table 11. LCD Clock Signal (LCDCK) Frame Frequency

LCDCK Frequency	Static	1/2 Duty	1/3 Duty	1/4 Duty
$fw/2^9$ (64Hz)	64	32	21	16
$fw/2^8$ (128Hz)	128	64	43	32
$fw/2^7$ (256Hz)	256	128	85	64
$fw/2^6$ (512Hz)	512	256	171	128

NOTES: 'fw' is the watch timer clock frequency of 32.768 kHz.

Table12. Maximum Number of Display Digits Per Duty Cycle

LCD Duty	LCD Bias	COM Output Pins	Maximum Digit Display 8 Segment Pins)
Static	Static	COM0	4
1/2	1/2	COM0–COM1	8
1/3	1/2	COM0–COM2	12
1/3	1/3	COM0–COM2	12
1/4	1/3	COM0–COM3	16

Table 13. LCD Mode Control Register (LMOD) Organization (8-Bit W)

LMOD.7	LCD voltage dividing register control bit
0	Internal voltage dividing resistor.
1	External voltage dividing resistor; internal voltage dividing resistors are off.

LMOD.6	Always logic zero

LMOD.5	LMOD.4	LCD Clock (LCDCK) Frequency
0	0	$fw/2^9$ = 64 Hz
0	1	$fw/2^8$ = 128 Hz
1	0	$fw/2^7$ = 256 Hz
1	1	$fw/2^6$ = 512 Hz

LMOD.3	LMOD.2	LMOD.1	LMOD.0	Duty and Bias Selection for LCD Display
0	x	x	x	LCD display off
1	0	0	0	1/4 duty, 1/3 bias
1	0	0	1	1/3 duty, 1/3 bias
1	0	1	0	1/2 duty, 1/2 bias
1	0	1	1	1/3 duty, 1/2 bias
1	1	0	0	Static

NOTE:'x' means 'don't care'.

LCD DRIVE VOLTAGE

The LCD display is turned on only when the voltage difference between the common and segment signals is greater than VLCD. The LCD display is turned off when the difference between the common and segment signal voltages is less than VLCD.

NOTE: The LCD panel display may deteriorate if a DC voltage is applied that lies between the common and segment signal voltage. Therefore, always drive the LCD panel with AC voltage

COMMON (COM) SIGNALS

The common signal output pin selection (COM pin selection) varies according to the selected duty cycle.

Table 14. Common Signal Pins Used Per Duty Cycle

Display Mode	COM0 Pin	COM1 Pin	COM2 Pin	COM3 Pin
Static	Selected	N/C	N/C	N/C
1/2 duty	Selected	Selected	N/C	N/C
1/3 duty	Selected	Selected	Selected	N/C
1/4 duty	Selected	Selected	Selected	Selected

NOTE:'NC'means that no connection is required

Figure 13. LCD Common Signal Waveform (static)

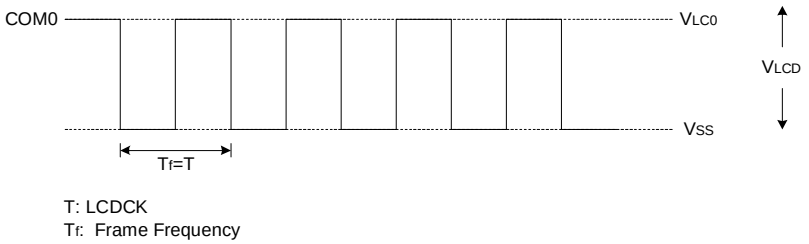


Figure 14. LCD Common Signal Waveforms at 1/2 Bias (1/2, 1/3 Duty)

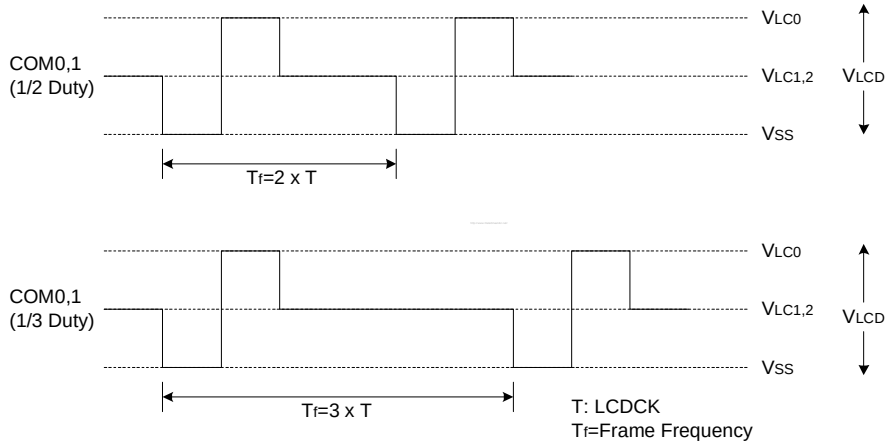
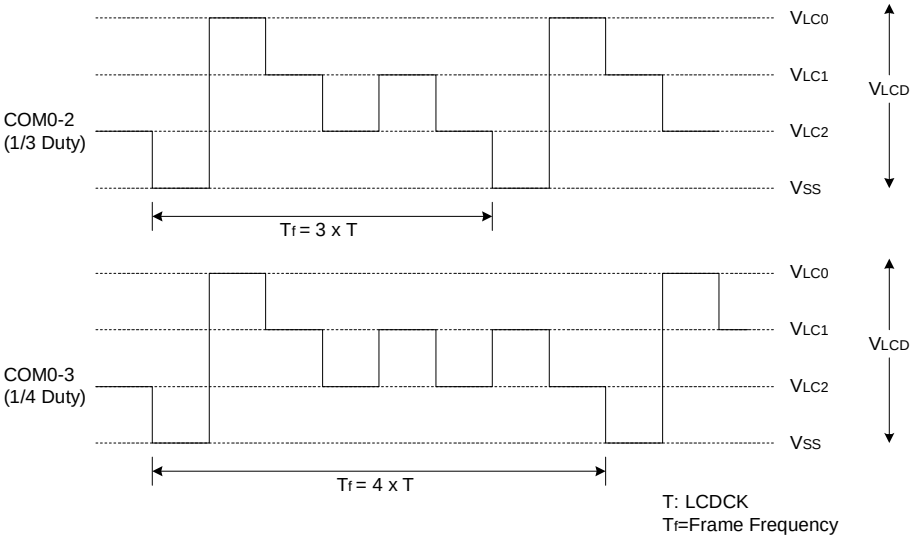


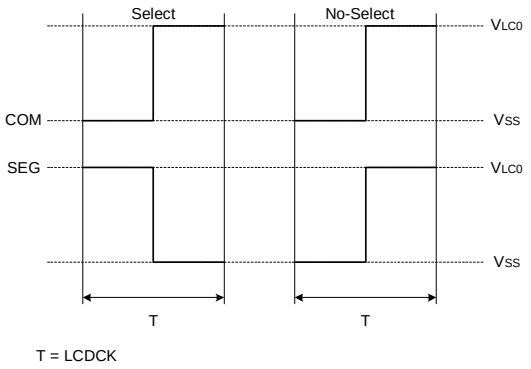
Figure 15. LCD Common Signal Waveforms at 1/3 Bias (1/3, 1/4 Duty)



SEGMENT (SEG) SIGNALS

The 40 LCD segment signal pins are connected to corresponding display RAM locations at 1E0H–1FFH. Bits 0–3 of the display RAM are synchronized with the common signal output pins COM0, COM1, COM2, and COM3.

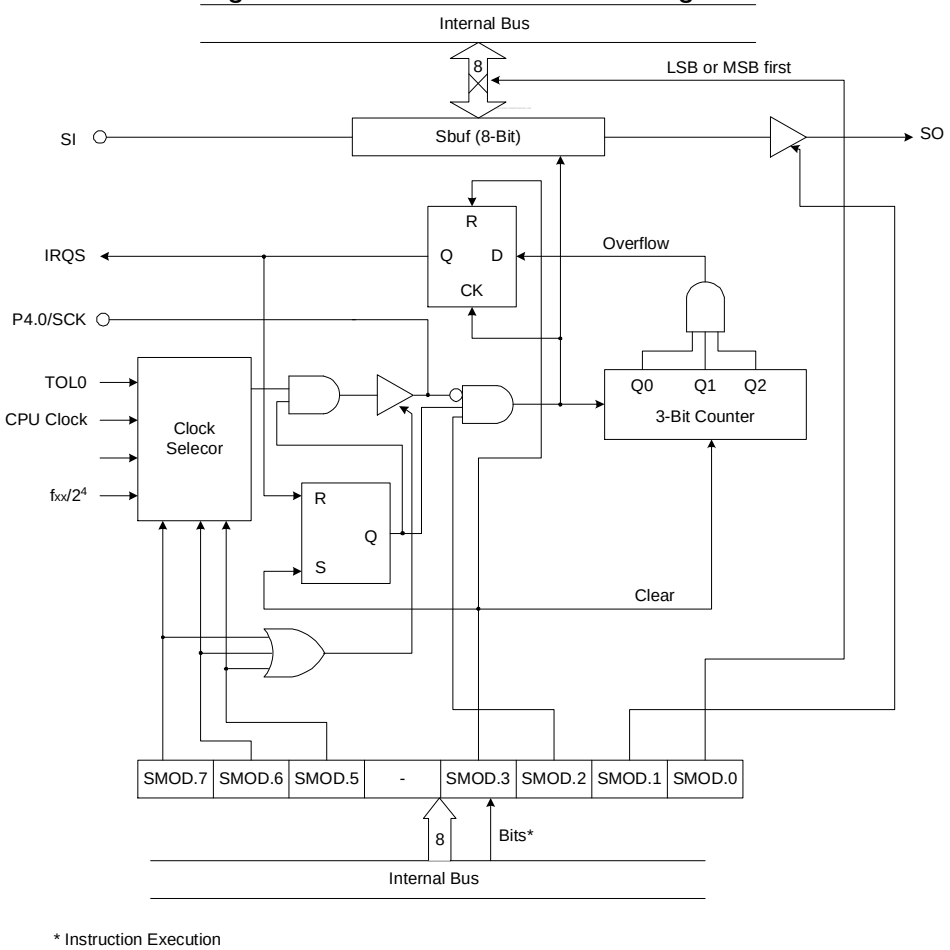
Figure 16. Select/No-Select Bias Signals in Static Display Mode



SERIAL I/O INTERFACE

Using the serial I/O interface, you can exchange 8-bit data with an external device. The serial interface can run off an internal or an external clock source, or the TOL0 signal that is generated by the 8-bit timer/counter 0, TC0. If you use the TOL0 clock signal, you can modify its frequency to adjust the serial data transmission rate.

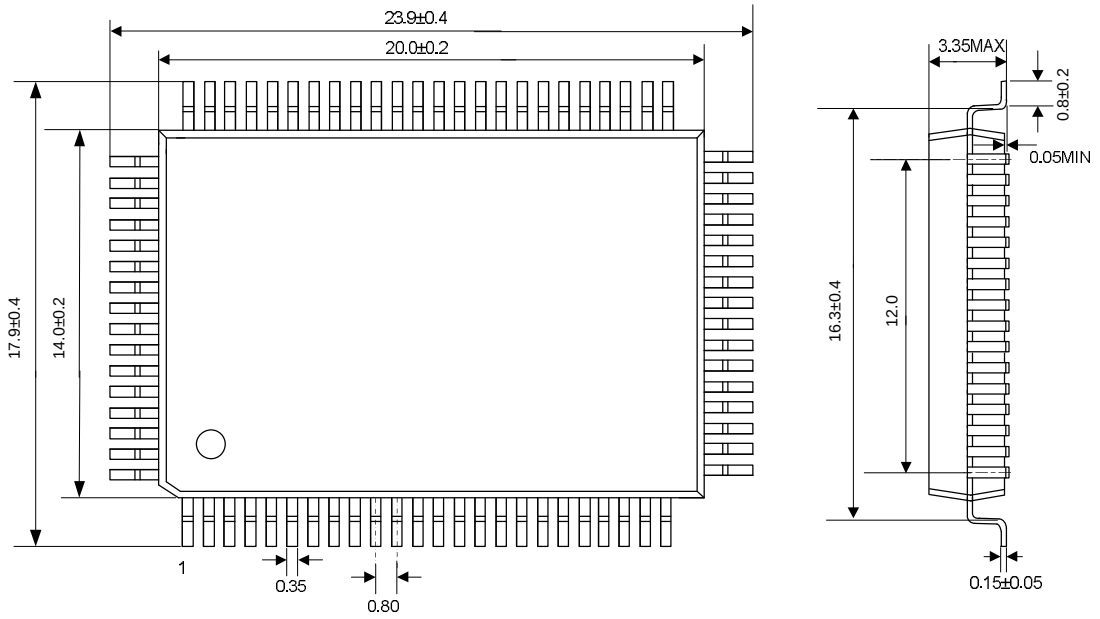
Figure 17. Serial I/O Interface Circuit Diagram



* Instruction Execution

PACKAGE OUTLINE

QFP-80-14×20-0.8 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.