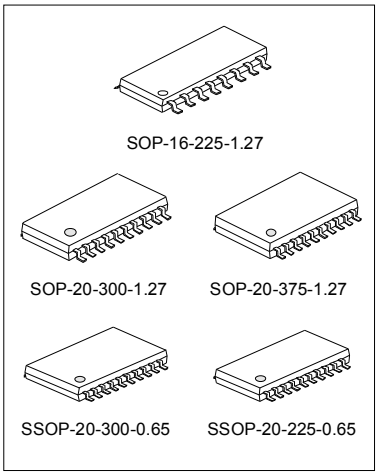
4-BIT MCU FOR REMOTE CONTROLLER(MASK TYPE)

DESCRIPTION

SC73C1602 is one of Silan's 4-bit CMOS single-chip micro-controllers for infrared remote control transmitters (IRCTs). It can be implemented in various IRCTs circuits by mask option.



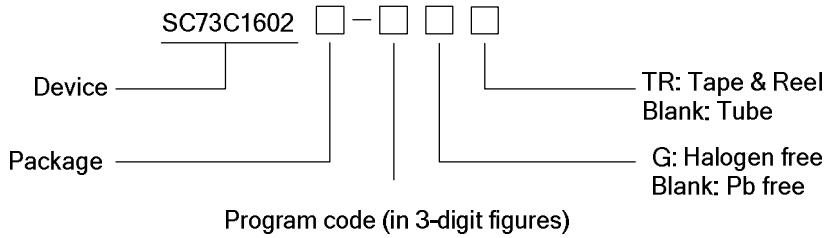
FEATURES

* Wide operating voltage (1.8~4.0V)
* Low static power consumption (<1μA)
* ROM: 2K x 9 bits
* Data memory: 32 x 4bits
* Timer/counter: (10~15 bits)
* 8-bit timer, generates various frequencies and duty carrier
* 16 I/O pins, four 4-bit I/O ports (export P53)
* Oscillator frequency (fosc): fosc=4MHz (TYP.)
  or fosc=455KHz(TYP.)
* Operating frequency (fmain): fosc/8 (fosc=4MHz)
  fosc (fosc=455KHz)
* Instruction cycle: 5/fmain
* Support low voltage detection

APPLICATIONS

* Infrared remote control devices, such as TV, Video Cassette Recorder, VTR, laser phonograph and acoustics remote controllers.

ORDERING INFORMATION

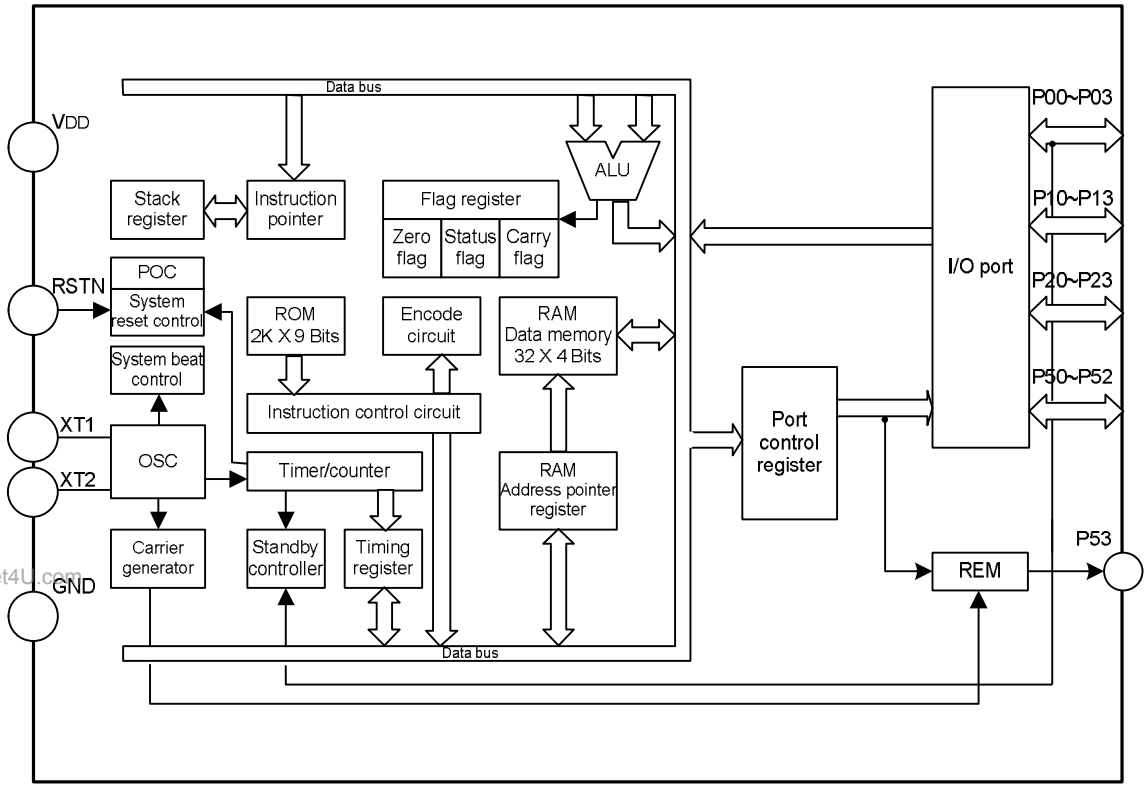


Part No.	Package	Pin Layout Format	Material	Package Type
SC73C1602N-XXX	SSOP-20-300-0.65	Format 1	Pb free	Tube
SC73C1602N-XXXG	SSOP-20-300-0.65		Halogen free	Tube
SC73C1602N-XXXTR	SSOP-20-300-0.65		Pb free	Tape & Reel
SC73C1602N-XXXGTR	SSOP-20-300-0.65		Halogen free	Tape & Reel
SC73C1602NA-XXX	SOP-20-300-1.27		Pb free	Tube
SC73C1602NA-XXXG	SOP-20-300-1.27		Halogen free	Tube
SC73C1602NA-XXXTR	SOP-20-300-1.27		Pb free	Tape & Reel
SC73C1602NA-XXXGTR	SOP-20-300-1.27		Halogen free	Tape & Reel
SC73C1602NC-XXX	SSOP-20-225-0.65		Pb free	Tube

Part No.	Package	Pin Layout Format	Material	Package Type
SC73C1602NC-XXXG	SSOP-20-225-0.65	Format 1	Halogen free	Tube
SC73C1602NC-XXXTR	SSOP-20-225-0.65		Pb free	Tape & Reel
SC73C1602NC-XXXGTR	SSOP-20-225-0.65		Halogen free	Tape & Reel
SC73C1602ND-XXX	SOP-20-375-1.27		Pb free	Tube
SC73C1602ND-XXXG	SOP-20-375-1.27		Halogen free	Tube
SC73C1602ND-XXXTR	SOP-20-375-1.27		Pb free	Tape & Reel
SC73C1602ND-XXXGTR	SOP-20-375-1.27		Halogen free	Tape & Reel
SC73C1602NE-XXX	SOP-16-225-1.27		Pb free	Tube
SC73C1602NE-XXXG	SOP-16-225-1.27		Halogen free	Tube
SC73C1602NE-XXXTR	SOP-16-225-1.27		Pb free	Tape & Reel
SC73C1602NE-XXXGTR	SOP-16-225-1.27		Halogen free	Tape & Reel
SC73C1602M-XXX	SSOP-20-300-0.65	Format 2	Pb free	Tube
SC73C1602M-XXXG	SSOP-20-300-0.65		Halogen free	Tube
SC73C1602M-XXXTR	SSOP-20-300-0.65		Pb free	Tape & Reel
SC73C1602M-XXXGTR	SSOP-20-300-0.65		Halogen free	Tape & Reel
SC73C1602MA-XXX	SOP-20-300-1.27		Pb free	Tube
SC73C1602MA-XXXG	SOP-20-300-1.27		Halogen free	Tube
SC73C1602MA-XXXTR	SOP-20-300-1.27		Pb free	Tape & Reel
SC73C1602MA-XXXGTR	SOP-20-300-1.27		Halogen free	Tape & Reel
SC73C1602MC-XXX	SSOP-20-225-0.65		Pb free	Tube
SC73C1602MC-XXXG	SSOP-20-225-0.65		Halogen free	Tube
SC73C1602MC-XXXTR	SSOP-20-225-0.65		Pb free	Tape & Reel
SC73C1602MC-XXXGTR	SSOP-20-225-0.65		Halogen free	Tape & Reel
SC73C1602MD-XXX	SOP-20-375-1.27		Pb free	Tube
SC73C1602MD-XXXG	SOP-20-375-1.27		Halogen free	Tube
SC73C1602MD-XXXTR	SOP-20-375-1.27		Pb free	Tape & Reel
SC73C1602MD-XXXGTR	SOP-20-375-1.27		Halogen free	Tape & Reel
SC73C1602ME-XXX	SOP-16-225-1.27		Pb free	Tube
SC73C1602ME-XXXG	SOP-16-225-1.27		Halogen free	Tube
SC73C1602ME-XXXTR	SOP-16-225-1.27		Pb free	Tape & Reel
SC73C1602ME-XXXGTR	SOP-16-225-1.27		Halogen free	Tape & Reel
SC73C1602Q-XXX	SSOP-20-300-0.65	Format 3	Pb free	Tube
SC73C1602Q-XXXG	SSOP-20-300-0.65		Halogen free	Tube
SC73C1602Q-XXXTR	SSOP-20-300-0.65		Pb free	Tape & Reel
SC73C1602Q-XXXGTR	SSOP-20-300-0.65		Halogen free	Tape & Reel
SC73C1602QA-XXX	SOP-20-300-1.27		Pb free	Tube
SC73C1602QA-XXXG	SOP-20-300-1.27		Halogen free	Tube
SC73C1602QA-XXXTR	SOP-20-300-1.27		Pb free	Tape & Reel
SC73C1602QA-XXXGTR	SOP-20-300-1.27		Halogen free	Tape & Reel

Part No.	Package	Pin Layout Format	Material	Package Type
SC73C1602QC-XXX	SSOP-20-225-0.65	Format 3	Pb free	Tube
SC73C1602QC-XXXG	SSOP-20-225-0.65		Halogen free	Tube
SC73C1602QC-XXXTR	SSOP-20-225-0.65		Pb free	Tape & Reel
SC73C1602QC-XXXGTR	SSOP-20-225-0.65		Halogen free	Tape & Reel
SC73C1602QD-XXX	SOP-20-375-1.27		Pb free	Tube
SC73C1602QD-XXXG	SOP-20-375-1.27		Halogen free	Tube
SC73C1602QD-XXXTR	SOP-20-375-1.27		Pb free	Tape & Reel
SC73C1602QD-XXXGTR	SOP-20-375-1.27		Halogen free	Tape & Reel

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Tamb=25°C)

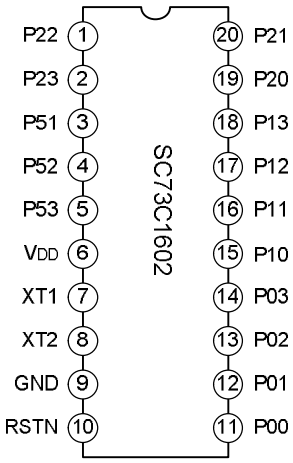
Characteristics	Symbol	Value	Units
Supply Voltage	V_{DD}	-0.3 ~ +5.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
Output Current	I_{OUT} (P53)	-12.0	mA
Power Consumption	P_D	500	mW
Storage Temperature	T_{stg}	-40~+125	°C
Operating Temperature	T_{opr}	-20~+75	°C

ELECTRICAL CHARACTERISTICS (T_{amb}=25°C, V_{DD}=3.0V)

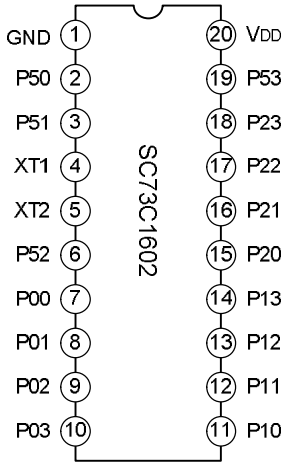
Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Units.
Power Supply Voltage	V_{DD}	All function		1.8	3.0	4	V
Low Voltage Reset Voltage	V_{LVD}	All function		1.1	--	1.4	V
Operating Current	I_{DD}	In operating		--	--	0.5	mA
Oscillation Frequency	F_{OSC}	MASK1		300K	455k	2M	Hz
		MASK2		2M	4M	6M	Hz
Static Power Consumption	I_{DS}	Oscillator stops		--	--	1	μA
Input Pull-Down Resistor	R	V_{DD}=3V	P00-P03 P10-P13 P20-P23 P50-P52	80	95	110	KΩ
High Input Voltage	V_{IH}	--		0.7V_{DD}	--	V_{DD}	V
Low Input Voltage	V_{IL}	--		0	--	0.3V_{DD}	V
High Output Current	I_{OH}	V_{DD}=3V V_{OH}=2.7V	P53	--	-12.0	--	mA
			P00-P03 P10-P13 P20-P23 P50-P52	--	-2.0	--	
Low Output Current	I_{OL}	V_{DD}=3V V_{OL}=0.3V	P53	--	1.0	--	mA
			P00-P03 P10-P13 P20-P23 P50-P52	--	0.15	--	

PIN CONFIGURATIONS (20 PINS CONFIGURATION)

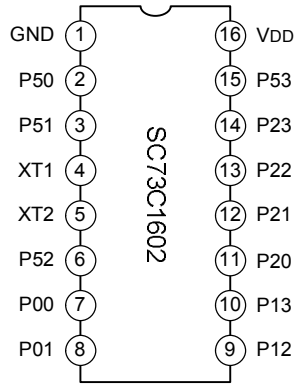
SOP-20/SSOP-20 Pin Layout Format 1



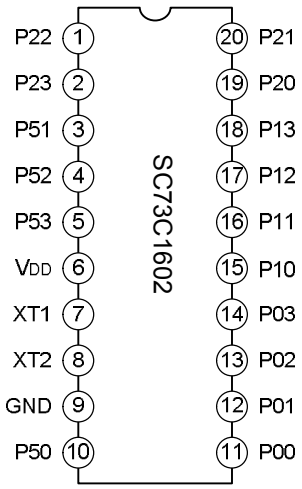
SOP-20/SSOP-20 Pin Layout Format 2



SOP-16 Pin Layout Format 2



SOP-20/SSOP-20 Pin Layout Format 3

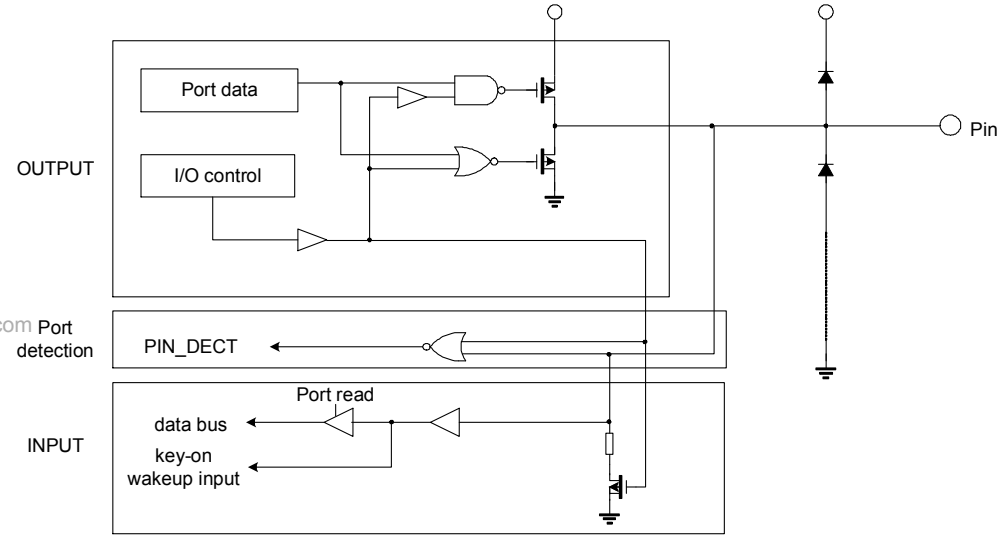


PIN DESCRIPTION

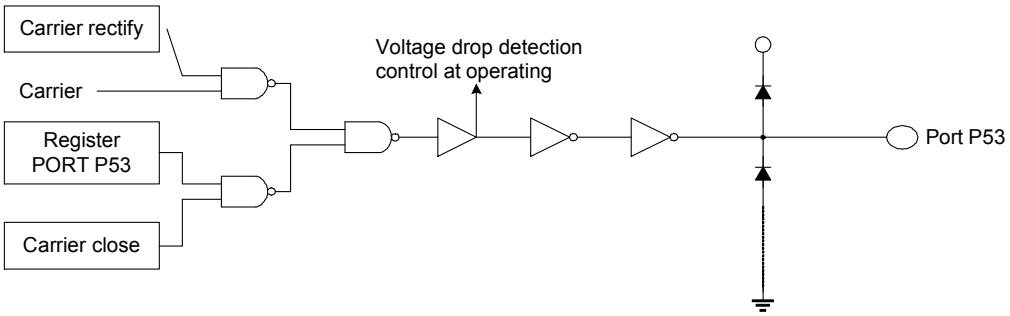
Symbol	Description
VDD	Power Supply positive
GND	Power Supply negative
RSTN	Reset pin (active low)
XT1	OSC output pin
XT2	OSC input pin
P00~P03	4-bit I/O pin. In input mode, it is used as the keyboard-scan input port (with internal pull-down resistor). In output mode, it is used as the keyboard-scan output port.
P10~P13	Same as P00-P03
P20~P23	Same as P00-P03
P50-P52	Same as P00-P03
P53	Outputs remote control signal with carrier.

Note: The package of the IC is to be determined by customer.

PORT BLOCK DIAGRAMS



P0, P1, P2, P50, P51, P52 Configuration



P53 configuration

Note: The I/O mode of P0, P1, P2 , P5 port refer to the PR register.

FUNCTION DESCRIPTION

1. PC

PC refers to the program counter, 11 bits. The maximum addressing area is 2K ROM .The program counter contains the address of the instruction that will be executed next. The PC value is cleared to 0 after reset. The PC is set to predefined value when one of the 3 following occasions occurs: 1) when the JUMP instruction is executed; 2) when a subroutine call is back; 3) when a program call is back. In the SC73C1602, all instructions are one-byte OP Code instructions, so generally PC increments by 1 each time an instruction is executed.

2. MBR

Memory buffer register (MBR) is the write-only, higher 4-bit of the program pointer. The ROM of SC73C1602 can be divided into 16 blocks. Each block has 128 bytes. These blocks can be addressed by the MBR. When the program starts executing a branch instruction, it must load the corresponding value to the MBR register, and then executes the command BSS label.

3. STACK

Stack register stores the previous value of program pointer during execution of subroutine calls, 11 bits. Because there is two-level hardware stack registers, two-level programs can be called. When the user tries to make a nested two-level program call, an error will occur.

4. B, H, D

Lower 3-bit of register B and all bits (4-bit) of H, D (ROM address is formed according to BHD order) are used as pointers pointing to data table when accessing data in ROM whose space of 2K can be used for data table, otherwise, register H, D act as general purpose register as others. Data lookup in ROM automatically whose 11-bit address is decided by lower 3-bit of register B and all bits of register H & D, is available through corresponding instructions.

5. ROM

Address	2K x 9 bits
000H	
001H	
002H ⋮ 01FH	Subroutine call start address
020H ⋮ 7FFH	Program address or Table data

6. CH0, CH1, CL0, CL1

CH0, CH1, CL0 and CL1 are carrier level control registers for controlling the high and low level to （CH＋1）/fosc and（CL＋1）/fosc.

7. LL, LH

LL register, 4 bits, LH register, 1 bit. LH[0]LL[3:0] is the address pointer of RAM.

8. RAM

Data memory consists of 32x4 bits and is used to store temporary data and results after a program is executed. It can address the entire RAM areas by the pointer LH[0]LL[3:0]. When reset, the contents of RAM are not defined. We recommend users to initialize it at the beginning of their software program.

9. ALU

The arithmetic and logic unit plays a leading role in performing various operations of 4-bit binaries. The operation of ALU will change the carry flag (CF) and the zero flag (ZF).

10.Acc

4-bit accumulator, it is mostly used to store data and results.

11.CF

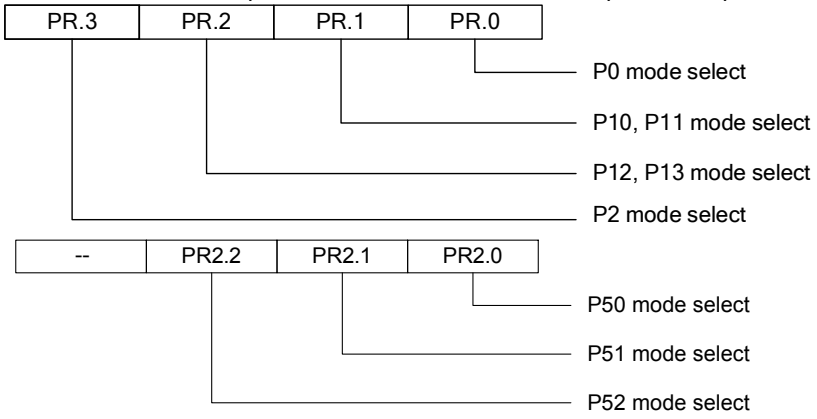
Carry flag.

12.SF

Status flag bit, the value of SF is 1 after reset.

13.PR (PR , PR2)

The port mode register, which specifies the input mode or output mode of the I/O port, is 4-bit write-only. When PR=1, the corresponding port is set to output mode. PR=0, it is set to input mode. The execution of the HOLD instruction won't affect the I/O modes of operation. When reset, PR=0. The port is in input mode.



14.PORT

SC73C1602 has 4 groups of I/O ports, totally 16 pins. Each group can operate in both input and output mode (except P53). Details are as follows:

P0 port: P00-P03, 4-bit input/output port. The PR1.0 determines the port operation mode. In input mode, it has an internal pull-down resistor and can be used for keyboard scan input. When the input level is high, it can release the HOLD mode. In output mode, it can be used for keyboard scan output.

P1 port: P10-P13, same as P0 port, PR1.1 determines the port operation mode.

P2 port: P20-P23, same as P0 port, PR1.2 determines the port operation mode.

P5 port: P50-P52, same as P0 port.

P53: large current output port, this pin is used to output infrared remote signal. If P53 is set to 1, this pin outputs modulated signal with carrier. If it is set to 0, it outputs low level voltage.

15. Timer/counter

SC73C1602 has two internal timers:

One is a 17-bit timer. The clock source of the timer is main frequency (fmain) of the circuit. There are timing steps from 10 (which generates pulses with frequency fmain/2^{10}) to 15 (fmain/2^{15}). The timer can output pulse frequency ranging from fmain/2^{10} to fmain/2^{15}, and can be used for timer after releasing the HOLD mode. It can also be used as a WDT. After the HOLD mode released and the timer reset instruction TMRST executed, the timer value is cleared.

The other timer is a carrier generator. Setting different length of high and low level time span respectively through programming, it generates various different duty and frequency carriers.

16. TR

Timer register, it selects the status of the timer mode, 4-bit write-only. SC73C1602 has no special instructions to read the register, so it uses the following instructions: LD A, TM or LD @LL, TM.

3	2	1	0
IBNS	TIBS		

TR timer register

17. IBNS

The control bit of the read timer. When the value is 0, it reads TM3 (IT3), and IT2~IT0 become 0. When the value is 1, it reads 4-bit data TM3~TM0(IT3~IT0).

TM3: 2^{15}/fmain

TM2: 2^{14}/fmain

TM1: 2^{13}/fmain

TM0: 2^{12}/fmain

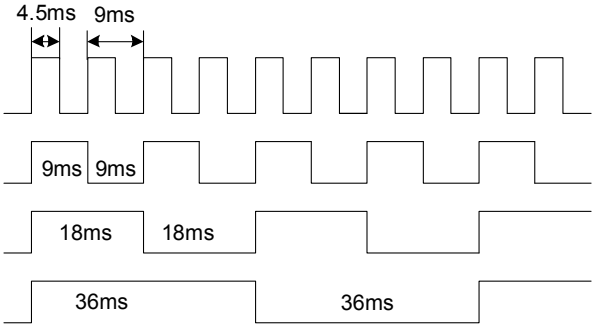
Example: when the crystal oscillator select 455KHz, the corresponding time of port P50 is 2^{12}÷455≈9ms. This means the time from TM=1111B to 1101 is 9ms, and the time from TM=1111B to 1110 is 4.5ms.See the following program:

```
LD      A#1000B
LD      TM,A
TMRST
```

```
        ......
        LD      L,#TEMP
        LD      @LL,#1110B
LOOP:   LD      A,TM
        XOR     A,@LL
        JMPS    LOOP
        END
```

In above program, the time from TMRST start to END is 4.5ms, that it from TM=1111B to 1110B is 4.5ms..

Time change :



The maximum adjustable time of the timer is 2^{16}/fmain. When the timer acts as a WDT and the timer is activated, it must execute the TMRST instruction and clear the timer in 2^{16}/fmain's time, otherwise, it will lead the WDT to overflow, and causes the MCU to reset.

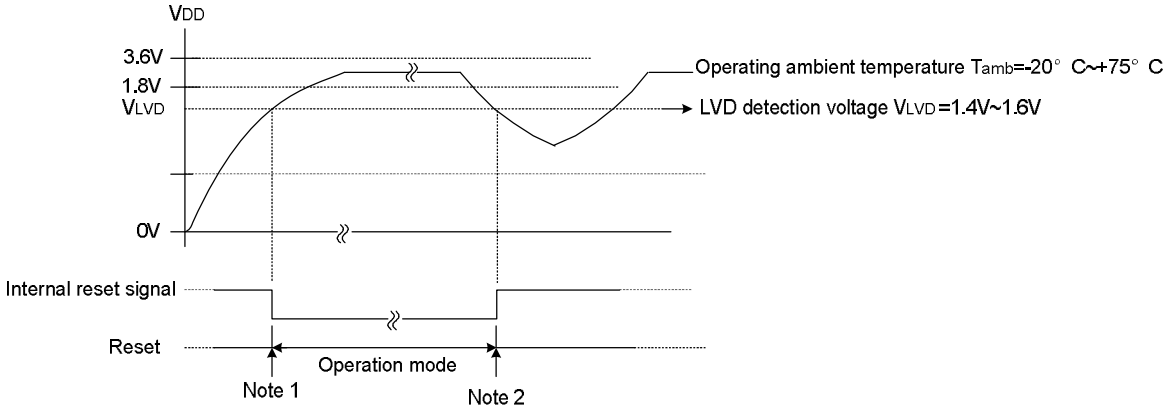
18. LVD Circuit

The LVD circuit monitors the power supply voltage and applies an internal reset to the micro-controller.

The LVD circuit has the following functions:

- Generates an internal reset signal when $V_{DD} \leq V_{LVD}$（note 1）.
- Cancels an internal reset signal when $V_{DD} > V_{LVD}$.

Where, V_{DD}: power supply voltage. V_{LVD}: LVD detection voltage.



Notes. 1. Actually, there is a short oscillation stabilization wait time before the circuit is in operation mode. The oscillation stabilization wait time is about 216/fmain.

2. The LVD circuit generates an internal reset signal when the power supply voltage has fallen. When the circuit is sending code, it will cause a large current. When using old batteries (high resistor), battery output voltage will drop. When the output voltage is lower than a reference value, the

oscillator will stop. This causes system to malfunction. In this condition, the system will initiate the LVD circuit to generate an internal reset signal to remove the malfunction.

19.Instruction Cycle

Instructions and internal operations are executed in synchronization with the main clock. The minimum unit of instruction is called the instruction cycle. SC73C1602 has 1 and 2-cycle OP Code instructions.
An instruction cycle consists of 5 states (STCLK1 – STCLK5). Each state consists of 1 main clock. Therefore, the instruction cycle time is 5/fmain [s].

20.The Carrier

1. fcarry is the output carrier frequency. Fin is the input frequency of the carrier generator (a register concerned with the settings of the carrier). It is also the oscillation frequency of the IC.
2. fcarry = Fin / (CH+CL+2). For example, 38.10(105) at Fin =4000KHz, 38.10 mean the carrier frequency that can be achieved under certain conditions, If CH + CL + 2 = 105, the generated carrier frequency is 38.10KHz.
3. CH: the register that determines the duration of the high level carrier, the duration of the high level carrier is: (CH + 1) / Fin .
4. CL: the register that determines the duration of the low level carrier, the duration of the low level carrier is : (CL + 1) / Fin .

INSTRUCTION SETS

1. Transmit instruction

Instruction	Operation	CF	SF	Cycle
LD A, LL	A ← LL	---	1	2
LD A, LH	A ← LH	---	1	2
LD A, B	A ← B	---	1	2
LD A, H	A ← H	---	1	2
LD A, D	A ← D	---	1	2
LD A, @LL	A ← RAM(LL)	---	1	1
LD A, #k	A ← k	---	1	1
LD CL1, A	CL1 ← A	---	1	2
LD CL0, A	CL0 ← A	---	1	2
LD CH1, A	CH1 ← A	---	1	2
LD CH0, A	CH0 ← A	---	1	2
LDH A, @BD	A ← ROM(BD)7-4	---	1	2
LDL A, @BD	A ← ROM(BD)3-0	---	1	2
LDS A, @BD	A ← ROM(BD)8	---	1	2
LDH @LL, @BD	RAM(LL) ← ROM(BD)7-4	---	1	2
LDL @LL, @BD	RAM(LL) ← ROM(BD)3-0	---	1	2
LDS @LL, @BD	RAM(LL) ← ROM(BD)8	---	1	2
LD LL, A	LL ← A	---	1	2
LD LH, A	LH ← A	---	1	2
LD LL, #k	LL ← k	---	1	1
LD @LL, A	RAM(LL) ← A	---	1	1
LD @LL, #k	RAM(LL) ← k	---	1	1
LD D, A	D ← A	---	1	2
LD H, A	H ← A	---	1	2
LD B, A	B ← A	---	1	2
LD PR, A	PR ← A	---	1	2
LD PR2, A	PR2 ← A	---	1	2
LD TM, A	TM ← A	---	1	2
LD A, TM	A ← TM	---	1	2

1. LD A, LL — Load values in the LL register to the accumulator.
2. LD A, LH — Load values in the LH register to the accumulator.
3. LD A, D — Load values in the D register to the accumulator.
4. LD A, H — Load values in the H register to the accumulator.
5. LD A, B — Load values in the B register to the accumulator.
6. LD A, @LL — Load the contents of RAM pointed at by the LL (LL & LH) register to accumulator.
7. LD A, #k — Load the 4 bit immediate K to accumulator.
8. LDL A, @BD — Load the lower 4 bit of ROM data pointed at by the BHD to accumulator.

9.	LDH A, @BD	Load the higher 4 bit of ROM data pointed at by the BHD to accumulator.
10	LDS A, @BD	Load the highest 1 bit of ROM data pointed at by the BHD to accumulator
11	LDL @LL, @BD	Load the lower 4 bit of ROM data pointed at by the BHD to RAM pointed at by the LL register.
12	LDH @LL, @BD	Load the higher 4 bit of ROM data pointed at by the BHD to RAM pointed at by the LL register.
13	LDS @LL, @BD	Load the highest 1 bit of ROM data pointed at by the BHD to RAM pointed at by the LL register.
14	LD LL, A	Load the contents of the accumulator to the LL register.
15	LD LH, A	Load the contents of the accumulator to the LH register.
16	LD LL,#K	Load immediate K to the LL register.
17	LD @LL, A	Load the content of the accumulator to the RAM pointed at by the LL register.
18	LD @LL, #k	Load the immediate K to RAM pointed at by the LL register.
19	LD D, A	Load the content of the accumulator to the D register.
20	LD H, A	Load the content of the accumulator to the H register.
21	LD B, A	Load the content of the accumulator to the B register.
22	LD CL1, A	Load the content of the accumulator to the CL1 register.
23	LD CL0, A	Load the content of the accumulator to the CL0 register.
24	LD CH1, A	Load the content of the accumulator to the CH1 register.
25	LD CH0, A	Load the content of the accumulator to the CH0 register.
26	LD PR, A	Load the content of the accumulator to the port register(PR).
27	LD PR2, A	Load the content of the accumulator to the port register(PR2).
28	LD TM, A	Load the content of the accumulator to the timer register.
29	LD A, TM	Load the content of the timer register to the accumulator.

Execution the above transmit instructions will not affect the carry flag, and the status flag remains 1.

2. Input/output instructions

Instruction	Operation	CF	SF	Cycle
LD A, %p	A ← PORT(p)	---	/Z	2
LD @LL, %p	RAM(LL) ← PORT(p)	---	/Z	2
LD %p, A	PORT(p) ← A	---	1	2
LD %p, @LL	PORT(p) ← RAM(LL)	---	1	2

a.	LD A, %P	Move the value of port(P) to the accumulator
b.	LD @LL, %p	Move the value of port(P) to RAM pointed at by the LL register.
c.	LD %p, A	Move the contents of the accumulator to port (P).
d.	LD %p, @LL	Load the contents of RAM pointed at by the LL register to port(P).

The above four input/output instructions are used mostly for port operation, the two read instructions will affect the status flag SF.

3. Arithmetic and logical instructions

Instruction	Operation	CF	SF	Cycle
ADD A, @LL	A ← A+RAM(LL)	---	/C	1
ADDC A, @LL	A ← A+RAM(LL)+CF	C	/C	1
ADD A, #k	A ← A+k	---	/C	1
ADD LL, #k	LL ← LL+k	---	/C	2
SUBRC A, @LL	A ← RAM(LL)-A-/CF	C	C	1
INC @LL	RAM(LL) ← RAM(LL)+1	---	/C	1
DEC @LL	RAM(LL) ← RAM(LL)-1	---	C	1
INC LL	LL ← LL+1	---	/C	2
INC LH	LH ← LH+1	---	/C	2
DEC LL	LL ← LL-1	---	C	2
DEC LH	LH ← LH-1	---	C	2
INC D	D ← D+1	---	/C	2
INC H	H ← H+1	---	/C	2
INC B	B ←B+1	---	/C	2
DEC D	D ← D-1	---	C	2
DEC H	H ← H-1	---	C	2
DEC B	B ← B-1	---	C	2
AND A, @LL	A ← A&RAM(LL)	---	/Z	1
OR A, @LL	A ← A | RAM(LL)	---	/Z	1
XOR A, @LL	A ← A^RAM(LL)	---	/Z	1

1. ADD A, @LL — Add the contents of RAM pointed at by the LL to accumulator, store the sum in the ACC. This operation will affect SF, SF=/CF.
2. ADDC A, @LL — Add the contents of RAM pointed at by the LL register to accumulator with carry. Store the carry bit in the CF. This operation will affect SF, SF=/CF.

3. ADD A,#K — Add immediate K to accumulator. Store the sum in the ACC. This will affect SF, SF=/CF.
4. ADD L,#K — Add immediate K to the LL register. Store the sum in the LL. This will affect SF, SF=/CF.
5. SUBRC A, @LL — Subtract instruction with borrow(the complement of carry). Subtract the contents of the accumulator from the contents of RAM pointed at by the LL register, subtract the complement of the carry bit, then store the results in the accumulator, transfer the carry bit to the CF, this will affect SF and CF, SF=CF.
6. INC @LL — Increment instruction. Increment the contents of RAM pointed at by the LL register by 1. This will affect SF, SF=/CF.
7. DEC @LL — Decrement instruction. Decrement the contents of RAM pointed at by the LL register by 1. This will affect SF, SF=CF.
8. INC D — Increment instruction. Increment the contents of the D register by 1. This will affect SF, SF=/CF.
9. INC H — Increment instruction. Increment the contents of the H register by 1. This will affect SF, SF=/CF.

10.	INC B	Increment instruction. Increment the contents of the B register by 1. This will affect SF, SF=/CF.
11.	DEC D	Decrement instruction. Decrement the contents of the D register by 1. This will affect SF, SF=CF.
12.	DEC H	Decrement instruction. Decrement the contents of the H register by 1. This will affect SF, SF=CF.
13.	DEC B	Decrement instruction. Decrement the contents of the B register by 1. This will affect SF, SF=CF.
14.	INC LL	Increment instruction. Increment the contents of the LL register by 1. This will affect SF, SF=/CF.
15.	INC LH	Increment instruction. Increment the contents of the LH register by 1. This will affect SF, SF=/CF.
16.	DEC LL	Subtract 1 from the content in register LL. SF is affected, SF=/CF.
17.	DEC LH	Subtract 1 from the content in register LH. SF is affected, SF=/CF.
18.	AND A, @LL	The contents of the accumulator and RAM pointed at by the LL register are ANDed and the results are stored in the accumulator. SF changed, SF=/Z.
19.	OR A, @LL	The contents of the accumulator and RAM pointed at by the LL register are ORed and the results are stored in the accumulator. SF changed, SF=/Z.
20.	XOR A,@LL	The contents of the accumulator and RAM pointed at by the LL register are XORed and the results are stored in the accumulator. SF changed, SF=/Z.

4. Bit operation instructions

Instruction	Operation	CF	SF	Cycle
CLR @LL, b	RAM(LL)b←0	---	1	2
SET @LL, b	RAM(LL)b←1	---	1	2
TEST @LL, b	SF←/RAM(LL)b	---	*	2

a.	CLR @LL, b	Clear the B-bit of the RAM pointed at by the LL register.
b.	SET @LL, b	Set the B-bit of the RAM pointed at by the LL register to be 1.
c.	TEST @LL, b	Test the B-bit of the RAM pointed at by the LL register. If this bit is1, the SF is set to 0; otherwise, the SF is set to 1.

5. Carry operation instructions

Instruction	Operation	CF	SF	Cycle
CLR CF	CF←0	0	1	2
SET CF	CF←1	1	1	2
TESTP CF	SF←CF	---	*	1

a.	CLR CF	Clear the carry flag to logic zero.
b.	SET CF	Set the carry flag to logic 1.
c.	TESTP CF	Test the carry flag, send the carry flag to SF.

6. Branch instructions

Instruction	Operation	CF	SF	Cycle
BSS label		---	1	2
JMPS label		---	1	3

Jump instruction is active only when SF is 1, or else next instruction is executed. Please read the *Pseudo-instruction Set* for details.

BSS label Jump to destination address label with range of 128 bytes

JMPS label Jump to destination address label with range of 2K program.

Symbol description of above instructions:

a. label Destination address of jump
b. #k Immediate (0~15)
c. b Bit addressing (0~3)
d. %p Port address

7. Subroutine instructions

Instruction	Operation	CF	SF	Cycle
CALLS label		---	---	2
RET		---	---	2

When executing subroutine call and return instructions, the subroutine starting address is limited from 000H to 01FH.

8. Other instructions

Instruction	Operation	CF	SF	Cycle
HOLD		---	1	1
NOP		---	---	1
TMRST	Reset timer counter	---	---	1

a. HOLD After executing this instruction, MCU is in the power–save mode, the clock stops oscillation and power consumption reduces dramatically.
b. NOP Null operation. It doesn't affect anything.
c. TMRST Timer clear command. It will clear all values of the timer to 0. This instruction is often used to reset WDT in program.

9. Pseudoinstruction

ORG

Format:

[Label:] ORG address

Function:

Redefine following start address

Expression:

Label: selectable

Address: redefined address, can be binary, decimal or hexadecimal.

Redefined address is an absolute address which could not be returned back. That is, the redefined address

should be higher than that above, or a fault is occurred during compiling. 000H is defaulted if no address is set by ORG instruction.

Example:

ORG 0100H

EQU

Format:

Symbol EQU digital

Function:

Define a digital as a symbol. Symbol ＝ digital.

Expression:

Symbol should be legal, and digital should be binary, decimal or hexadecimal. There is no colone before EQU in definition, and it can only useful after the definition.

Example:

Data1 EQU 12H

Data2 EQU 1001B

DB

Format:

[Label:] [num] DB data

Function:

Define data with number of num.

Expression:

Label: selectable

Num: indicates number of data, default value is 1.

Data: data to be written to ROM. It should smaller than 0X200 as ROM is only 9-bit.lower 9-bit value of data is taken with warning if it is more than 0x200.(only lower 8-bit is taken if the instruction is used for data table)

Example:

DB 12H ; Define one data

DB 10010B ; Define one data

12H DB 55H ; Define continuous 18 data

JMPS

Format:

[Label:] JMPS address

Function:

Jump in ROM.

Expression:

Label: selectable

Address can be a digital, symbol defined by EQU or the address symbol.

Combined by:

LD MBR, #k

BSS label

The instruction is 2-byte long, and it can jump to any position in the ROM.

Example:

```
JMPS MAIN
JMPS 100H
```

VENT

Format:

VENT label

Function:

Define the entry and reset address of sub-program.

Expression:

Label is the sub-program name or the address symbol.

Use VENT to specify the entry and reset address of the sub-program, and it must be at the beginning of the program. The first VENT denotes the reset address and the following VENT instructions denote the entry of the sub-program. In general, 16 sub-programs can be defined at most. All the sub-programs called by CALL instruction should be defined in VENT, or else errors will occur in assembly.

Example:

```
VENT MAIN
VENT SUB1
VENT SUB2
……..
ORG 100H
MAIN:
NOP
NOP
CALLS SUB1
CALLS SUB2
```



```
……
SUB1:
……..
SUB2:
……..
```

END

Format:

END

Function:

Use the END instruction to end the assembly of a program.

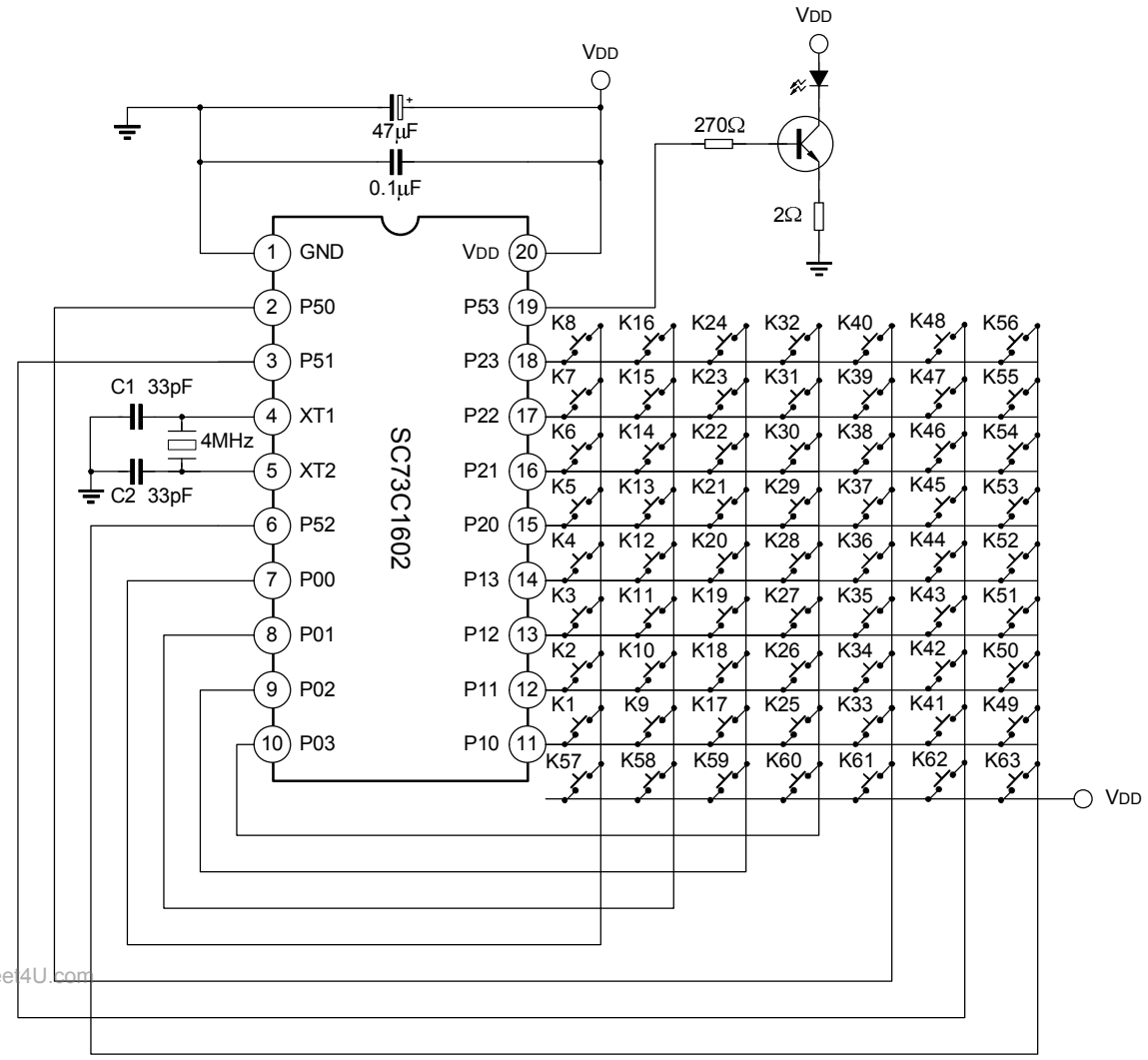
Expression:

END pseudoinstruction ends the assembly of a program and the content after END will not be processed by assembler. If END is omitted, the assembler will process all the lines of the source file.

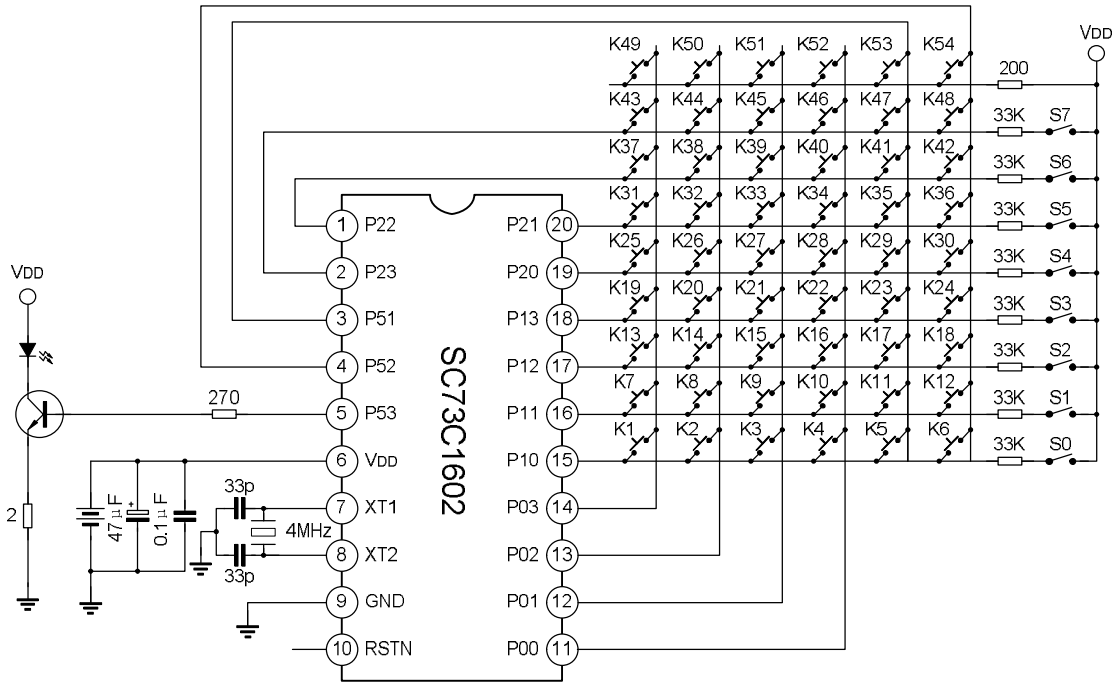
Example:

```
END
```

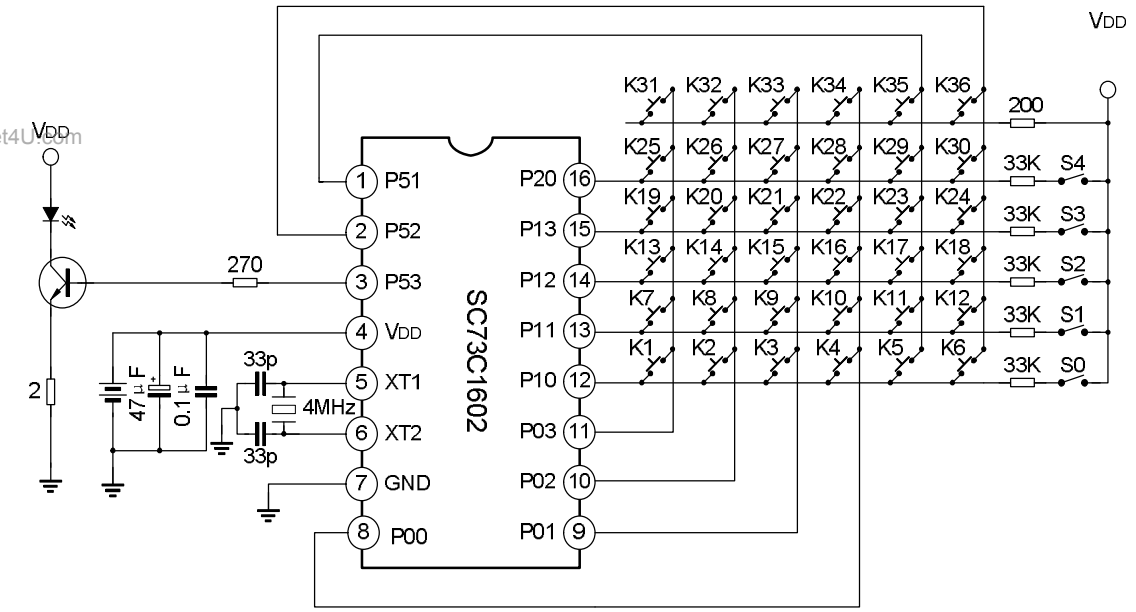
TYPICAL APPLICATION CIRCUIT (I) - REFER PIN LAYOUT FORMAT 1



TYPICAL APPLICATION CIRCUIT (II) - REFER PIN LAYOUT FORMAT 2

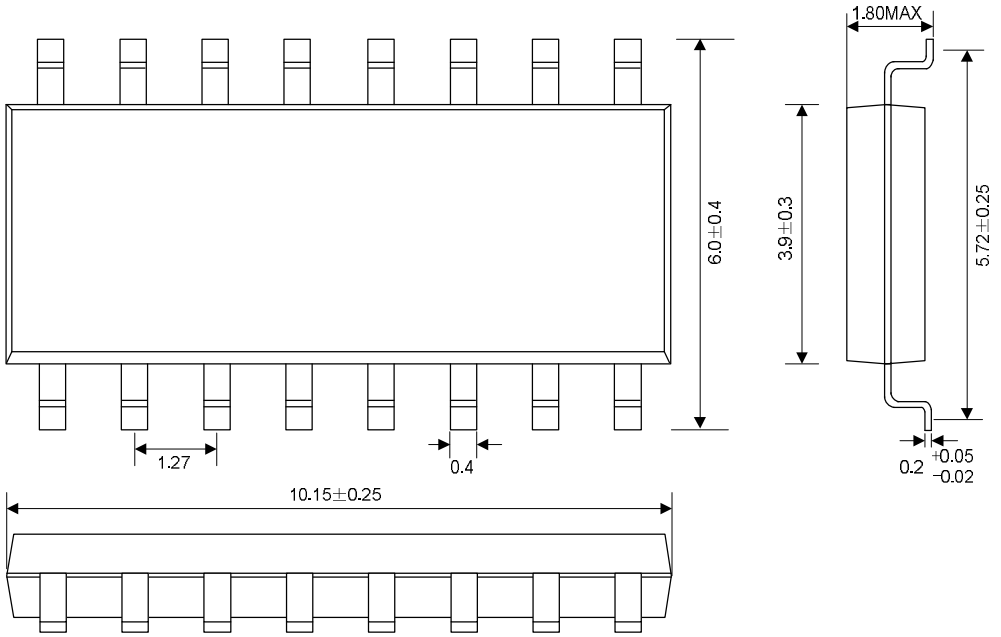


TYPICAL APPLICATION CIRCUIT (III) - REFER PIN LAYOUT FORMAT 3

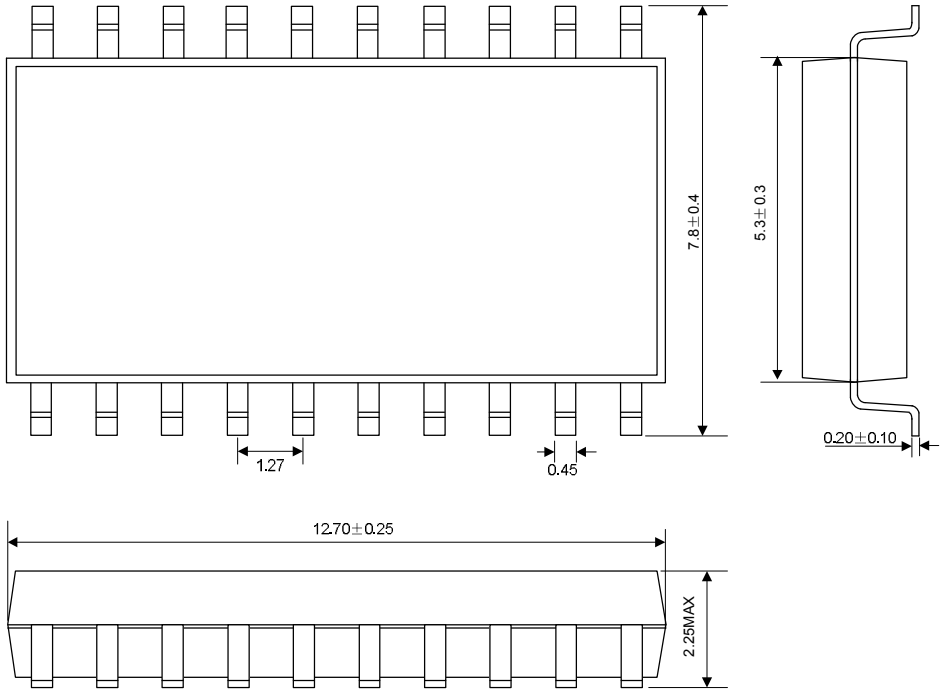


PACKAGE OUTLINE

SOP-16-225-1.27 Unit:mm

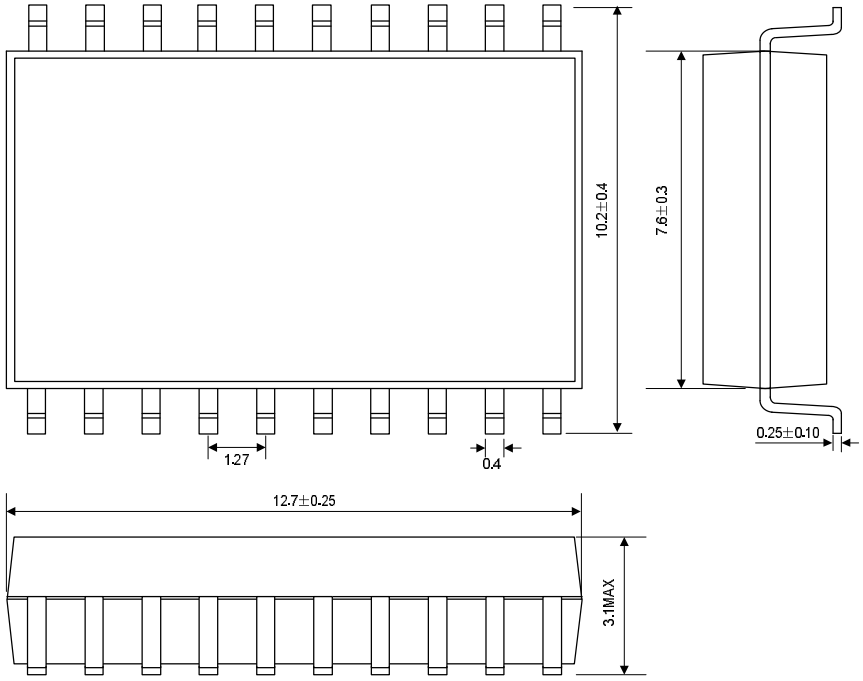


SOP-20-300-1.27 Unit: mm

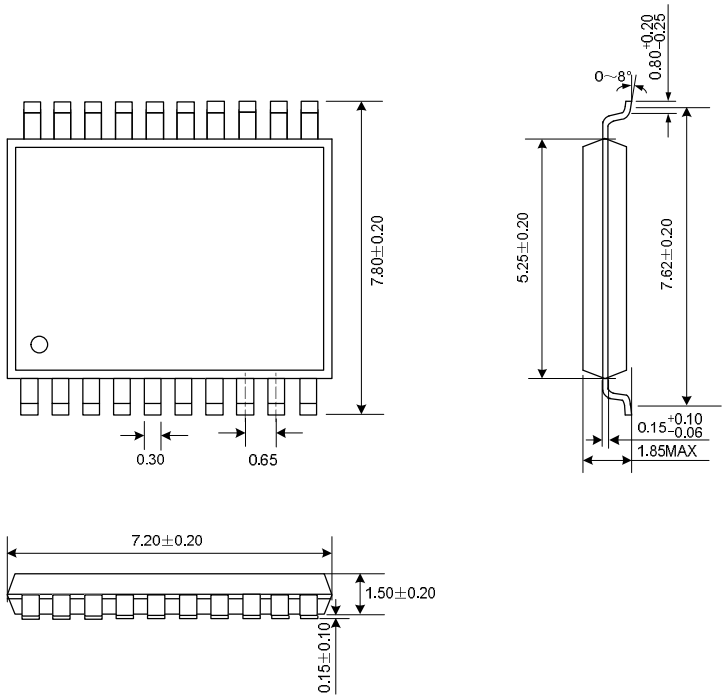


PACKAGE OUTLINE(Continued)

SOP-20-375-1.27 Unit: mm

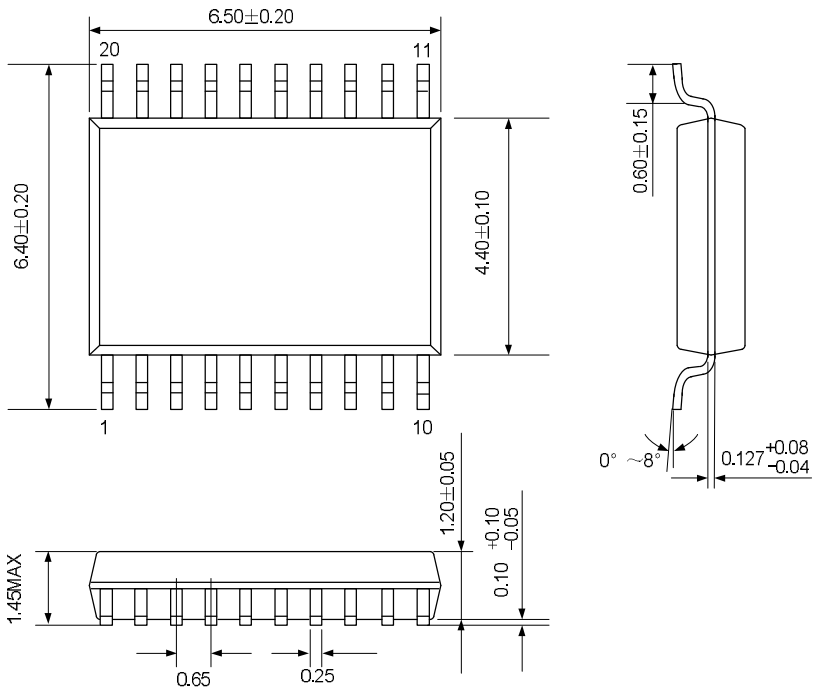


SSOP-20-300-0.65 Unit:mm



PACKAGE OUTLINE(Continued)

SSOP-20-225-0.65 Unit:mm



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

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- Silan will supply the best possible product for customers!