

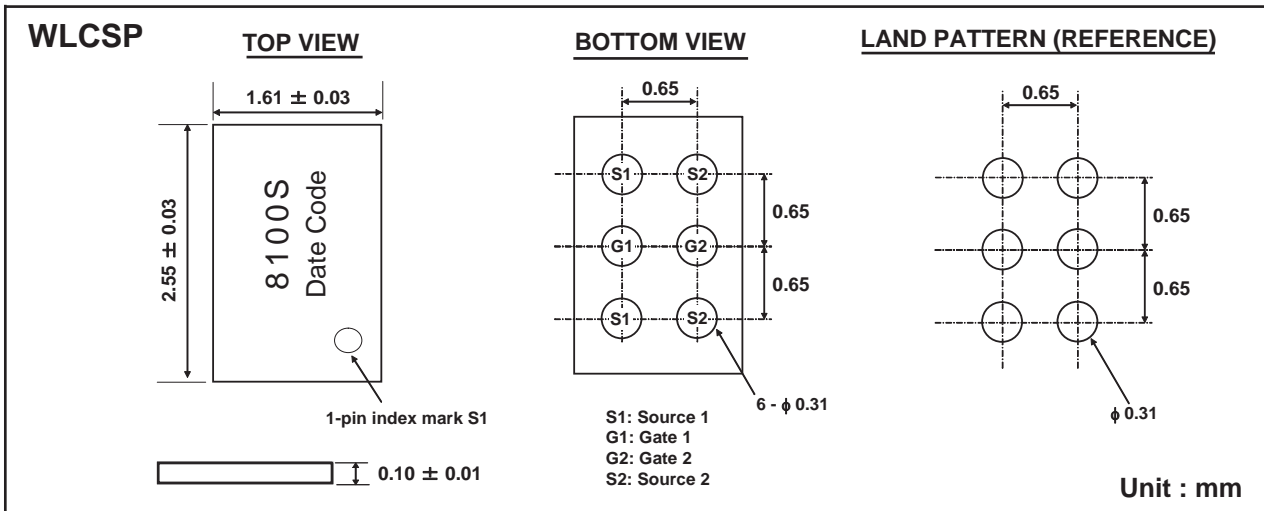


Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V _{SSS}	I _S	R _{SS(ON)} (mΩ) Typ
12V	8A	4.6 @ V _{GS} =4.5V
		4.8 @ V _{GS} =4.0V
		4.9 @ V _{GS} =3.8V
		5.7 @ V _{GS} =3.1V
		7.1 @ V _{GS} =2.5V

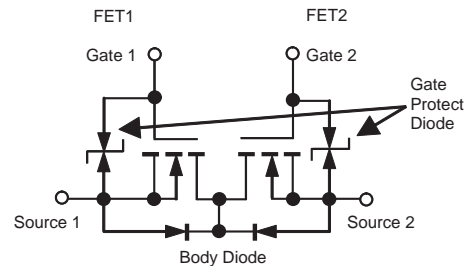
FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.



ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Symbol	Parameter	Limit	Units
V _{SSS}	Source-Source Voltage	12	V
V _{GSS}	Gate-Source Voltage	±8	V
I _S	Source Current-Continuous ^c	8	A
I _{SP}	-Pulsed ^{a c}	80	A
P _T	Total Power Dissipation	1.3	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C



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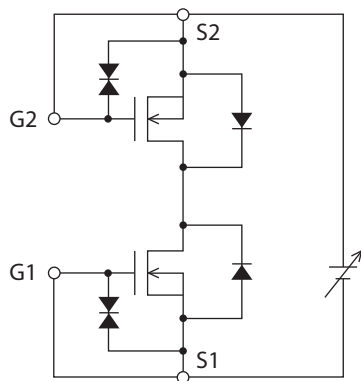
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ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

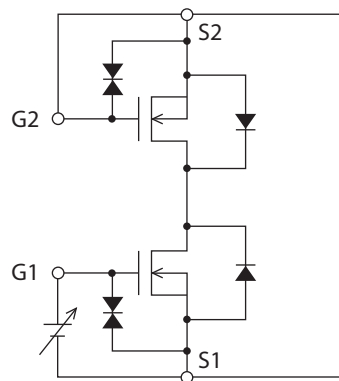
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{SSS}	Source-Source Breakdown Voltage	V _{GS} =0V , I _S =250uA	12			V
I _{SSS}	Zero Gate Voltage Source Current	V _{SS} =12V , V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±5V , V _{SS} =0V			±1	uA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{SS} =V _{GS} , I _S =1mA	0.5	0.8	1.3	V
R _{SS(ON)}	Source-Source On-State Resistance	V _{GS} =4.5V , I _S =4A	3.6	4.6	5.7	m ohm
		V _{GS} =4.0V , I _S =4A	3.7	4.8	5.9	m ohm
		V _{GS} =3.8V , I _S =4A	3.8	4.9	6.3	m ohm
		V _{GS} =3.1V , I _S =4A	4.2	5.7	7.8	m ohm
		V _{GS} =2.5V , I _S =4A	4.8	7.1	11.0	m ohm
g _{FS}	Forward Transconductance	V _{SS} =5V , I _S =4A		16		S
SWITCHING CHARACTERISTICS ^b						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =12V I _S =4A V _{GS} =4.0V R _{GEN} =6 ohm		296		ns
t _r	Rise Time			1080		ns
t _{D(OFF)}	Turn-Off Delay Time			3267		ns
t _f	Fall Time			2555		ns
Q _g	Total Gate Charge		V _{DD} =12V, I _S =4A, V _{G1S1} =4.0V		18.4	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V _{FSS}	Diode Forward Voltage	V _{GS} =0V, I _S =2A		0.77	1.2	V
Notes						
a.Pulse Test:Pulse Width ≤ 10us, Duty Cycle ≤ 1%.						
b.Guaranteed by design, not subject to production testing.						
c.Drain current limited by maximum junction temperature.						

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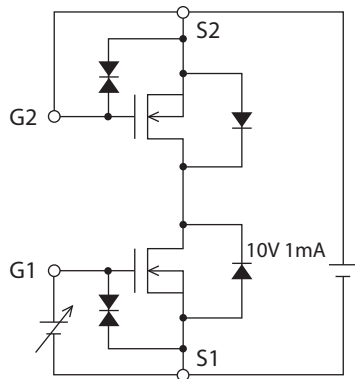
V_{SSS} / I_{SSS}



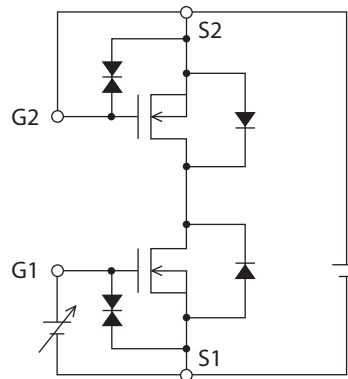
$I_{GSS} (+) / (-)$



$V_{GS} \text{ (off)}$



$|y_{fs}|$

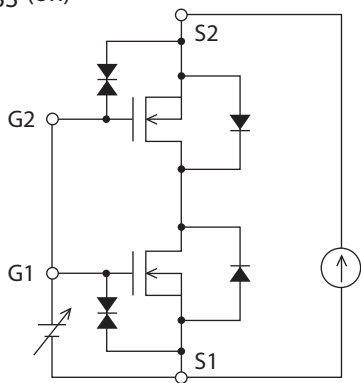


* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

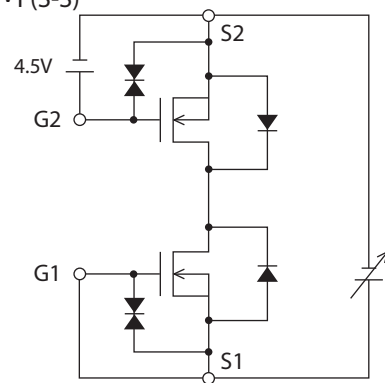
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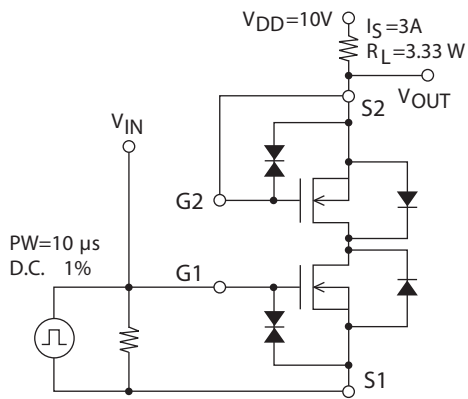
$R_{SS} \text{ (on)}$



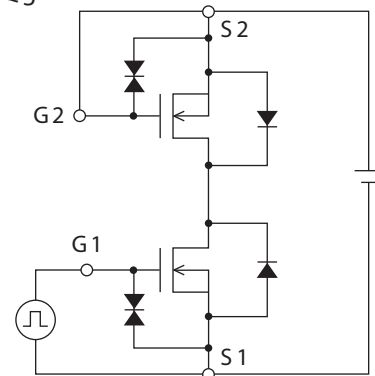
$V_F \text{ (S-S)}$



$t_d \text{ (on)}, t_r, t_d \text{ (off)}, t_f$



Q_g

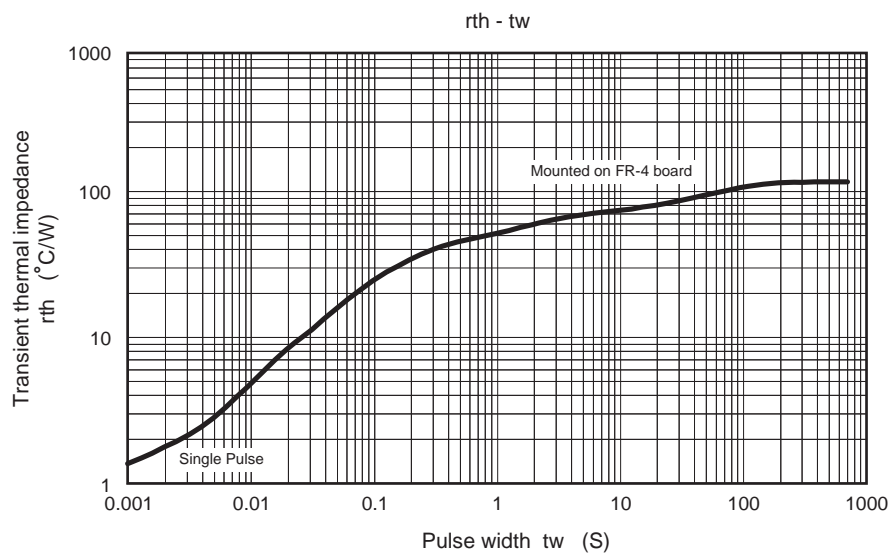
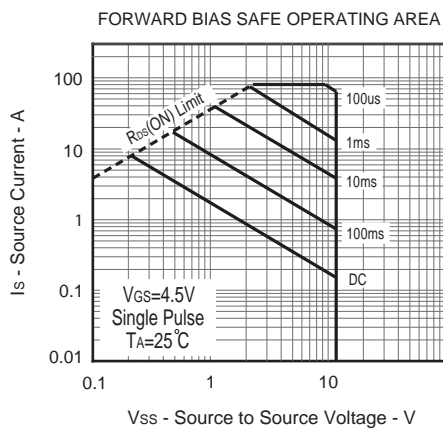
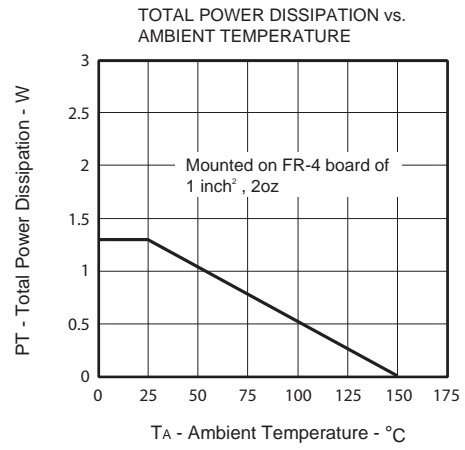
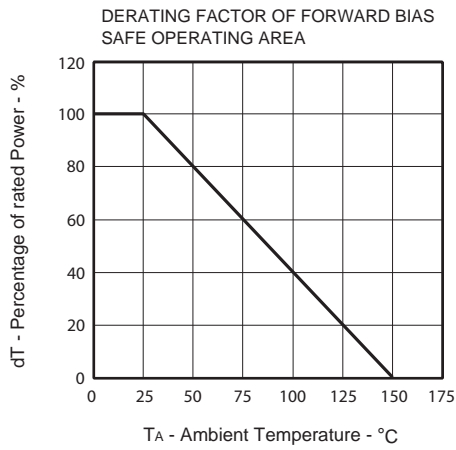


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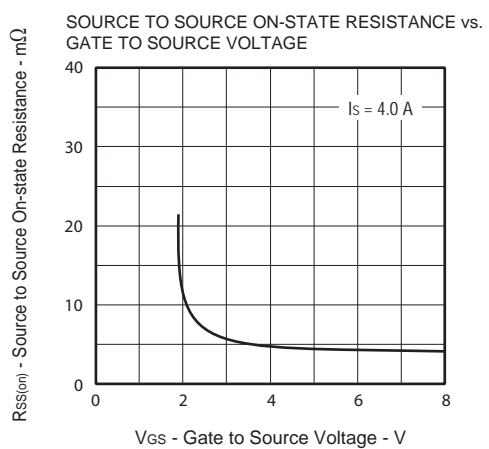
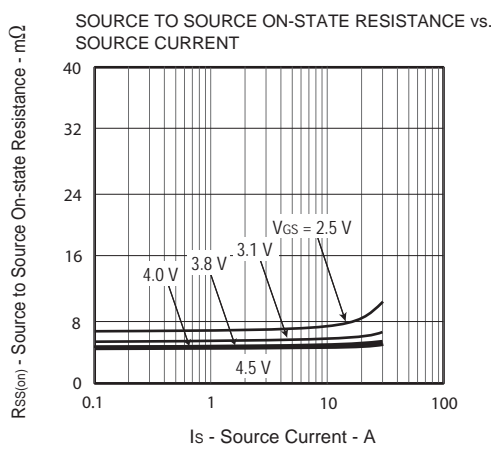
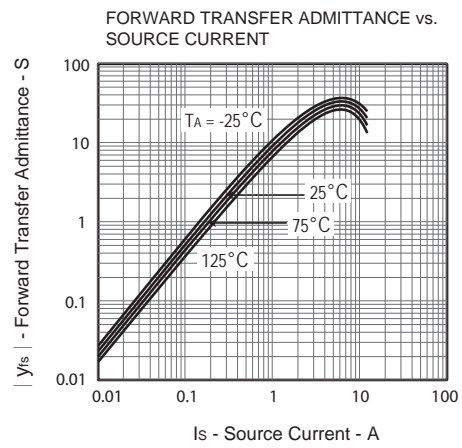
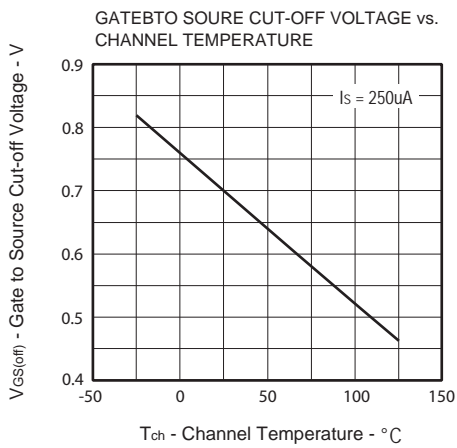
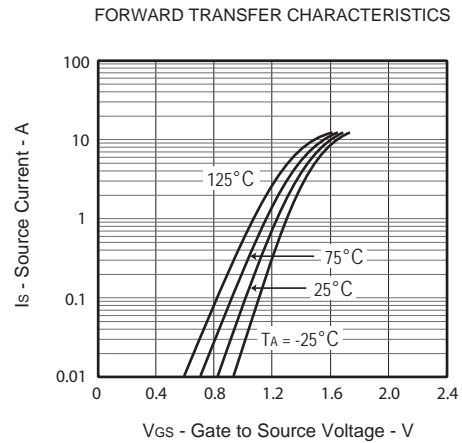
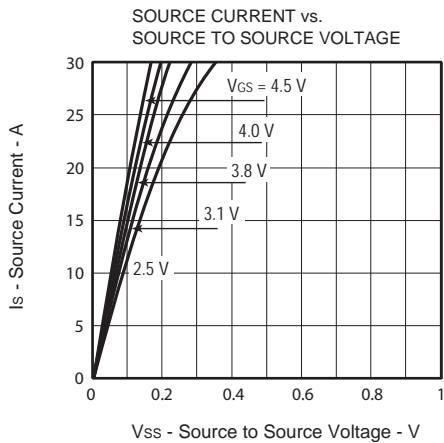
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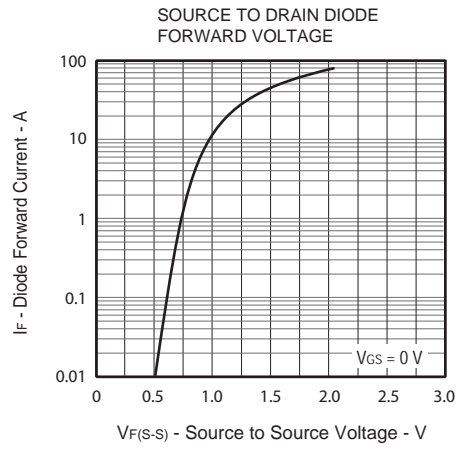
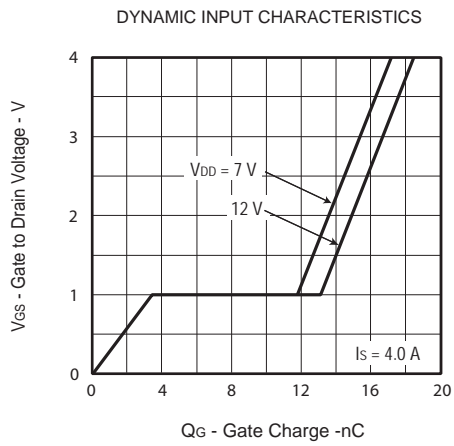
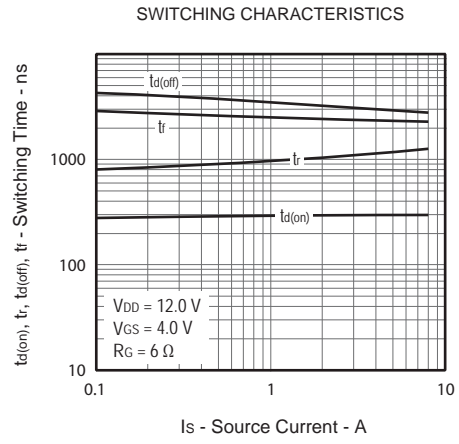
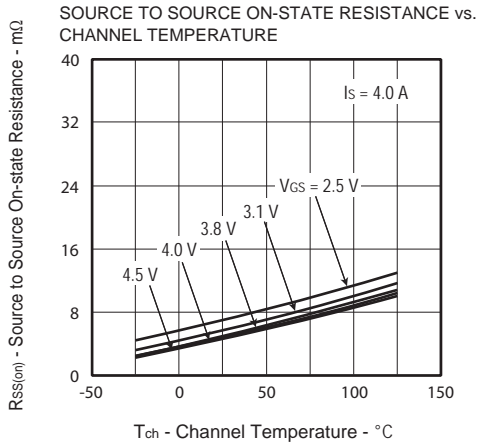
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TOP MARKING DEFINITION

