

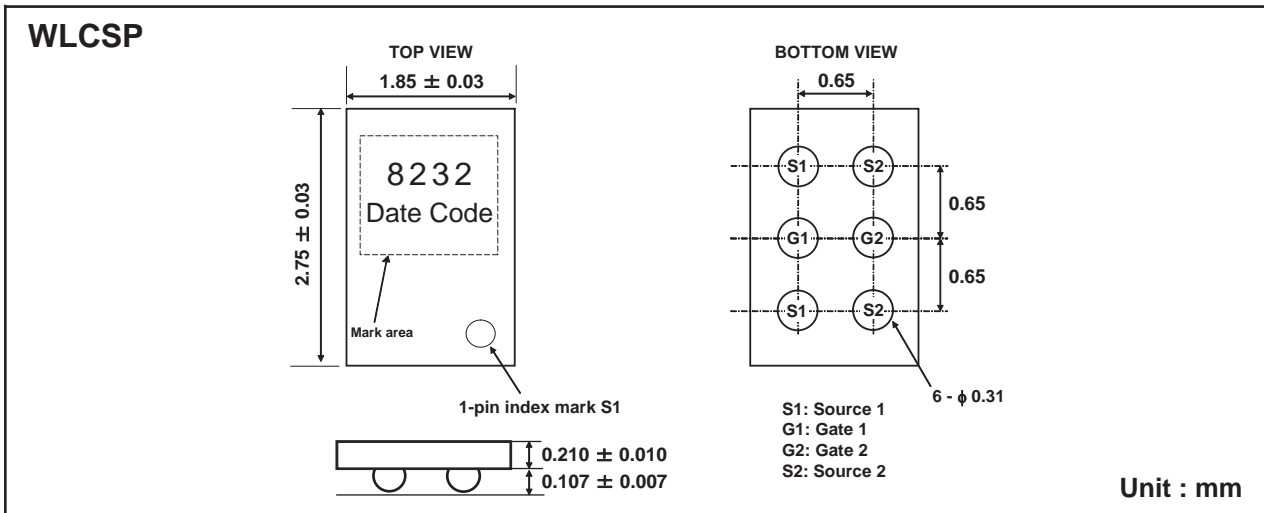


## Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>SSS</sub>	I <sub>S</sub>	R <sub>SS(ON)</sub> (mΩ) Max
20V	8A	11.0 @ V <sub>GS</sub> =4.5V
		12.0 @ V <sub>GS</sub> =4.0V
		13.0 @ V <sub>GS</sub> =3.8V
		15.0 @ V <sub>GS</sub> =3.1V
		18.0 @ V <sub>GS</sub> =2.5V

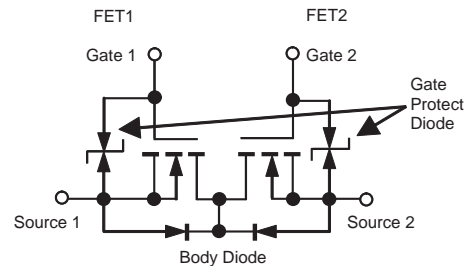
### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C)

Symbol	Parameter	Limit	Units
V <sub>SSS</sub>	Source-Source Voltage	20	V
V <sub>GSS</sub>	Gate-Source Voltage	±12	V
I <sub>S</sub>	Source Current-Continuous <sup>a</sup>	8	A
I <sub>SP</sub>	-Pulsed <sup>b</sup>	80	A
P <sub>T</sub>	Total Power Dissipation <sup>a</sup>	1.3	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C



# SC8232

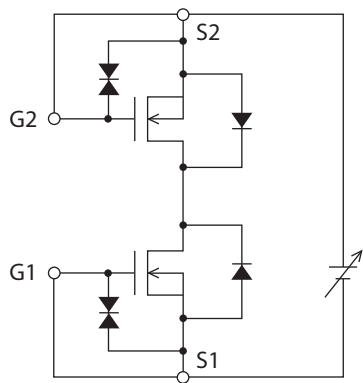
Ver 4.0

## ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

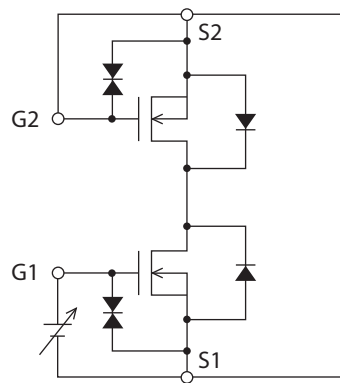
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>SSS</sub>	Source-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =250uA	20			V
I <sub>SSS</sub>	Zero Gate Voltage Source Current	V <sub>SS</sub> =20V, V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±12V, V <sub>SS</sub> =0V			±10	uA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>SS</sub> =V <sub>GS</sub> , I <sub>S</sub> =1mA	0.5	0.86	1.5	V
R <sub>SS(ON)</sub>	Source-Source On-State Resistance	V <sub>GS</sub> =4.5V, I <sub>S</sub> =3A	6.5	9.0	11.0	m ohm
		V <sub>GS</sub> =4.0V, I <sub>S</sub> =3A	7.0	10.0	12.0	m ohm
		V <sub>GS</sub> =3.8V, I <sub>S</sub> =3A	7.5	10.5	13.0	m ohm
		V <sub>GS</sub> =3.1V, I <sub>S</sub> =3A	8.0	11.5	15.0	m ohm
		V <sub>GS</sub> =2.5V, I <sub>S</sub> =3A	9.5	13.0	18.0	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>SS</sub> =5V, I <sub>S</sub> =3A		14		S
<b>DYNAMIC CHARACTERISTICS <sup>c</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>SS</sub> =10V, V <sub>GS</sub> =0V f=1.0MHz		660		pF
C <sub>OSS</sub>	Output Capacitance			340		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			120		pF
<b>SWITCHING CHARACTERISTICS <sup>c</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =20V I <sub>S</sub> =3A V <sub>GS</sub> =4.0V R <sub>GEN</sub> =6 ohm		336		ns
t <sub>r</sub>	Rise Time			1176		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			3820		ns
t <sub>f</sub>	Fall Time			2970		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =20V, I <sub>S</sub> =6A, V <sub>G1S1</sub> =4.0V		20.5		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>FSS</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =1.5A		0.77	1.2	V
<b>Note</b> a. Mounted on FR4 board of 25.4mm x 25.4mm x 1.6mm. b. Pulse Test: Pulse Width < 10us, Duty Cycle < 1%. c. Guaranteed by design, not subject to production testing.						

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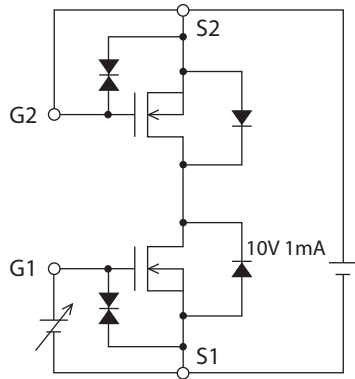
$V_{SSS} / I_{SSS}$



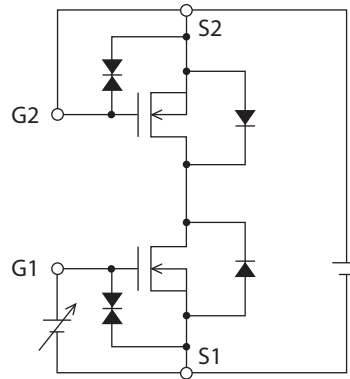
$I_{GSS} (+) / (-)$



$V_{GS} \text{ (off)}$

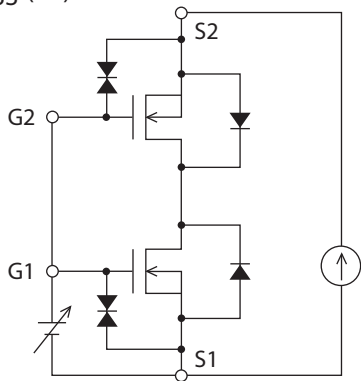


$|y_{fs}|$

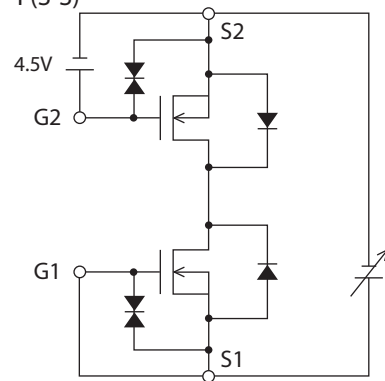


\* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

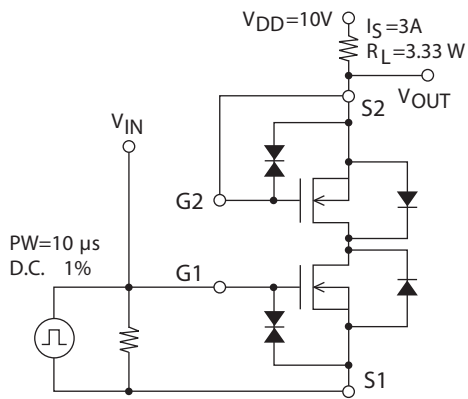
$R_{SS}(\text{on})$



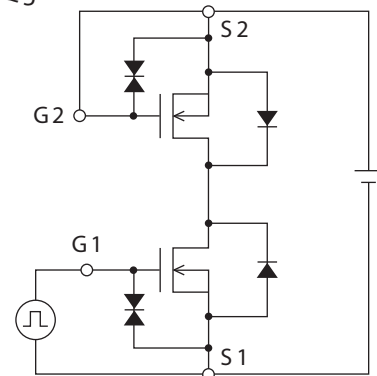
$V_F(S-S)$



$t_d(\text{on}), t_r, t_d(\text{off}), t_f$



$Q_g$



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## TOP MARKING DEFINITION

