

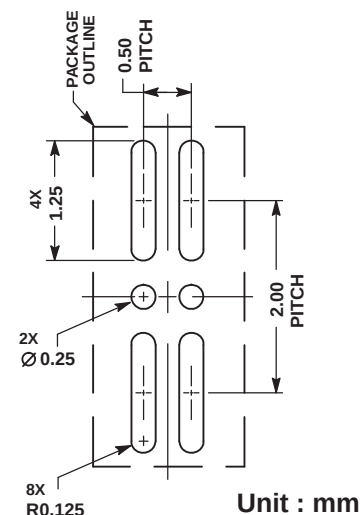
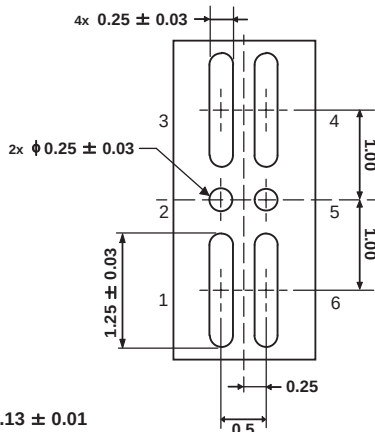


Ver 1.0

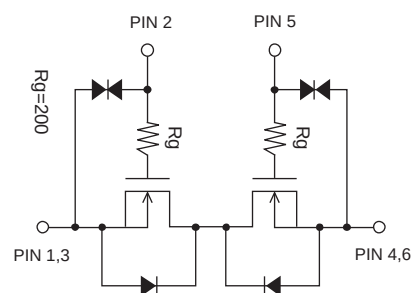
Dual N-Channel Enhancement Mode Field Effect Transistor

VSSS	IS	RSS(ON) (mΩ) Typ
20V	18A	4.2 @ VGS=4.5V
		4.3 @ VGS=4.0V
		4.4 @ VGS=3.8V
		4.9 @ VGS=3.1V
		5.6 @ VGS=2.5V

- Super high dense cell design for low Rds(ON).
- Rugged and reliable.
- Wafer level CSP.
- ESD Protected.



Symbol	Parameter	Limit	Units
V _{SSS}	Source-Source Voltage	20	V
V _{GSS}	Gate-Source Voltage	±8	V
I _S	Source Current-Continuous ^a	18	A
I _{SP}	-Pulsed ^b	100	A
P _T	Total Power Dissipation ^a	2.5	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C



PIN 1 : Source 1
PIN 2 : Gate 1
PIN 3 : Source 1
PIN 4 : Source 2
PIN 5: Gate 2
PIN 6 : Source 2

SC8605S

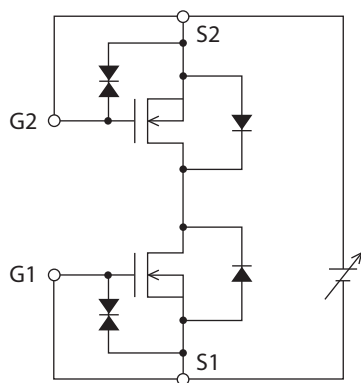
Ver 1.0

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

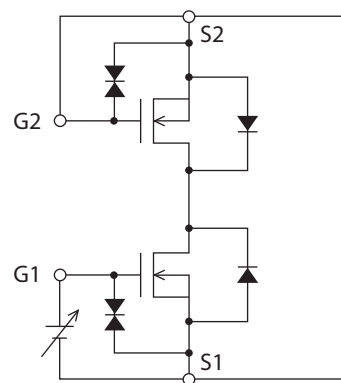
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{SSS}	Source-Source Breakdown Voltage	V _{GS} =0V, I _S =1mA	20			V
I _{SSS}	Zero Gate Voltage Source Current	V _{SS} =20V, V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±8V, V _{SS} =0V			±1	uA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{SS} =V _{GS} , I _S =1mA	0.5		1.3	V
R _{SS(ON)}	Source-Source On-State Resistance	V _{GS} =4.5V, I _S =4.5A	3.3	4.2	5.1	m ohm
		V _{GS} =4.0V, I _S =4.5A	3.4	4.3	5.2	m ohm
		V _{GS} =3.8V, I _S =4.5A	3.5	4.4	5.3	m ohm
		V _{GS} =3.1V, I _S =4.5A	3.9	4.9	6.4	m ohm
		V _{GS} =2.5V, I _S =4.5A	4.4	5.6	7.9	m ohm
g _{FS}	Forward Transconductance	V _{SS} =5V, I _S =4.5A		19		S
SWITCHING CHARACTERISTICS ^c						
t _{D(ON)}	Turn-On Delay Time	V _{SS} =20V I _S =4.5A V _{GS} =4.5V		80		ns
t _r	Rise Time			570		ns
t _{D(OFF)}	Turn-Off Delay Time			38000		ns
t _f	Fall Time			17700		ns
Q _g	Total Gate Charge	V _{SS} =20V, I _S =9A, V _{GS} =4.5V		100		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V _{FSS}	Diode Forward Voltage	V _{GS} =0V, I _S =4.5A		0.77	1.2	V
Note a. Mounted on FR4 board of 25.4mm x 25.4mm x 1.0mm. b. Pulse Test: Pulse Width ≤ 10us, Duty Cycle ≤ 1%. c. Guaranteed by design, not subject to production testing.						

Dec,06,2016

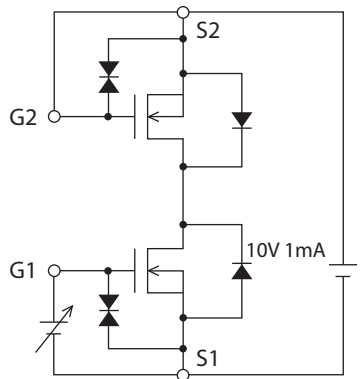
V_{SSS} / I_{SSS}



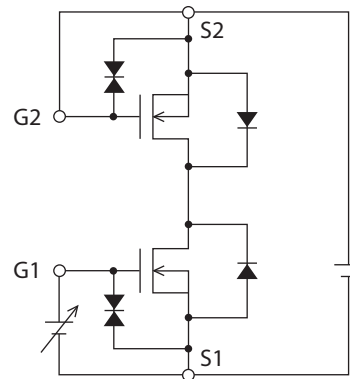
$I_{GSS} (+) / (-)$



$V_{GS} \text{ (off)}$

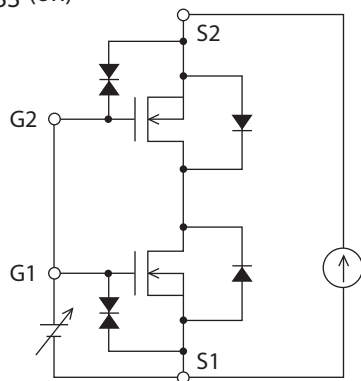


$|y_{fs}|$

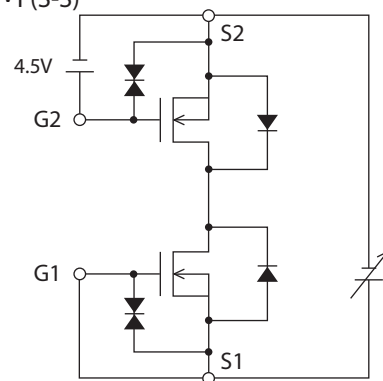


* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

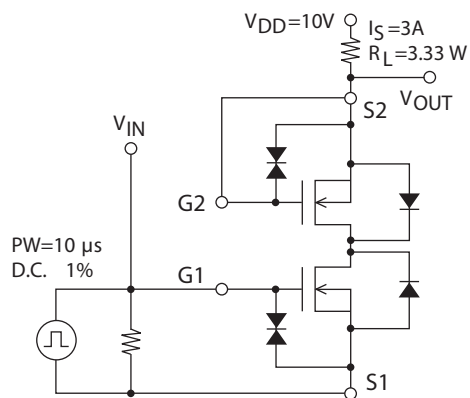
$R_{SS} \text{ (on)}$



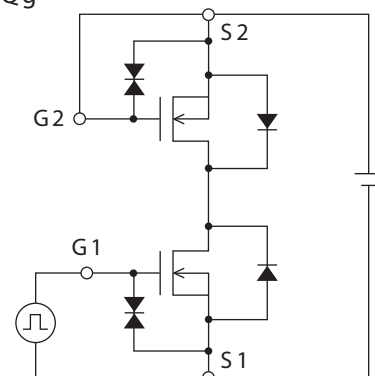
$V_F(S-S)$



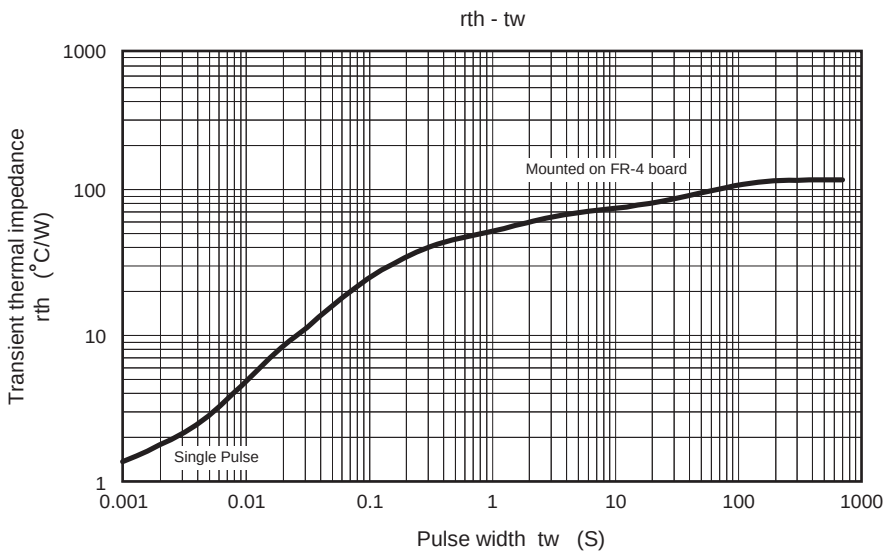
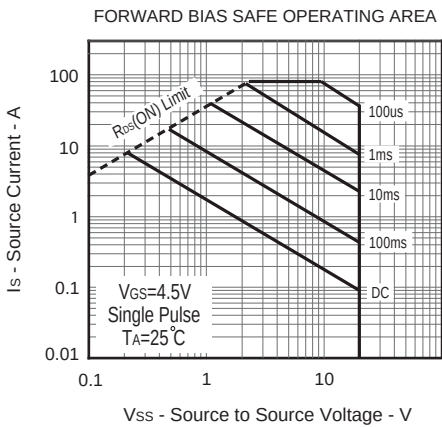
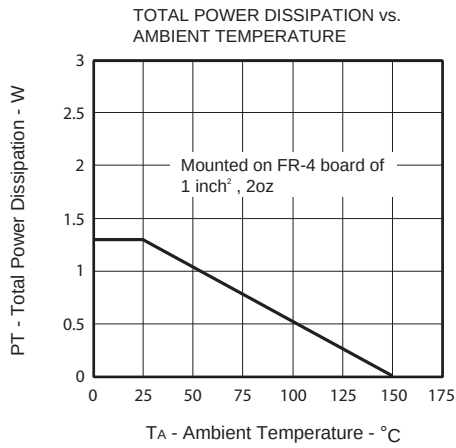
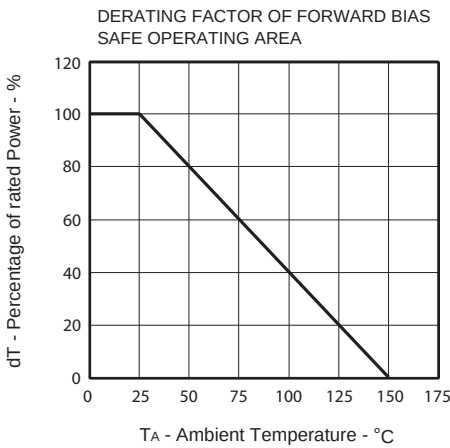
$t_d(\text{on}), t_r, t_d(\text{off}), t_f$

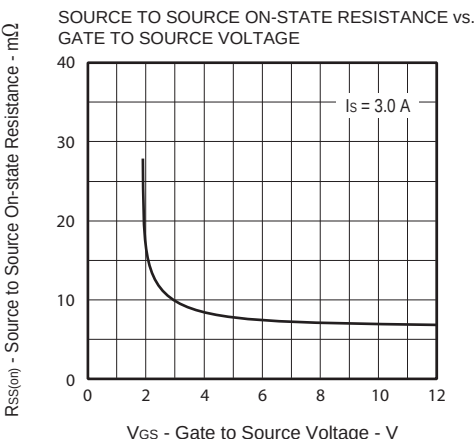
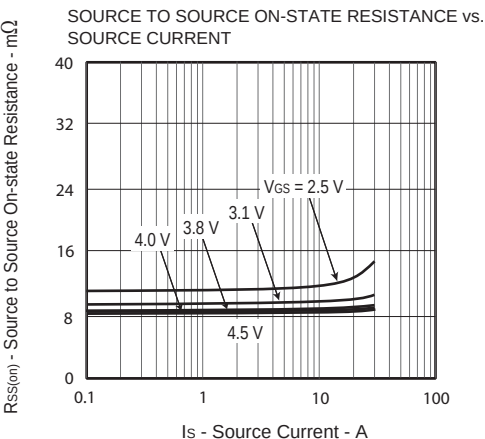
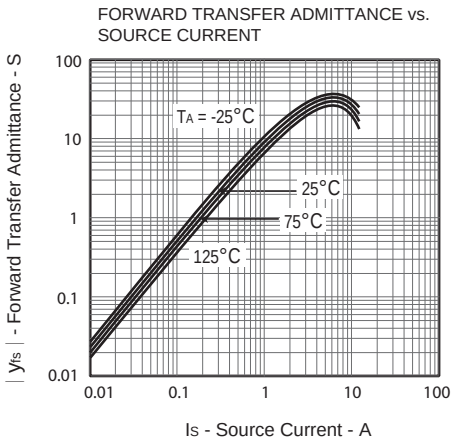
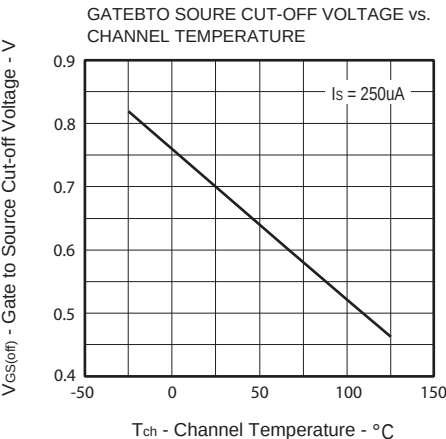
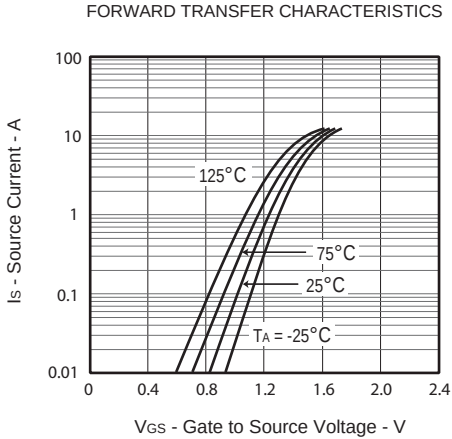
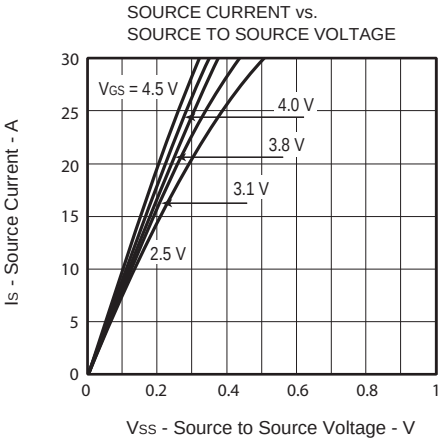


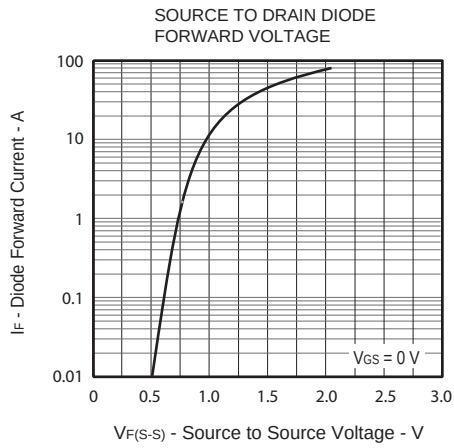
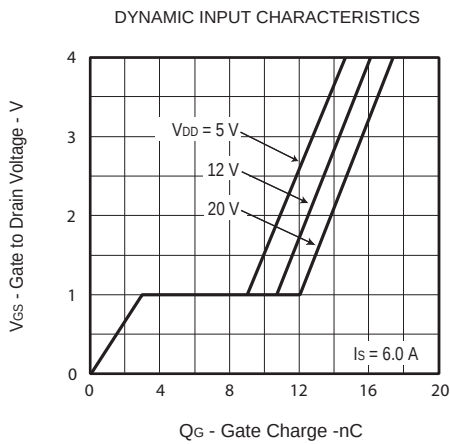
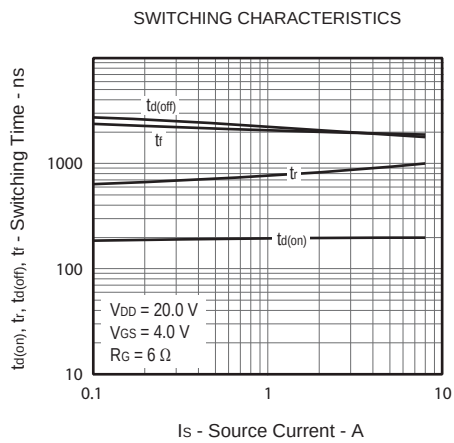
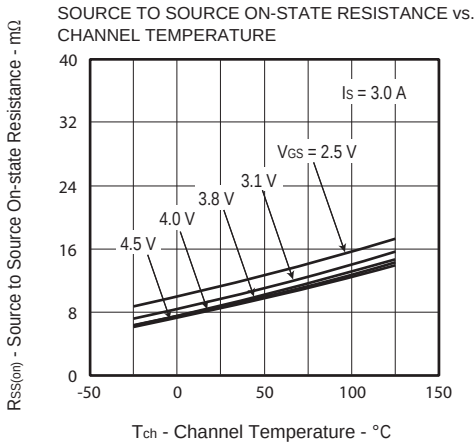
Q_g



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TOP MARKING DEFINITION

WLCSP

