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SC8721B High Efficiency, Synchronous, Buck-Boost Converter with Four Integrated MOSFET

1   Descriptions

SC8721B is a synchronous 4-switch buck-boost converter with four integrated switches. It is able to effectively output voltage no matter it is higher, lower or equal to the input voltage.

SC8721B supports very wide input and output voltage range. It can support applications from 2.7V to 22V input range and 0.7V to 22V output range. Through its I2C interface, user can program the output voltage and output current limit and switching frequency. VINREG voltage can be adjusted by external resistor.

SC8721B employs current-mode control and supports output current limit and dynamic output voltage adjustment for different application conditions.

The IC is in a 21 pin 4x4 QFN package.

2   Features

- High Efficiency Buck-Boost Conversion
- Integrated Switches, 10 mΩ for Q1/4, 20 mΩ for Q2/3
- Wide VIN Range: 2.7 V to 22 V, 25V sustainable
- Wide VOUT Range: 0.7 V to 22 V, 25V sustainable
- Dynamic Output Voltage Control
- Adjustable Switching Frequency
- Output Voltage Cable Drop Compensation
- I2C Programmable Output Voltage
- I2C Programmable Output Current Limit
- Output Current Monitor
- Under Voltage Protection, Over Voltage Protection
- QFN-21 4 x 4 Package
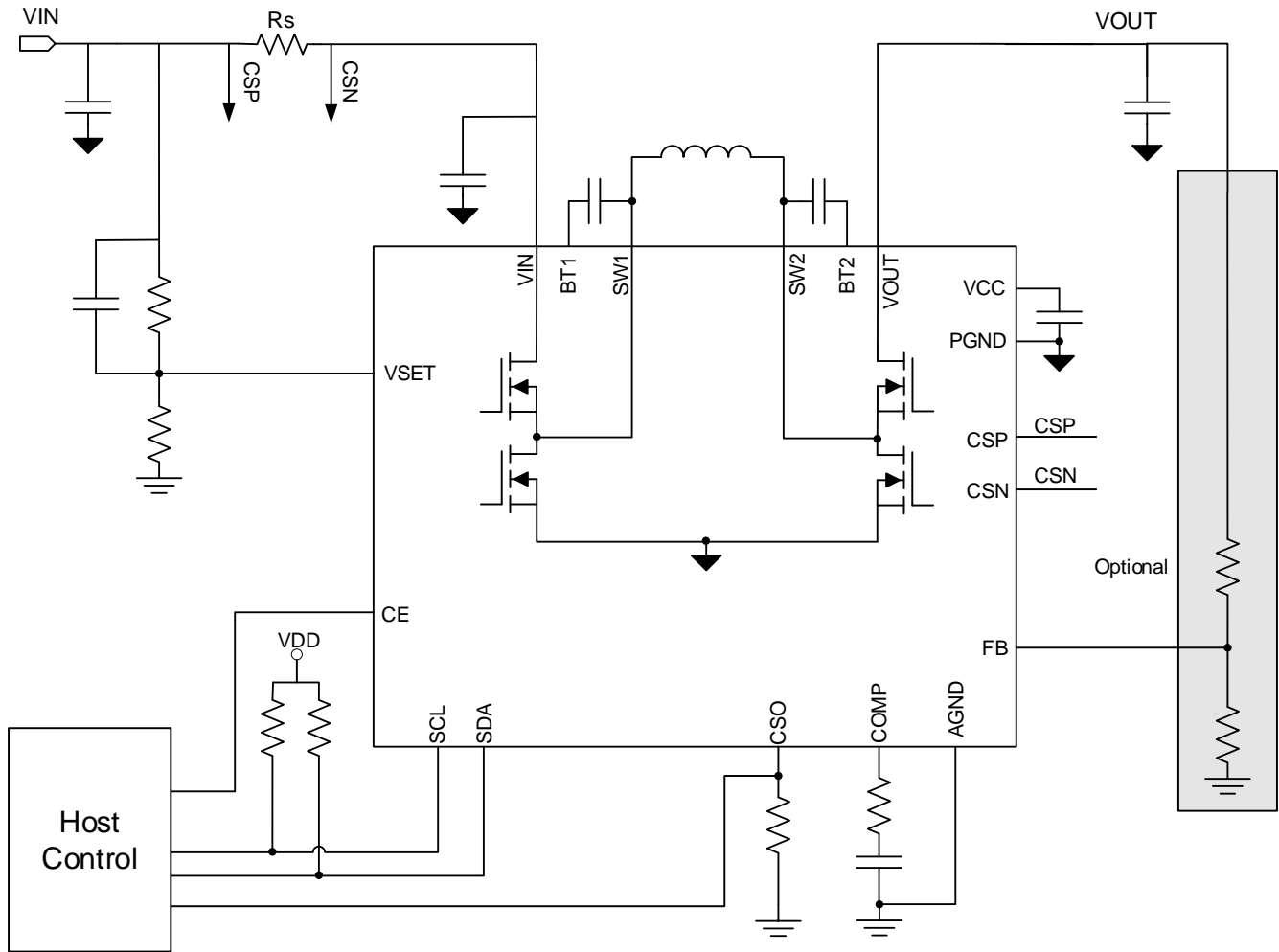
3   Applications

- E-cigarette
- USB Power Delivery
- Wall Adapter
- Type C Hub
- Industry Power Supplies

4   Device Information

Part Number	Package	Dimension
SC8721BQFER	21 pin QFN	4.0mm x 4.0mm x 0.75mm

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5   Typical Application Circuit
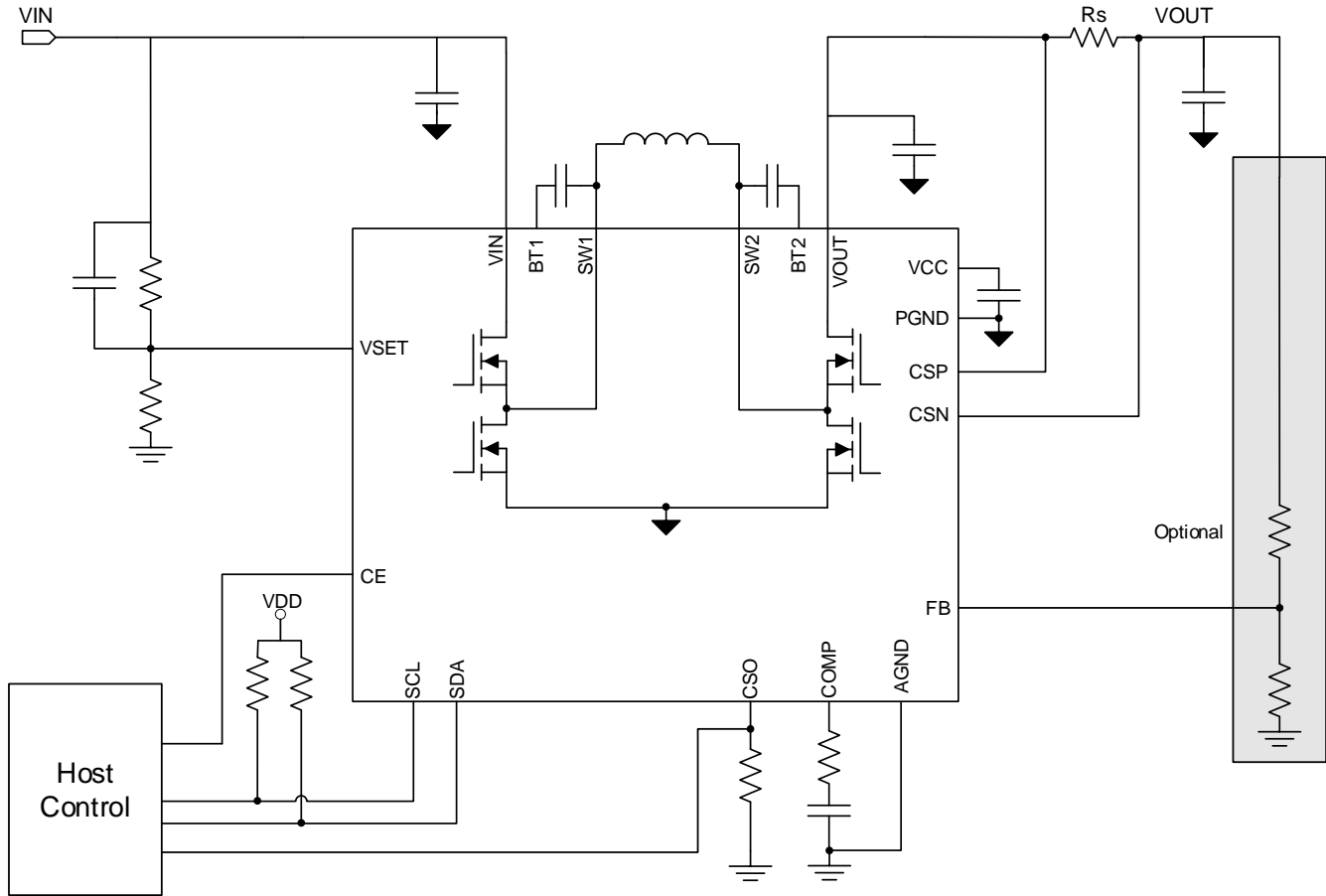
Typical application circuit 1. current sense at VOUT

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Typical application circuit 2. current sense at VIN

Note: User can place current sense resistor at VIN or VOUT according to application requirement. SC8721B constantly regulates the sense resistor current at setting value, which is decided by internal register and CSO resistor. Please refer to **Output Current Limit** for current setting specification.

6   Terminal Configuration and Functions

Top View
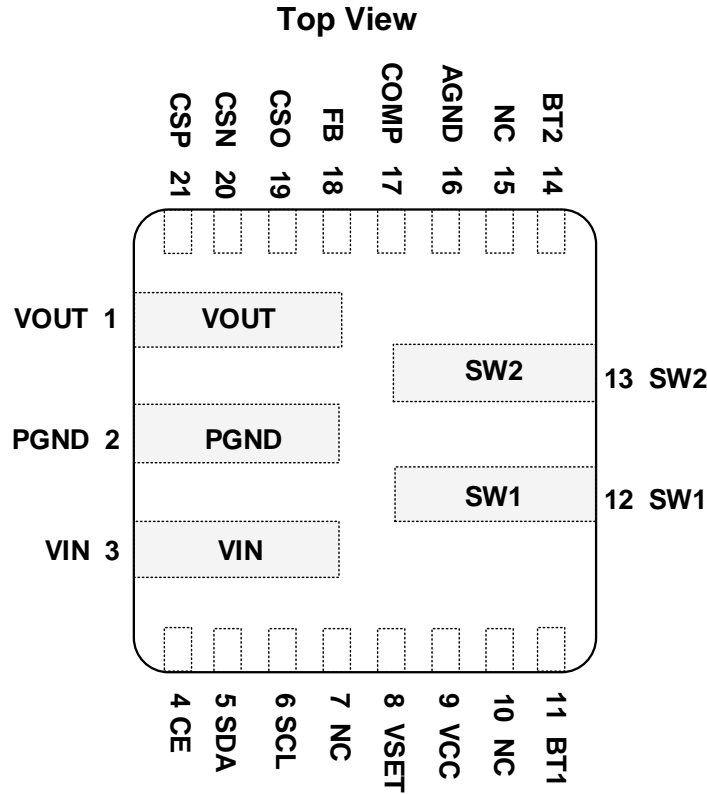
TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VOUT	I/O	The power output node of the converter.
2	PGND	I/O	Power ground. User shall connect PGND and AGND together on PCB.
3	VIN	I/O	the power input node of the converter.
4	CE	I	Chip enable pin, active high: pull this pin to logic low to disable the chip. This pin is internally pulled high.
5	SDA	I/O	I2C interface data. Connect SDA to the logic rail through a pull up resistor (typical 10 kΩ).
6	SCL	I	I2C interface clock. Connect SCL to the logic rail through a pull up resistor (typical 10 kΩ).
7	NC		Must be floating
8	VSET	IO	VINREG internal 1.2V voltage reference. Set the VINREG voltage by resistor divider from to this pin
9	VCC	O	Output of an internal regulator. Connect a 2.2 µF ceramic capacitor from VCC to PGND pin close to the IC. The regulator provides supply for internal gate drivers.

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10	NC		Must be floating
11	BT1	I	Connect a 100nF ceramic capacitor between BT1 pin and SW1 pin to provide the boosted bias voltage for high side gate driver.
12	SW1	I/O	Switching Node 1. Connect to inductor.
13	SW2	I/O	Switching Node 2. Connect to inductor.
14	BT2	I	Connect a 100nF ceramic capacitor between BT2 pin and SW2 pin to provide the boosted bias voltage for high side gate driver.
15	NC		
16	AGND	I/O	Analog ground. User shall connect PGND and AGND together on PCB.
17	COMP	I	Connect a RC network to compensate the control loop.
18	FB	I	Feedback node of VOUT output voltage. Set the VOUT output voltage by the resistor divider connected at this pin.
19	CSO	O	Use this pin to monitor the current sensed by CSP and CSN pin. The voltage of CSO is proportional to the sense current.
20	CSN	I	Negative input of an internal current sense amplifier. Connect a current sense resistor (typical 10 mΩ) between CSP and CSN to sense the current.
21	CSP	I	Positive input of an internal current sense amplifier. Connect a current sense resistor (typical 10 mΩ) between CSP and CSN to sense the current.

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7   Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	Unit
Voltage range at terminals[2]	CE, SDA, SCL, CSEL, VSET, COMP, CSO, FB	-0.3	5.5	V
	VCC	-0.3	6.5	V
	VIN, VOUT, CSP, CSN	-0.3	25	V
	SW1, SW2	-0.3	25	V
	BT1, BT2	-0.3	32	V
	CSP to CSN	-10	10	V
	BT1 to SW1, BT2 to SW2	-0.3	6.5	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1)   Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2)   All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE[1]		QFN-21 (4mmX4mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	45	°C/W
θ_{JC}	Junction to case resistance	10	°C/W

(1)   Measured on JESD51-7, 4-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD[1]	Human body model (HBM) ESD stress voltage[2]	-2	2	kV
	Charged device model (CDM) ESD stress voltage[3]	-750	750	V

(1)   Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2)   Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3)   Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

		MIN	MAX	UNIT
VIN	VIN voltage range	2.7	22	V
VOUT	VOUT voltage range	0.7	22	V

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C_{IN}, C_{OUT}	VIN Capacitance, VOUT capacitance	30		µF
L	Inductance	2.2	10	µH
R_S	Current Sense Resistor	5	10	mΩ
R_{CSO}	Current Limit setting resistor		64	KΩ

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7.5 Electrical Characteristics

T_J= 25℃ and VIN = 12V, Rs=10mΩ, Rcso=64kΩ unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{UVLO}	VIN under-voltage lockout threshold	Rising edge		2.5		V
		Hysteresis		160		mV
I_Q	Quiescent current into VIN	VIN = 8V, VOUT = 5V CE = H, non-switching		1.5		mA
$I_{SHUTDOWN}$	Shutdown current VIN	VIN = 8V, CE = L		5.5		μA
$I_{STANDBY}$	Standby current from VIN	VIN=8V, Standby mode, CE=H		30		μA
VCC, DIRVER AND POWER SWITCH						
V_{CC}	VCC regulation voltage	VIN = 9V	4.4	5	5.5	V
		VIN= 5V, ICC = 30mA	4			V
I_{VCC_LIM}	VCC current limit	VIN = 9V, VCC = 4V		80		mA
R_{DSon_HS}	High side MOS on resistance			10		mΩ
R_{DSon_LS}	Low side MOS on resistance			20		mΩ
REFERENCE VOLTAGE FOR VOUT						
V_{FB}	FB reference voltage		0.99	1	1.01	V
V_{FB_OVP}	FB OVP threshold, over FB target	Rising edge		110%		
		Hysteresis		2%		
V_{INOVP}	Absolute OVP threshold for VIN			23		V
V_{INREG_REF}	VSET reference voltage			1.2		V
CURRENT LIMIT						
I_{LIM}	Output current limit accuracy	$I_{OUT} R_S ≥ 20mV$	-5%		5%	
ERROR AMPLIFIER						
Gm_{EA}	Error amplifier gm			0.16		mS
R_{OUT}	Error amplifier output resistance			20		MΩ
I_{SINK_COMP}	COMP sink current			27		μA
I_{SRC_COMP}	COMP source current			16		μA
I_{BIAS_FB}	FB pin input bias current	FB in regulation			50	nA
LOGIC CONTROL						
R_{PH}	CE pin internal pull high resistor			2		MΩ
V_{IL}	CE pin input low voltage				0.4	V
V_{IH}	CE pin input high voltage		1.2			V
Frequency						
F_{sw}	Switching frequency	REG08 = 0x00		260		kHz
		REG08 = 0x01(default)		500		kHz
		REG08 = 0x02		720		kHz

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		REG08 = 0x03		920		kHz
SOFTSTART						
t_{SS}	Internal soft-start time	From 10% to 90% VOUT		15		ms
I2C INTERFACE (SDA, SCL)						
V_{IL}	SDA/SCL logic low input voltage level	V_{PULL_UP} = 3V			0.4	V
V_{IH}	SDA/SCL logic high input voltage level	V_{PULL_UP} = 3V	2			V
I_{SINK_SDA}	SDA sink current	V_{SDA} = 0.4 V	20			mA
f_{SCL}	I2C clock frequency				400	kHz

8 Feature Description

8.1 Chip Enable

The IC is enabled or disabled by CE signal. When CE input is logic high, the IC is enabled; when CE input is logic low, the IC is disabled. The CE pin is pulled high by 2 MΩ resistor internally.

8.2 Soft Start

The IC implements soft start feature to prevent inrush current during startup in discharging mode. After the discharging mode is enabled, the IC ramps up the internal reference voltage in around 15ms. The output voltage follows the reference, so it starts up slowly. Meantime, the IC ramps up the current limits during the startup. If a heavy load is applied before the output voltage is established, the IC may fail to start up due to the current limit.

8.3 Output Voltage Setting

8.3.1 External Setting method

When FB_SEL signal is 0, the output voltage is set by the resistor divider connected at FB pin and can be calculated as below.

$$VOUT = V_{FB\_REF} \times (1 + \frac{R_{UP}}{R_{DOWN}})$$

Where:

V_{FB_REF} is the internal reference voltage 1V,

R_{UP} and R_{DOWN} are the resistors connected from VOUT to FB and to AGND.

If external setting method is not needed, FB pin is not suggested to be float which may cause output overshoot. It is better to connect FB pin to resistor divider to ensure that SC8721 outputs regulated voltage, or connect it to AGND to set the output at 5V default.

8.3.2 Internal Setting method

When FB_SEL signal is 1, the out voltage can be programmed internally via IIC. VOUT offset voltage is decided by 10-bit register (Reg03<7:0> and Reg04<1:0>), a 20mV/step resolution is given.

OFFSET= [Reg03<7:0> x 4 + Reg04<1:0>] x 20mV

FB_ON is the mask control bit of VOUT_REF register. Only when FB_ON=1, the VOUT_REF register value is valid, the VOUT voltage is 5V default. FB_DIR is the direction control bit.

If FB_DIR=0, the VOUT voltage is:

VOUT = 5V + OFFSET

If FB_DIR=1, the VOUT voltage is:

VOUT = 5V - OFFSET

8.3.3 Dynamic Output Control

In discharging mode, output voltage can be set via IIC. In IIC, there's a load function, after Load is set to 1, VOUT starts to ramp at the speed of 1mV/us.

8.3.4 Cable drop compensation

VOUT has a cable drop compensation. The slope can be programmed via I2C registers. If external feedback resistor is applied, Rup must be 100K to have the designed slope.

8.4 Output Current Limit

The output current limit can be set by internal register and external resistor.

$$IOUT\_LIM = \frac{(CSO\_SET + 1) * 4mV * 2k\Omega}{R_S * R_{CSO}}$$

where

CSO_SET is reference voltage, set by Reg 0x01<7:0>;

R_{cso} = Resistors at CSO pin;

R_S = Current sense resistor value to sense output current;

When output is overload, the IC regulates the output current at setting current limit value and output voltage decreases automatically.

8.5 Output Current Monitor

In discharging mode, the output current can be monitored in real time by external ADC sampling CSO pins.

$$IOUT = \frac{V_{CSO} * 2k\Omega}{R_S * R_{CSO}}$$

where

VCSO is voltage of CSO pin;

R_{cso} = Resistors at CSO pin;

R_S = Current sense resistor value to sense IBUS current;

8.6 Self-adaptive Input Voltage Regulation

The IC features dynamic VIN power management. The allowed minimum VIN operation voltage is VINREG threshold, which can be set by resistor divider at the VSET pin. During charging, if the output current is higher than VIN's current capability, the input source will be overloaded,

and the VIN voltage is pulled low. Once the VIN voltage drops at VINREG threshold, the IC reduces the output voltage automatically and regulates the VIN voltage at VINREG threshold. the VINREG voltage is set by the resistor divider connected at VSET pin and can be calculated as below.

$$VINREG = V_{SET\_REF} \times (1 + \frac{R_{UP}}{R_{DOWN}})$$

Where:

V_{SET_REF} is the internal reference voltage 1.2V, R_{UP} and R_{DOWN} are the resistors connected from VIN to VSET and to AGND.

Connect VSET pin with 10kΩ pull-up resistor to VCC, or set Reg06<4> to 0, VINREG function is disabled.

8.7 Register Load function

When output current limit and output voltage register value is set via I2C, Load bit (Reg0x05<1>) must be set to 1, then value can be loaded to corresponding registers.

8.8 PWM/PFM Operation

The IC supports two operation modes: PWM mode and PFM mode.

In PWM mode, the IC always works with constant switching frequency for the whole load range. This helps achieve the best output voltage performance, but the efficiency is low at light load condition because of the high switching loss.

In PFM mode, the IC still works with constant switching frequency under heavy load condition, but under light load condition, it changes to pulse frequency modulation operation to reduce the switching loss. The efficiency can be improved under light load condition while output voltage ripple will be a little larger compared with PWM operation. Below figure shows the output voltage behavior of PFM mode.
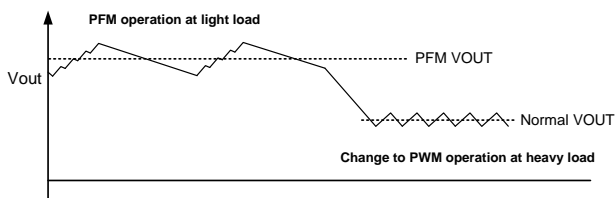

Figure 1 PFM operation

8.9 Switching Frequency

The SC8721B provides four switching frequency selection from 230kHz/500kHz/720kHz/920kHz.

8.10   VCC Driver Voltage

The IC integrates a VCC regulator so to generate the driver voltage for internal driver circuit. The VCC is supplied by VIN and is clamped to 5V. Connect a 2.2μF ceramic capacitor from VCC to PGND pin close to the IC.

8.11   Loop Compensation

The internal control loop should be compensated by the resistor and capacitor connected at COMP pin. 10 kΩ resistor and 22 nF capacitor are suggested for most applications. If faster response is required, the user can increase the resistor value but should keep R*C value unchanged. After changing the compensation, check and make sure the loop is stable under target conditions.

8.9 Standby Mode

When CE signal is high and DIS_DCDC bit is 1, the IC enters into Standby mode. In this mode, the IC stops switching to save the quiescent current. The other functions are still valid, and the MCU can still control the IC through I2C.

8.10 Shutdown Mode

When CE signal is low, the IC enters into Shutdown mode. In this mode, the IC stops working and disables the I2C interface to save the power.

8.12   Protections

8.12.1   Over Voltage Protection

The IC supports three mechanisms for over voltage protection.

The first is once the IC detects the VIN voltage is higher than typical 23V, the IC stops switching until the voltage drops below the threshold.

The second is once the IC detects the VOUT voltage is higher than the setting target by typical 10%(FB_SEL=0), the IC stops switching until the voltage drops below the threshold.

The third is once the IC detects the VOUT voltage is 500mV higher than the setting target (FB_SEL=1), the IC stops switching until the voltage drops below the threshold.

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8.12.2 FB Short Protection

The IC supports FB pin short circuit protection when external divider resistor is applied to adjust voltage in discharging mode. During power on, the IC monitors the FB pin status. Once it detects the FB pin is short to ground, it still starts up and limits the VOUT voltage at 5V fixed voltage. This helps protect the circuits connected at VOUT pin from over voltage stress.

8.13 I2C and Registers

8.13.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x62 (8-bit address is 0xC4 for write command, 0xC5 for read command). The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to 100kbits) and fast mode (up to 400k bits with 5 kΩ pull up resistor at SCL pin and SDA pin respectively).

8.13.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.
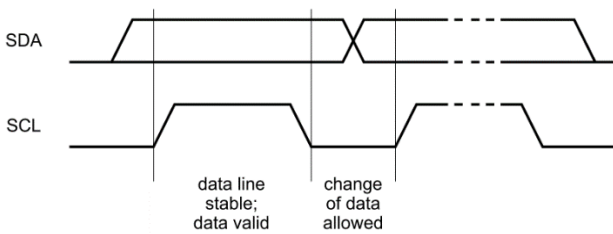

Figure 2 Bit transfer on the I2C bus

8.13.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
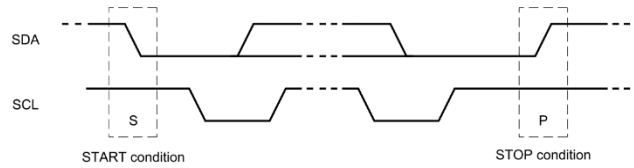

Figure 3 START and STOP conditions

8.13.1.3 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.
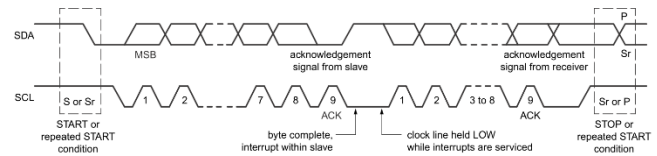

Figure 4 Data transfer on the I2C bus

8.13.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

8.13.1.5 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data

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transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.
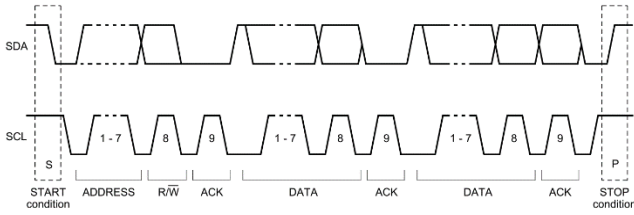

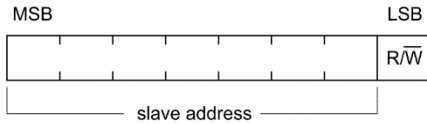Figure 5 A complete data transfer

Figure 6 The first byte after the START procedure

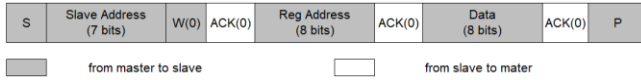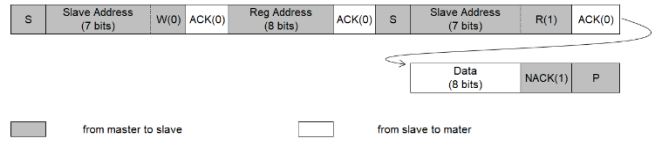### 8.13.1.6 Single Read and Write

Figure 7 Single Wite

Figure 8 Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

8.13.1.7 Multi-Read and Multi-Write

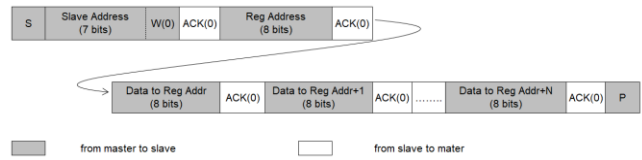The IC supports multi-read and multi-write for continuous registers.
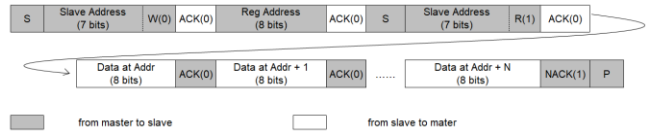

Figure 9 Multi-Write

Figure 10 Multi-Read

9   Application Information

9.1 Input and Output Capacitor Selection

Since MLCC ceramic capacitor has good high frequency filtering and low ESR, X5R or X7R capacitors are recommended for input and output capacitors. Typically, three 22 µF ceramic input capacitors and three 22 µF ceramic output capacitors work for most applications. The input / output capacitors should be places as close to VIN / CSN pins as possible, and they should be also near the PGND pins or thermal pad.

Capacitors' derating effect under DC bias should be taken into account when selecting the capacitors. Ceramic capacitor normally loses its most capacitance at the rated voltage, so leave margin on voltage rating to ensure adequate effective capacitance. For example, if the highest operating voltage is 12V, select 16V or 25V capacitor.

Besides this, high value electrolytic capacitor or tantalum capacitor is recommended to place in parallel with the ceramic capacitors at output to improve the load transient response.

9.2 Inductor Selection

Because the selection of inductor affects the loop stability and the power efficiency, inductor is one of the most important components for the DCDC design.

The IC can work with inductors between 2.2 µH to 10 µH range for most applications. A higher value is suggested to keep the inductor current ripple ≤ 30% of the DC current.

Compared with high value inductor in the same package size, a lower value inductor normally has smaller DC resistance (DCR), so can reduce the conduction power loss, which can be calculated roughly as

$$PL\_DC = IL^2 \cdot DCR$$

IL is the average value of inductor current, and it equals to IIN or IOUT.

However, besides DCR, the core loss or AC loss of an inductor also affects the power efficiency a lot. The low value inductor causes large inductor current ripple, thus high core loss or AC loss, so it is not always the low value inductor supports the higher efficiency.

Since the core loss is related to the inductor material type, and normally the inductor vendors don't provide the core loss data, it is very difficult to suggest what inductor value can result in higher efficiency. As a rule of thumb, high value

inductor like 4.7 µH to 10 µH is recommended for applications where the difference between input voltage and output voltage is big, such as 5V to 20V; while for those applications where input voltage is close to output voltage but large current is on power path, low value inductor like 2.2 µH is suggested.

For applications where efficiency or thermal dissipation is very important, it is highly suggested that the user chooses the inductor in larger package size for lower DCR, and also tests the efficiency with different inductor values, so to find the best combination to achieve the highest efficiency.

The saturation current is another important parameter when selecting the inductor. The inductance can decrease 20% to 35% when the current approaches saturation level, so the user should make sure the saturation current is higher than the inductor peak current during the operation.

The inductor peak current can be calculated by below formula.

$$IL\_peak = IIN + \frac{VIN \cdot (VOUT - VIN \cdot \eta)}{2 \cdot fsw \cdot L \cdot VOUT} \quad (VOUT \geq VIN)$$

$$IL\_peak = IOUT + \frac{VOUT \cdot (VIN - VOUT)}{2 \cdot fsw \cdot L \cdot VIN \cdot \eta} \quad (VOUT < VBIN)$$

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the output current.

9.3 Current Sense Resistor

The R_S in the typical application circuit are current sense resistors for current limit functions.

A high resistor value can result in high current limit / monitor accuracy but causes high conductor loss. Typically, 10 mΩ is recommended. But for applications where efficiency is more important than accuracy, lower value is suggested.

When selecting the current sense resistor, its power rating and temperature coefficient should also be considered.

The power dissipation can be roughly calculated as $P = I^2 R$, where I is the highest current flowing through it. The power rating should be higher than the calculated value.

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The resistor value varies with temperature and the variation is decided by its temperature coefficient. If high accuracy of limit or monitor is required, select as lower temperature coefficient as possible.

9.4 Snubber Circuit

The RC snubber circuits at SWx nodes as shown below can be used to suppress the switching spike so to improve the EMC performance. A typical snubber circuit is composed by a 2.2Ω resistor and 1nF capacitor. The user can reduce the resistance and increase the capacitance further to improve the EMC. However, because it often causes higher switching loss and results in lower efficiency, it is suggested not to add snubber circuits unless necessary.
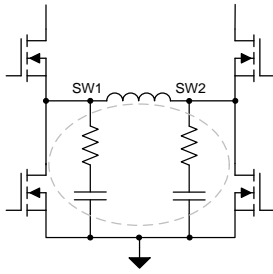

Figure 11 Snubber circuit at SWx nodes

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10 Register Map

Addr	Register	Type	Default value @POR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01H	CSO	R/W	1111 0000	CSO_SET							
02H	SLOPE_COMP	R/W	xxxx xx00	RESERVED						SLOP_COMP	
03H	VOUT_SET_MSB	R/W	0000 0000	VOUT_SET_MSB							
04H	VOUT_SET_LSB	R/W	xxx0 0000	RESERVED			FB_SEL	FB_ON	FB_DIR	VOUT_SET_LSB	
05H	GLOBAL_CTRL	R/W	xxxx x000	RESERVED					DIS_DCDC	REG_LOAD	RESERVED
06H	SYS_SET	R/W	00x1 xxxx	EN_PWM	EXT_DT	RESERVED	EN_VINREG	RESERVED			
07H	RESERVED	R/W	xxxx xxxx	RESERVED							
08H	FREQ_SET	R/W	0000 0001	RESERVED						FREQ_SET	
09H	STATUS_1	R	0000 0000	RESERVED	VOUT_VIN_H	RESERVED	RESERVED	THD	RESERVED	RESERVED	OCP
0AH	STATUS_2	R	0000 0000	VINOVP	RESERVED	RESERVED	RESERVED	RESERVED	VINREG_FLAG	IBUS_FLAG	RESERVED

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Table 1 0x01H CSO_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	CSO voltage setting	1111 0000	CSO_SET used to set VOUT current reference limit The output current limit is calculated as: $$IOUT\_ILIM = \frac{(CSO\_SET+1)*4mV*2k\Omega}{Rs*R_{CSO}}$$ CSO_SET range:0~255 0000 0000: 0 0000 0001: 1 0000 0010: 2 …. 1111 0000: 240 (default) …. 1111 1111: 255	CSO_SET is clamped to be higher than 0x08 internally.

Table 2 0x02H SLOPE_COMP Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-2	R/W	Reserved	000000	**Internal use. Don't overwrite this bit.**	
1-0	R/W	SLOPE_COMP	00	SLOPE_COMP is used to set VOUT cable drop compensation 00: no slope compensation(default) 01: 50mV/A 10: 100mV/A 11:150mV/A	

Table 3 0x03H VOUT _SET_MSB Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	VOUT_SET_MSB	000000	The highest 8-bit of the VOUT_ SET. VOUT_SET_MSB and VOUT_SET_LSB are used to set VOUT_SET The VOUT_SET is calculated as: $VOUT\_SET = VOUT\_SET\_MSB \ x4 + VOUT\_SET\_LSB) \ x \ 20mV$	

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Table 4 0x04H VOUT_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-5	R/W	Reserved	000	**Internal use. Don't overwrite this bit**	
4	R/W	FB_SEL	0	VOUT voltage setting control, only for discharging mode: 0: External VOUT setting, VOUT output voltage is set by resistor divider at FB pin 1: Internal VOUT setting, VOUT output voltage is set by VOUT _SET_MSB, VOUT _SET_LSB and FB_DIR	
3	R/W	FB_ON	0	VOUT_SET mask bit 0: VOUT voltage is not allowed to be revised 1: VOUT voltage is allowed to be revised	
2	R/W	FB_DIR	0	VOUT_SET_direction: 0: Increment(default) 1: Decrement	
1-0	R/W	VOUT_SET_LSB	00	The lowest 2-bit of the VOUT_SET	

Table 5 0x05H GLOBAL_CTRL Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-3	R/W	Reserved	0000	**Internal use. Don't overwrite this bit**	
2	R/W	DIS_DCDC	0	DCDC switching control: 0: enable(default) 1: disable	
1	R/W	Load	0	Write 1 to load register (CSO_SET/VOUT_SET /FB_DIR) and clear to 0 automatically after read	
0	R/W	Reserved bit	0	**Internal use. Don't overwrite this bit**	

Table 6 0x06H SYS_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	EN_PWM	1	EN_ PWM: 0: disable, auto pwm mode(default) 1: enable, force pwm mode	
6	R/W	EXT_DT	0	Switching dead time setting: 0: 20ns(default) 1: 40ns	

5	R/W	Reserved bit	0	**Internal use. Don't overwrite this bit**	
4	R/W	EN_VINREG_PFM	1	VINREG enable control: 0: disable 1: enable (default)	
3-0	R/W	Reserved bit	0000	**Internal use. Don't overwrite this bit**	

Table 7 0x07H TERM_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	Reserved bit	00000000	**Internal use. Don't overwrite this bit**	

Table 8 0x08H FREQ_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-2	R/W	Reserved bit	000000	**Internal use. Don't overwrite this bit**	
1-0	R/W	Frequency set	01	Switching frequency setting: 00: 260kHz 01: 500kHz(default) 10: 720kHz 11: 920kHz	

Table 9 0x09H STATUS_1 Register

| Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R	Reserved bit	0	**Internal use. Don't overwrite this bit**	
6	R	VOUT_VOUT_H	0	0: VOUT < VIN 1: VOUT > VIN	
5	R	Reserved bit	0	**Internal use. Don't overwrite this bit**	
4	R	Reserved bit	0	**Internal use. Don't overwrite this bit**	
3	R	THD	0	1: Thermal shutdown	
2	R	Reserved bit	0	**Internal use. Don't overwrite this bit**	
1	R	Reserved bit	0	**Internal use. Don't overwrite this bit**	

| 0 | R | OCP | 0 | 1: Internal over current protection happens | |

Table 10 0x0AH STATUS_2 Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R	VINOVP	0	1: VIN higher than absolute voltage threshold (22V) happens	
6	R	Reserved bit	0	**Internal use. Don't overwrite this bit**	
5	R	Reserved bit	0	**Internal use. Don't overwrite this bit**	
4	R	Reserved bit	0	**Internal use. Don't overwrite this bit**	
3	R	Reserved bit	0	**Internal use. Don't overwrite this bit**	
2	R	VINREG_FLAG	0	1: IC working in VINREG loop	
1	R	IBUS_FLAG	0	1: IC working in current limit loop	
0	R	Reserved bit	0	**Internal use. Don't overwrite this bit**	

MECHANICAL DATA

QFN-21 (4x4x0.75)
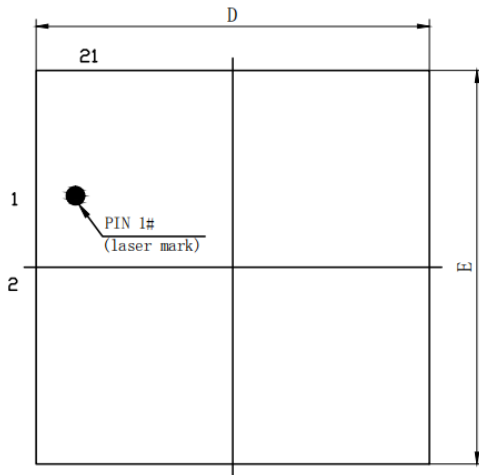
TOP VIEW
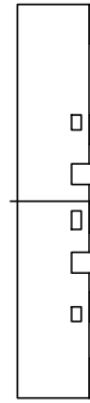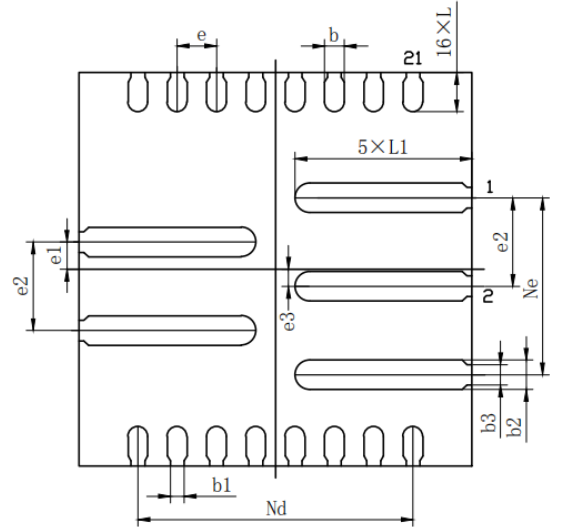
BOTTOM VIEW

SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
b2	0.25	0.30	0.35
b3	0.21REF		
c	0.203REF		
D	3.90	4.00	4.10
e	0.40BSC		
e1	0.275BSC		
e2	0.90BSC		
e3	0.175BSC		
E	3.90	4.00	4.10
Nd	2.80BSC		
Ne	1.80BSC		
L	0.35	0.40	0.45
L1	1.75	1.80	1.85

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RECOMMENDED FOOTPRINT

QFN-21 (4x4x0.75) (Unit: mm)