



# SC8915 High Efficiency, Synchronous, Bi-Directional Buck-Boost Charge Converter with I2C Interface

## 1 Description

SC8915 is a synchronous buck-boost Li-ion battery charger which also supports reverse discharging operation. It integrates two power MOSFETs and can support up to 36V battery voltage and up to 26V VBUS. It can be used to effectively manage the charging process for 1~6 cell Li-ion batteries no matter adapter voltage is higher, lower or equal to the battery voltage. When a system needs to generate an output from the battery, SC8915 can also discharge the cells and delivers desired output no matter it is higher, lower or equal to the battery voltage.

Through its I2C interface, user can set the charging / discharging mode easily, and program the charging current, charging voltage, reserve output voltage, current limits, switching frequency and other parameters flexibly. Besides that, SC8915 integrates 10-bit ADC, so user can read the VBUS / VBAT voltage and current in real time, simplifying the system design.

SC8915 supports internal current limit, over voltage protection, output short protection and over temperature protections to ensure safety under different abnormal conditions.

SC8915 adopts 40 pin QFN 6x6 package.

## 3 Applications

- Power Bank
- USB Power Delivery
- Type C Hub
- Industrial Power Supplies

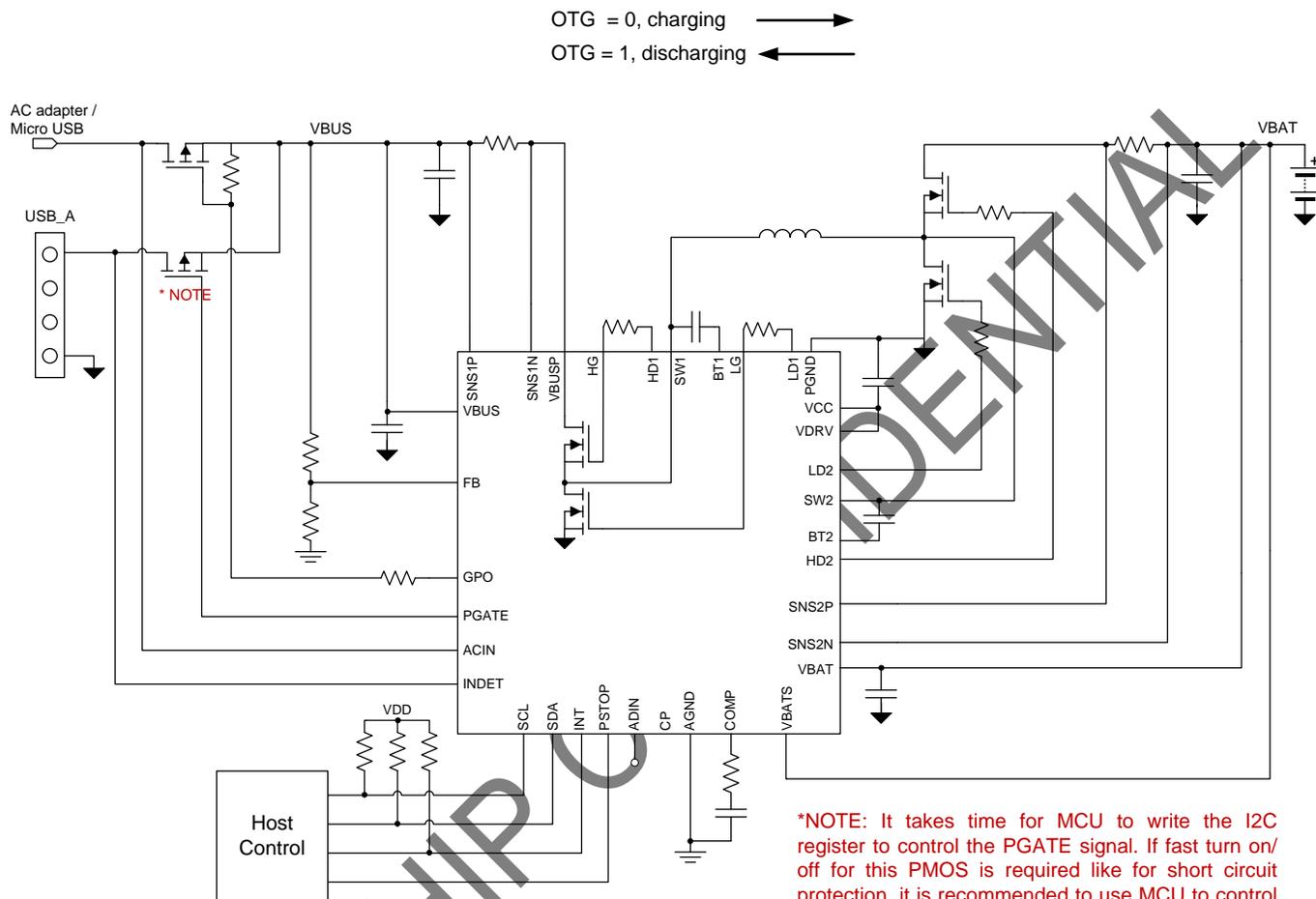
## 2 Features

- Buck-Boost Battery Charger for 1 to 6 Cell Batteries
- Charging Management including Trickle Charge, CC Charge, CV Charge and Charge Termination
- Buck-Boost Reverse Discharging Mode
- Integrates Two Power MOSFETs
- Wide V<sub>BAT</sub> Range: 2.5 V to 36 V, 40V sustainable
- Wide V<sub>BUS</sub> Range: 2.5 V to 26 V, 30V sustainable
- I2C Programmable Charging Current and Voltage
- I2C Programmable Discharging Output Voltage
- I2C Programmable Input / Output Current Limit
- I2C Programmable Switching Frequency
- High Efficiency Buck-Boost Conversion
- 10-bit ADC resources
- Charging Status Indication
- Event Detections, including Automatic Adapter Insert and Automatic Load Insert Detection
- Power Path Control
- Under Voltage Protection, Over Voltage Protection, Over Current Protection, Short Circuit Protection and Thermal Shutdown Protection
- QFN-40 Package

## 4 Device Information

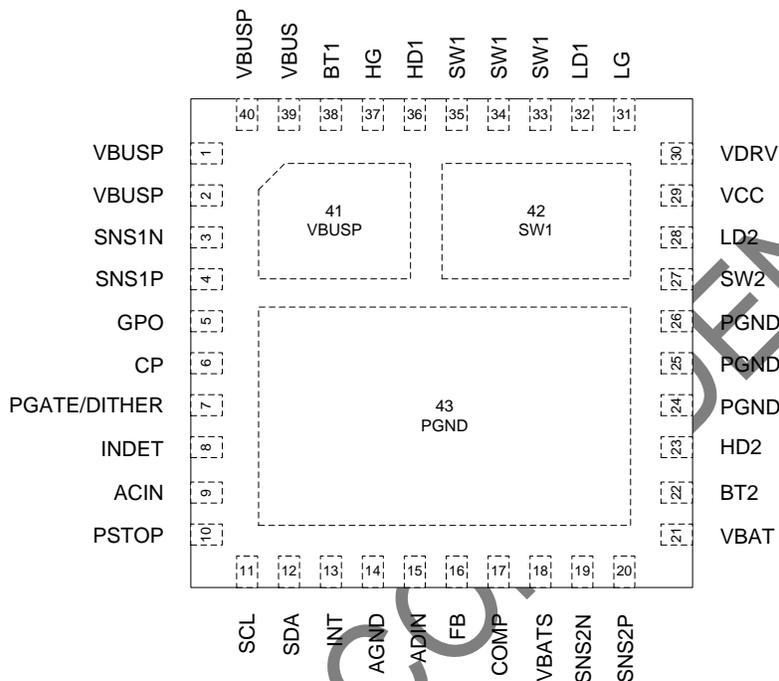
Part Number	Package	Dimension
SC8915QDHR	40 pin QFN	6.0mm x 6.0mm x 0.75mm

## 5 Typical Application Circuit



## 6 Terminal Configuration and Functions

**SC8915**  
Top View



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1, 2, 40	VBUSP	I/O	Power node of VBUS. Connect to adapter input port or USB port. Work as the power input of the converter when in charging mode, and power output in discharging mode.
3	SNS1N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from VBUS.
4	SNS1P	I	Positive input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from VBUS.
5	GPO	O	Open drain output for general purpose. It is controlled by GPO_CTRL bit. User can use this pin to drive external PMOS with a pull up resistor.
6	CP	O	Driver for external charge pump circuit. <b>(CHARGE PUMP NOT RECOMMENDED. It is suggested to leave this pin floating, and connect VDRV with VCC. Consult local FAE if charge pump is needed)</b>
7	PGATE/DITHER	IO	PMOS gate driver controlled by PGATE bit, used to control the external PMOS on the power path. This pin can be configured through I2C for switching frequency dithering function. Connect a ceramic capacitor (typical 100nF) from this pin to ground when for frequency dither function.
8	INDET	I	Connect this pin to a USB-A port to detect the load insertion event. When an insertion event is

			detected, the IC sets INDET bit and outputs an INT interrupt pulse to inform MCU.
9	ACIN	I	Connect this pin to AC adapter input node or micro-USB port to detect an AC adapter insertion event. When an insertion event is detected, the IC sets AC_OK bit and outputs an INT interrupt pulse to inform MCU.
10	PSTOP	I	Power stop control. Pull this pin to logic low to enable the power blocks; pull this pin to logic high to disabled the power blocks, and the IC enters into Standby mode. In Standby mode, only the AC adapter and load insert detection functions and the I2C circuits keep working.  This pin is internally pulled low.
11	SCL	I	I2C interface clock. Connect SCL to the logic rail through a pull up resistor (typical 10 kΩ). The IC works as a slave, and the I2C address is 0x74H.
12	SDA	I/O	I2C interface data. Connect SDA to the logic rail through a pull up resistor (typical 10 kΩ).
13	INT	O	An open drain output for interrupt signal. The IC sends a logic low pulse at INT pin to inform the host if an interrupt event happens.
14	AGND	I/O	Analog ground. Connect PGND and AGND together at the thermal pad under IC.
15	ADIN	I	ADC input pin. Apply an analog signal ( $\leq 2.048V$ ) to this pin, the internal 10-bit ADC can convert this analog signal to digital signals, and store the digital values in a register.
16	FB	I	Feedback node for VBUS voltage. Connect a resistor divider from VBUS to FB to set the VBUS discharging output voltage in external way. The FB reference can also be programmed through I2C.
17	COMP	I	Connect resistor and capacitor at this pin to compensate the control loop.
18	VBATS	I	Sense node for VBAT voltage. Connect to VBAT rail if internal way is selected for VBAT charging termination voltage setting; connect a resistor divider at VBATS if external way is selected.
19	SNS2N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from battery.
20	SNS2P	I	Positive input of a current sense amplifier. Connect to the other pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from battery.
21	VBAT	I	Power supply to the IC. Connect to the battery positive node. Place a 1 μF capacitor from this pin to PGND as close to the IC as possible.
22	BT2	I	Connect a 100nF capacitor between BT2 pin and SW2 pin to bootstrap a bias voltage for high side MOSFET driver.
23	HD2	O	Gate driver output to control the external high side power MOSFET.
24-26	PGND	I/O	Power ground. Connect PGND and AGND together at the PGND thermal pad under IC.
27	SW2	I/O	Switching node. Connect to the inductor.
28	LD2	O	Gate driver output to control the external low side power MOSFET.
29	VCC	O	Output of an internal 5V linear regulator. Connect a 1 μF capacitor from VCC pin to PGND as close to the IC as possible.
30	VDRV	I	Power supply input for internal driver circuits. One way of getting the power supply is to connect VCC to this pin directly. Another way is to use the CP driver to implement a charge pump between VCC and VDRV pin. <b>(CHARGE PUMP WAY IS NOT RECOMMENDED. CONSULT LOCAL FAE IF CHARGE PUMP IS USED)</b>



31	LG	I	Gate input of the integrated low side MOSFET. Connect to LD1 pin with or without a driving resistor in between.
32	LD1	O	Gate driver output to the integrated low side MOSFET. User can short LD1 pin and LG pin directly, or connect a driving resistor between LD1 and LG pins to limit the driver current.
33 – 35	SW1	I/O	Switching Node. Connect to the inductor.
36	HD1	O	Gate driver output to the integrated high side MOSFET. User can short HD1 pin and HG pin directly, or connect a driving resistor between HD and HG pins to limit the driver current.
37	HG	I	Gate input of the integrated high side MOSFET. Connect to HD1 pin with or without a driving resistor in between.
38	BT1	I	Connect a 100nF capacitor between BT1 pin and SW1 pins to bootstrap a bias voltage for high side MOSFET driver.
39	VBUS	I	Power supply to the IC. Connect to the VBUS rail. Place a 1 $\mu$ F capacitor from this pin to PGND as close to the IC as possible.
41	VBUSP	I/O	VBUSP thermal pad under IC. Connect to VBUSP pins together.
42	SW1	I/O	Switching thermal pad under IC. Connect to SW1 pins together.
43	PGND	I/O	PGND thermal pad under IC. Connect to PGND pins together. Connect AGND and PGND together at this thermal pad.