High Efficiency, Synchronous 3A Buck Charger for 1 cell Li-ion Battery with NVDC Power Path Management

1 DESCRIPTION

The SC89601A is a 1.5MHz highly integrated switch-mode buck charger for 1 cell Li-ion battery applications and NVDC system power path management, which separate the system load and charge current, also the system can power up with deep depletion battery. System can get the power from VBUS, VBAT or both. It supports 3.9-13.5V input voltage, up to 3A charging current and provide battery charge management functions including trickle charge, constant current charge, constant voltage charge, charge termination ,auto recharge and charging status indication.

The SC89601A supports flexible charge current option, the user can program the current and all others charger spec by I2C interface.

The SC89601A supports USB OTG with up to 1.4A output with PFM/PWM mode. Meanwhile, the SC89601A supports USB Input BC1.2, non-standard adapters.

The SC89601A supports input current and voltage limit, input under voltage and over voltage protections, internal cycle by cycle current limit, battery short circuit protection, and output over voltage protection. It also offers charging safety timer and over temperature protection to ensure safety under different abnormal conditions.

The SC89601A integrated all MOSFETs, current sensing, loop compensation and I2C interface.

The SC89601A is available in QFN(24)-4*4 package.

2 FEATURES

- Integrated Synchronous Buck Charger
- Integrated NVDC Power Path Management
- Charging Management (Trickle Charge / Constant/ Current Charge / Constant Voltage Charge / Charge Termination)
- Integrated I2C Interface
- I2C Programmable Constant Charge Current, ±5% @1.5A-3A Accuracy
- I2C Programmable Constant Voltage,±0.5% Accuracy
- I2C Programmable Charge Safety Timer
- Support OTG Discharging Function and I2C Programmable Output Voltage: 3.9V~5.4V with up 1.4A Current
- Charge Status Indication
- NTC for Battery Protection (Support JEITA Standard)
- Input Under Voltage and Over Voltage Protection
- Internal Cycle by Cycle Over Current Protection
- OTG OCP/OVP/VBAT_LOW Protection
- Battery Over Voltage and Short Protection
- Battery Discharging Over Current and Under voltage Protection
- Thermal Regulation and Shutdown
- QFN(24)-4*4 Footprint

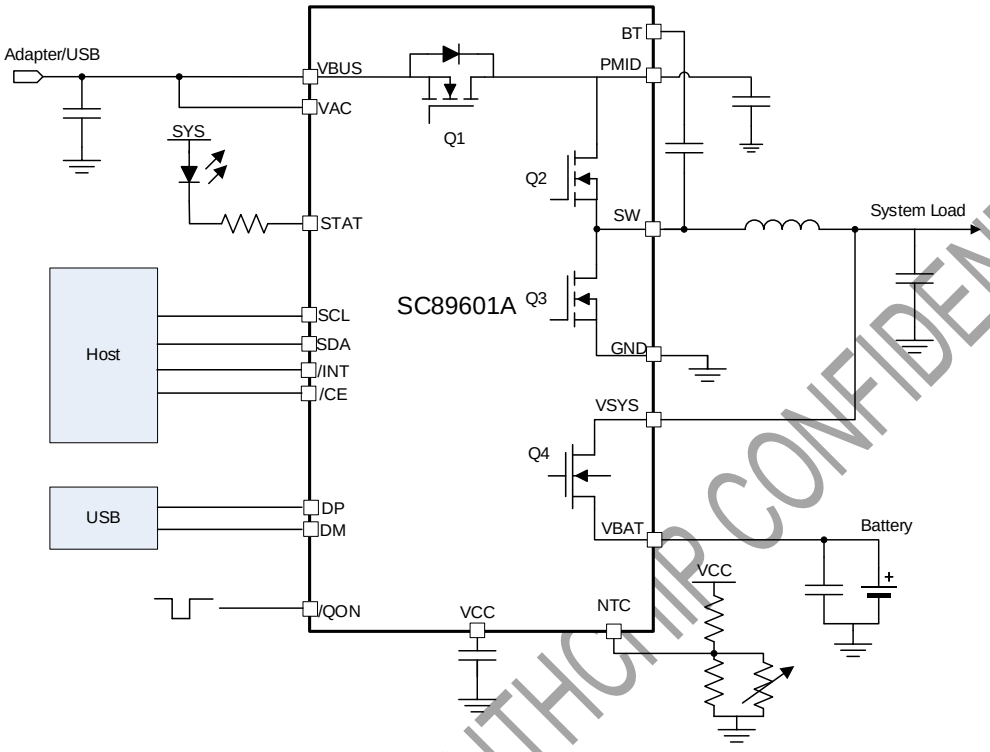
3 APPLICATIONS

- Smart Phones
- Portable Internet Devices and Accessory

4 DEVICE INFORMATION

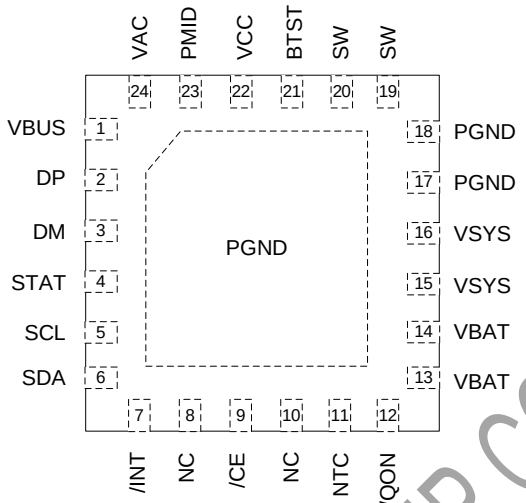
Part Number	Package	Dimension
SC89601AQDLR	QFN(24)-4*4	4mm x 4mm

5 Typical Application Circuit



6 Terminal Configurations and Functions

QFN(24) 4x4 (TOP View)



I/O			DESCRIPTION
SC89601A	NAME		
1	VBUS	I	Power supply pin. Place a 1μF ceramic capacitor from VBUS to GND close to the IC.
2	DP	IO	Positive line of the USB data line pair. DP/DM based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2.
3	DM	IO	Negative line of the USB data line pair. DP/DM based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2.
4	STAT	O	Open-drain charge status output. Connect the STAT pin to a logic rail via 10-kΩ resistor. The STAT pin indicates charger status. Collect a current limit resister and a LED from a rail to this pin. Charge in progress: LOW Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses This pin can be disabled via STAT DIS register bit.
5	SCL	I	I2C interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
6	SDA	IO	I2C interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
7	/INT	O	Open-drain interrupt Output. Connect the INT to a logic rail through 10-kΩ resistor. The /INT pin sends an active low, 256-μs pulse to host to report charger device status and fault.
8	NC		Not Connected
9	/CE	I	Charger enable pin. Low to enable battery charging.
10	NC		Not Connected
11	NTC	IO	Connect to the Negative Temperature Coefficient (NTC) thermistor inside the battery cells to sense the battery cells temperature for protection. When NTC is not used, connect a 10KΩ resistor to GND.
12	/QON	I	BATFET enable control input. When BATFET is in ship mode, a logic low of $t_{SHIPMODE}$ duration turns on BATFET to exit shipping mode.
13,14	VBAT	O	Battery connection point to the positive terminal of the battery pack. Connect a 10μF ceramic capacitor close to the VBAT pin.

15,16	VSYS	O	Converter output connection point. Connect a 20 µF capacitor close to the VSYS pin.
17,18	PGND	I	Power ground pin.
19,20	SW	O	Switching node output. Connected to output inductor. Connect the 47nF bootstrap capacitor from SW to BTST.
21	BTST	IO	PWM high side driver positive supply. Internally, the BTST pin is connected to the cathode of the boost-strap diode. Connect the 47nF bootstrap capacitor from SW to BTST.
22	VCC	O	HSFET and LSFET driver and internal supply output. Internally, VCC is connected to the anode of the boost-strap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor from VCC to GND. The capacitor should be placed close to the IC.
23	PMID	O	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND.
24	VAC	I	Connected to VBUS.

7 Specification

7.1 Absolute Maximum Rating

Over operating free-air temperature range (unless otherwise noted)(1)

		Min.	Max.	Unit
Voltage(2)	VBUS, VAC	-0.3	22	V
	PMID	-0.3	22	V
	BTST	-0.3	22	V
	SW(3)	-2(10ns)	16	V
	BTST to SW	-0.3	6	V
	DP,DM,VCC,NTC,/CE,VBAT,VSYS,SDA,SCL,/INT,/QON , QON, STAT	-0.3	6	V
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
(2) All voltages are with respect to network ground terminal.
(3) VBUS, PMID, BTST, SW should be tied together to test the SW abs voltage.

7.2 Thermal Information

THERMAL RESISTANCE(1)		QFN (4mmX4mm)	Unit
θ_{JA}	Junction to ambient thermal resistance	34	°C/W
θ_{JC}	Junction to case resistance	25	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.3 ESD Ratings

			Min.	Max.	Unit
V_{ESD}(1)	Human-body Model (HBM) (2)	All pins	-2	+2	kV
	Charged-device Model (CDM) (3)		-750	750	V

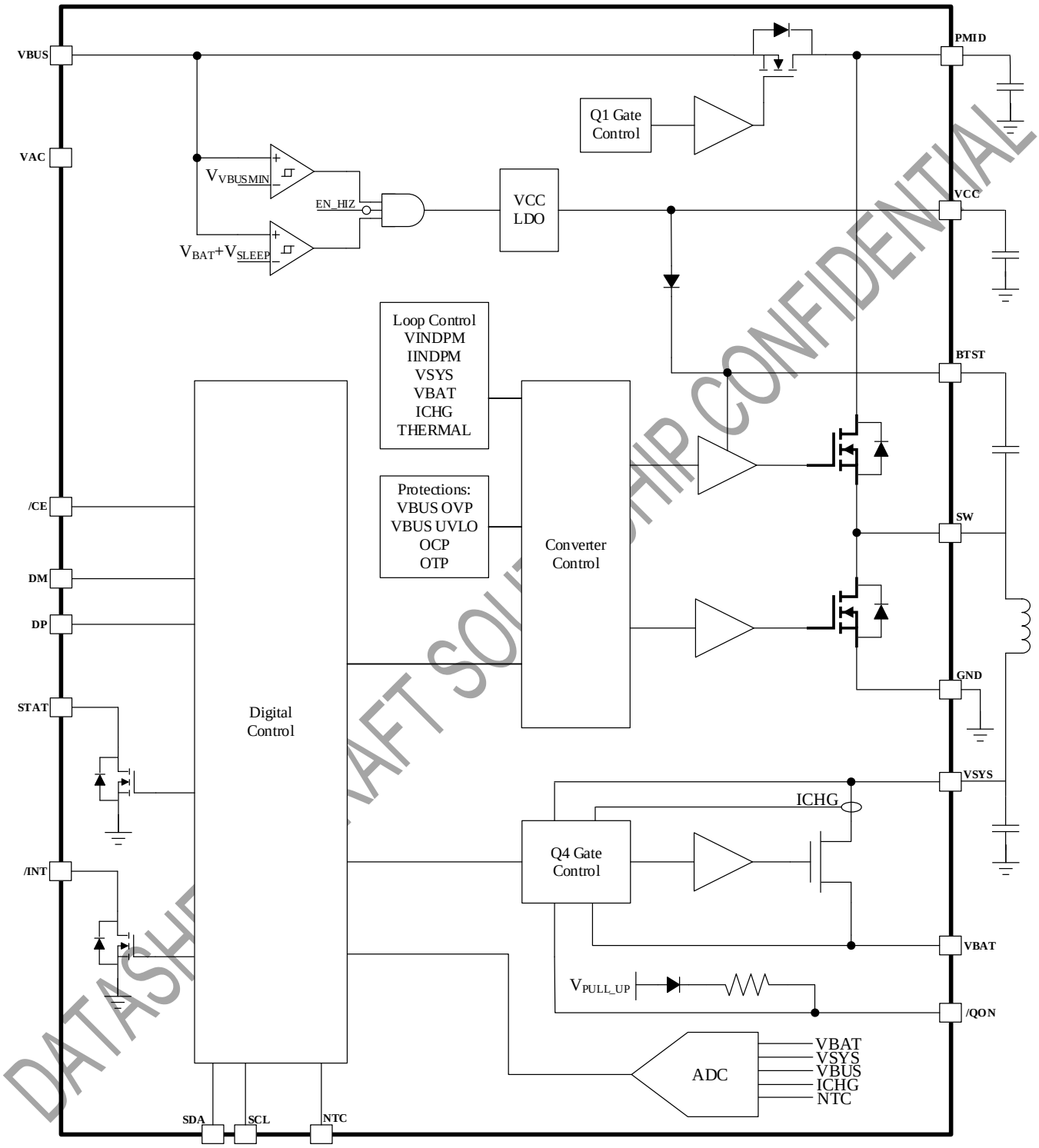
(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operation Conditions

		MIN	TYP	MAX	UNIT
V_{BUS}	VBUS voltage range	3.9		13.5	V
V_{BAT}	VBAT voltage range		4.2	4.848	V
I_{IN}	Input current limit			3.25	A

I_{CC}	Constant current charge current			3	A
I_{DIS}	Discharging current		10		A
L	Inductance		1		μH
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

8 Function Block Diagram



9 Electrical Characteristics

T_J= -40°C to 125 °C and V_{AC_UVLO}< V_{BUS} < V_{VAC_OVP}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{BUS}	Operating input V_{BUS} voltage		3.9		13.5	V
V_{VAC_UVLO}	V_{BUS} for active I2C, no battery	Rising edge		3.3	3.7	V
		Hysteresis		300		mV
V_{SLEEP}	V_{BUS}-V_{BAT} threshold	Falling edge	20	100	210	mV
		Rising edge	120	220	370	mV
V_{VAC_OVP}	V_{BUS} Over Voltage threshold	5.8V , Rising edge	5.4	5.8	6.1	V
		Hysteresis		300		mV
		6.4V, Rising edge	6.1	6.4	6.75	V
		Hysteresis		300		mV
		10.5V, Rising edge	10	10.5	11.1	V
		Hysteresis		300		mV
		14.2V, Rising edge	13.5	14.2	14.9	V
		Hysteresis		300		mV
V_{VBAT_UVLO}	BAT for active I2C, no VBUS	Rising edge	2.25			V
		Hysteresis		240		mV
V_{VBAT_DPL}	Battery Depletion threshold	Rising edge	2.5	2.6	2.75	V
		Hysteresis		200		mV
$V_{VBUSMIN}$	Bad adapter detection threshold	Falling edge	3.6	3.7	3.8	V
		Hysteresis		200		mV
I_{BADSRC}	Bad adapter detection sink current from V_{BUS} to GND			30		mA
I_{BAT}	Battery discharge current in Buck mode	V_{BAT} = 4.5 V, HIZ mode, no V_{BUS}, BATFET_DIS Enable,T_J ≤ 85°C		15	25	μA
		V_{BAT} = 4.5 V, HIZ mode, no V_{BUS}, BATFET_DIS Disable ,T_J ≤ 85°C		22	35	μA
I_{VBUS_HIZ}	Input supply current in buck mode when HIZ mode is enabled	V_{BUS}=5V, HIZ mode and BATFET _DIS Disable, no battery			70	μA
		V_{BUS}=12V,HIZ mode and BATFET _DIS Disable, no battery			70	μA
I_{VBUS}	Input supply current in buck mode	V_{BUS} > V_{VAC_UVLO}, V_{BUS}>V_{BAT}, Converter not switching		1.5	3	mA
		V_{BUS} > V_{VAC_UVLO}, V_{BUS}>V_{BAT}, Converter switching, V_{BAT}=3.8V, I_{SYS}=0A，disable charger		3		mA
I_{BOOST}	Battery discharge current in boost mode	V_{BAT}=4.2V,boost mode, I_{VBUS}=0A, converter switching			3	mA
POWER PATH						

V_{SYS}	Typical system regulation voltage	I_{SYS}=0A,V_{BAT}<V_{SYSMIN},I_{SYS}=0A, BATFET Disable		V_{SYSMIN}+180mV		V
		I_{SYS}=0A,V_{BAT}>V_{SYSMIN},I_{SYS}=0A, BATFET Disable		V_{BAT}+50 mV		V
V_{SYS_MAX}	Maximum DC system voltage output	I_{SYS}=0A,V_{BAT}>V_{SYSMIN},I_{SYS}=0A, BATFET Disable, V_{BAT}<=4.4V	4.4	4.45	4.51	V
R_{DSON_Q1}	Reverse blocking MOSFET on resistance	V_{CC}=5V		38		mΩ
R_{DSON_Q2}	High side switching MOSFET on resistance	V_{CC}=5V		50		mΩ
R_{DSON_Q3}	Low side switching MOSFET on resistance	V_{CC}=5V		50		mΩ
R_{DSON_Q4}	V_{SYS} to V_{BAT} MOSFET on resistance	V_{VBAT}=4.2V		20		mΩ
V_{FWD}	Supplement mode Q4 forward voltage			50		mV
CHARGER MANAGEMENT						
V_{BATREG_RANGE}	Regulation Charge Voltage		3.84		4.848	V
V_{BATREG_STEP}	Charge Voltage Step			16		mV
V_{BATREG_ACC}	Charge Voltage accuracy	V_{BATREG}=4.208V	4.18	4.208	4.23	V
		V_{BATREG}=4.384V	4.36	4.384	4.4	V
		V_{BATREG}=4.432V	4.4	4.432	4.45	V
I_{CC_RANGE}	Constant charging current range		0		3	A
I_{CC_STEP}	Constant charging current step			60		mA
I_{CC_ACC}	Constant charging current accuracy	I_{CC} =240mA， V_{BAT}=3.1V or 3.8V	216	240	264	mA
		I_{CC} =720mA， V_{BAT}=3.1V or 3.8V	684	720	756	mA
		I_{CC} =2040mA， V_{BAT}=3.1V or 3.8V	1938	2040	2142	mA
		I_{CC} =3000mA， V_{BAT}=3.1V or 3.8V	2850	3000	3150	mA
V_{TC}	Trickle charge to CC Charge battery voltage threshold	Rising edge	2.9	3	3.1	V
		Hysteresis		200		mV
I_{TC_RANGE}	Trickle charge current range		60		960	mA
I_{TC_STEP}	Trickle charge current step			60		mA
I_{TC_ACC}	Trickle charge current accuracy	I_{TC} =120mA	90	120	150	mA

		I_{TC} =420mA	390	420	450	mA
I_{TERM_RANGE}	Termination current range		30		930	mA
I_{TERM_STEP}	Termination current step			60		mA
I_{TERM_ACC}	Termination current accuracy	I_{TERM} =120mA	90	120	150	mA
		I_{TERM} =420mA	390	420	450	mA
V_{BAT_SHORT}	Battery short voltage	Falling edge	1.85	2	2.15	V
		Hysteresis		200		mV
I_{SHORT}	Battery short charge current	V_{BAT} =1V	35	50	65	mA
V_{RECHG}	Recharge threshold below V_{BAT_REG}	V_{BAT} falling edge,100mV	80	100	140	mV
		V_{BAT} falling edge, 200mV	170	200	250	mV
$I_{SYSLOAD}$	System discharge load current	V_{SYS}=4.2V		30		mA
t_{TERM_DGL}	Deglitch time for charge termination		200	250	300	ms
t_{RECH_DGL}	Deglitch time for recharge		200	250	300	ms
t_{SYSOCP_DGL}	System over-current deglitch time to turn off Q4		50	100	150	us
t_{SYSOVP_DGL}	System over-voltage deglitch time to turn off DCDC			1		us
t_{BATOVP_DGL}	Battery over-voltage deglitch time to disable charger			1		us
INPUT VOLTAGE AND CURRENT REGULATION						
V_{INDPM_RANGE}	Input voltage regulation limit range		3.9		5	V
V_{INDPM_STEP}	Input voltage regulation limit step			100		mV
V_{INDPM_ACC}	Input voltage regulation limit accuracy	V_{INDPM}=4.8V	4.6	4.8	4.944	V
I_{INDPM_RANGE}	Input current regulation limit range		100		3250	mA
I_{INDPM_STEP}	Input current regulation limit step			50		mA
I_{INDPM_ACC}	Input current regulation limit accuracy	V_{BUS} =5V, I_{INDPM} =500 mA	410		500	mA
		V_{BUS} =5V,I_{INDPM} =900 mA	750		900	mA
		V_{BUS} =5V,I_{INDPM} =1500 mA	1300		1500	mA

		V_{BUS} =5V,I_{INDPM} =2400 mA	2200		2400	mA
I_{IN_START}	Input current limit during system start-up sequence			200		mA
PROTECTION						
V_{BAT_OVP}	Battery over voltage threshold	Rising	102	104	105	%
		Hysteresis		2		%
I_{BAT_OCP}	Battery discharge over current threshold		10			A
PWM						
f_{SW}	PWM switching frequency	V_{BUS}= 9V， V_{BAT}=4V， $I_{CC=}$ 3A	1320	1500	1680	KHz
D_{MAX}	Maximum PWM duty cycle(Buck)			97		%
JEITA (BUCK MODE)						
V_{COLD}	NTC cold temp (0°C) threshold, as percentage of VCC	Rising	72.4	73.3	74.2	%
		Falling	71.5	72	72.5	%
V_{COOL}	NTC cool temp threshold, ration as percentage of VCC	Rising	67.75	68.25	68.75	%
		Falling	66.45	66.95	67.45	%
V_{WARM}	NTC warm temp threshold , as percentage of VCC	Falling	44.25	44.75	45.25	%
		Rising	45.3	45.8	48.3	%
V_{HOT}	NTC hot temp (60°C) threshold, as percentage of VCC	Falling	33.7	34.2	34.7	%
		Rising	34.8	35.3	35.8	%
NTC (BOOST MODE)						
V_{BCOLD}	NTC cold temp (-25°C) threshold, as percentage of VCC	Rising	79.5	80	80.5	%
		Falling	78.5	79	79.5	%
V_{BHOT}	NTC hot temp (60°C) threshold, as percentage of VCC	Falling	29.7	31.2	32	%
		Rising	33.9	34.4	34.9	%
BOOST MODE OPERATION						
$V_{OTG\_REG\_RANGE}$	Boost mode regulation voltage range		3.9		5.4	V
$V_{OTG\_REG\_STEP}$	Boost mode regulation voltage step			100		mV
$V_{OTG\_REG\_ACC}$	Boost mode regulation voltage accuracy	V_{OTG_REG} =5V, V_{BAT}=3.8V, I_{BUS}=0A	4.85	5	5.15	V
		V_{OTG_REG} =5.2V, V_{BAT}=3.8V, I_{BUS}=0A	5.04	5.2	5.36	V
$V_{VBATLOW\_OTG}$	Battery voltage exiting boost mode	V_{VBAT} falling,2.8V	2.7	2.8	2.9	V
		Hysteresis		200		mV
		V_{VBAT} falling,2.5V	2.4	2.5	2.6	V
		Hysteresis		300		mV
I_{OTG}	OTG mode output current limit	I_{OTG} = 1.2A	1.2	1.4	1.6	A
		I_{OTG} = 0.5A	0.5	0.6	0.72	A

V_{OTG_OVP}	OTG overvoltage threshold	Rising		5.8		V
VCC LDO						
V_{VCC}	V_{CC} LDO output voltage	V_{BUS}=5V,I_{VCC}=40mA		4.5		V
I_{VCC}	V_{CC} current limiter	VBUS=5V, V_{VCC} = 3.8V,Charger disable	50			mA
LOGIC IO						
V_{ILO}	Input low threshold				0.4	V
V_{IHO}	Input high threshold		0.9			V
/QON TIMING						
$t_{SHIPMODE}$	/QON low time to turn on BATFET and exit ship mode		0.9		1.3	s
$t_{SHIPMODE\_DGL}$	Enter ship mode delay		10		15	s
t_{RESET}	/QON low time to reset BATFET		8		12	s
t_{RESET_LAST}	BATFET off time during full system reset		250		400	ms
DIGITAL CLOCK AND WATCHDOG TIMER						
t_{WDT}	Watchdog timer		20	40	60	s
f_{SCL}	SCL Clock frequency				400	KHz
SAFETY TIMER						
t_{TC}	Safety timer for Trickle charge		2	4	6	hours
$t_{CC/CV}$	Safety timer for CC and CV	12 hours	6	12	18	hours
VBUS Power up						
t_{VAC_OVP}	V_{BUS} OVP reaction time			150		ns
t_{BADSRC}	Bad adapter detection duration		15	30	45	ms
THERMAL REGULATION and SHUTDOWN						
T_{REG}	Thermal regulation temperature	Range	60		120	°C
		Step		20		°C
T_{SD}	Thermal shutdown temperature			150		°C
	Thermal shutdown hysteresis			30		°C

10 Feature Description

10.1 Power-On-Reset(POR)

The SC89601A powers internal bias circuits from the higher voltage of VBUS and VBAT. When VBUS rises above V_{VBUS_UVLO} or VBAT rises above V_{VBAT_UVLO} , the sleep comparator, battery depletion comparator and BATFET driver are active. I2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

10.2 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold , the BATFET turns on and connects battery to system. The VCC LDO stays off to minimize the quiescent current. The low R_{DSON} of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through BATFET (Supplement Mode). When the system is overloaded or shorted (I_{BAT} > I_{BATFET_OCP}), the device turns off BATFET immediately and set BATFET_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods described in BATFET Enable (Exit Shipping Mode) is applied to re-enable BATFET.

10.3 Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on VCC LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power up VCC LDO

2. Poor Source Qualification

3. Input Source Type Detection is based on DP/DM to set default input current limit (IINDPM) register or input source type

4. Input Voltage Limit Threshold Setting (VINDPM threshold)

5. Converter Power-up

10.3.1 Power Up VCC LDO Regulation

The VCC LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The VCC also provides bias rail to NTC external resistors. The pull-up rail of STAT can be connected to VCC as well. The VCC is enabled when all the below conditions are valid:

- V_{BUS} above $V_{VBUSMIN}$, above V_{BAT} + V_{SLEEP} in buck mode
- V_{BUS} below V_{BAT} + V_{SLEEP} in boost mode
- Above conditions are satisfied during 220ms delay

If any one of the above conditions is not valid, the device is in high impedance mode (HIZ) with VCC LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during HIZ state. The battery powers up the system when the device is in HIZ mode.

By setting EN_HIZ bit to 1 with adapter, the device enters high impedance state (HIZ). In HIZ mode, the system is powered from battery even with good adapter present. The device is in the low input quiescent current state with Q1 RBFET, VCC LDO and the bias circuits off.

10.3.2 Poor Source Qualification

After VCC LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements in order to start the buck converter:

- VAC voltage below V_{VAC_OV}
- VBUS voltage above $V_{VBUSMIN}$ when pulling I_{BADSRC} (typical 30 mA)

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the /INT pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

10.3.3 Input Source Type Detection

After the VBUS_GD bit is set and VCC LDO is powered, the device runs input source detection through DP/DM. The SC89601A follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input source (SDP/CDP/DCP) and non-standard adapter through USB DP/DM lines.

After input source type detection is completed, an INT pulse is asserted to the host. in addition, the following registers and pin are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit

2. PG_STAT bit is set

3. VBUS_STAT bit is updated to indicate USB or other input source

The host can over-write IINDPM register to change the input current limit if needed. The charger input current is always

limited by the IINDPM register.

The SC89601A contains a DP/DM based input source detection to set the input current limit at VBUS plug-in. The DP/DM detection includes standard USB BC1.2 and non-standard adapter. When input source is plugged in, the device starts standard USB BC1.2 detection. The USB BC1.2 is capable to identify Standard Downstream Port (SDP), Charging Downstream Port(CDP) and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer expires, the nonstandard adapter detection is applied to set the input current limit. The non-standard detection is used to distinguish vendor specific adapters based on their unique dividers on the DP/DM pins. If an adapter is detected as DCP, the input current limit is set at 2.4 A. If an adapter is detected as unknown, the input current limit is set at 0.5 A.

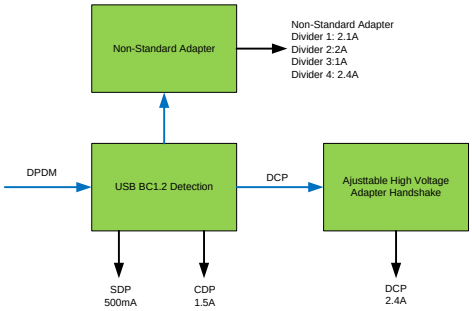


Figure 1 USB DP/DM Detection

D+/D- DETECTION	INPUT CURRENT LIMIT
USB SDP	500mA
USB CDP	1.5A
USB DCP	2.4A
Divider 1	2.1A
Divider 2	2A
Divider 3	1A
Divider 4	2.4A
Unknown Adapter	500mA

Table1 Input current limit setting from DP/DM Detection

After the input source detection, DP and DM return to HI-Z.

10.3.4 Input Voltage Limit Threshold Setting

The SC89601A supports wide range of input voltage limit. and provides three methods to set Input Voltage Limit (VINDPM) threshold to facilitate autonomous detection.

1. Absolute VINDPM (FORCE_VINDPM=1)

By setting FORCE_VINDPM bit to 1, the VINDPM threshold setting algorithm is disabled. Register VINDPM is writable and allows host to set the absolute threshold of VINDPM function.

2. Relative VINDPM based on VINDPM_OS registers (FORCE_VINDPM=0)

When FORCE_VINDPM bit is 0 (default), the VINDPM threshold setting algorithm is enabled. The VINDPM register is read only and the charger controls the register by using VINDPM Threshold setting algorithm(VBUS-VINDPM_OS).

FORCE_ VINDPM	VINDPM REGULATION VOLTAGE
0	VBUS-VINDPM_OS
1	Register VINDPM(0x0D[6:0])

Table2 VINDPM Function

10.3.5 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The SC89601A provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current is limited to is to the lower of 200 mA or IINDPM register setting. After the system rises above 2.2 V, the device limits input current to the value set by IINDPM register.

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The SC89601A switches to PFM control at light load or when battery is below minimum system voltage setting or charging is disabled.

10.4 Boost Mode Operation From Battery

The SC89601A supports boost converter operation to deliver

power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500 mA output requirement. The maximum output current is up to 1.4 A. The boost operation can be enabled if the conditions are valid:

1. VBAT above $V_{VBATLOW\_OTG}$

2. VBUS less than VBAT + V_{SLEEP}

3. Boost mode operation is enabled

4. Battery is not in BCOLD and BHOT.

5. Above conditions are satisfied during 30ms delay.

During boost mode, the status register VBUS_STAT bits is set to 111, the VBUS output is I2C programmed (default) and the output current can reach up to 1.4 A, selected through I2C (BOOST_LIM bit). The boost output is maintained when BAT is above $V_{VBATLOW\_OTG}$ threshold.

When OTG is enabled, the device starts up with PFM and later transits to PWM to minimize the overshoot. The PFM_DIS bit can be used to prevent PFM operation in either buck or boost configuration.

10.5 Host Mode and Default Mode

The SC89601A is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode.

When the charger is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings. in default mode, the device keeps charging the battery with default 10-hour fast charging safety timer. At the end of the 10-hour, the charging is stopped and the buck converter continues to operate to supply system load.

Writing a 1 to the WD_RST bit transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer expires (WATCHDOG_FAULT bit = 1), the device returns to default mode and all registers are reset to default values except IINDPM, VINDPM, BATFET_RST_EN, BATFET_DLY, and BATFET_DIS bits.

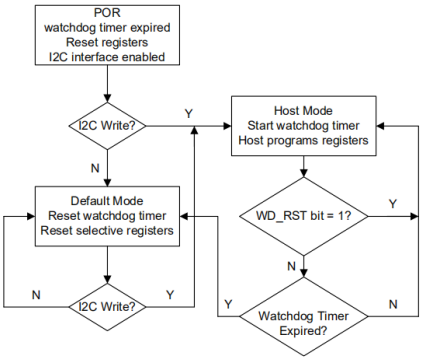


Figure 2 Watch dog

10.6 NVDC Power Path Management

The SC89601A accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (VSYS) from input source (VBUS), battery (VBAT), or both.

10.6.1 Battery Charging Management

The SC89601A charges 1-cell Li-Ion battery with up to 3.0-A charge current for high capacity tablet battery. The 11-mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

10.6.1.1 Autonomous Charging Cycle

With battery charging is enabled (CHG_CONFIG bit = 1 and /CE pin is LOW), the device autonomously completes a charging cycle without host involvement. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I2C.

Charging Parameters	Default Value
Charging Voltage	4.208V
CC Current	2.040A
TC Current	120mA
Termination Current	270mA
Battery Temperature Profile	JEITA
Safety Timer	TC:4hours, CC/CV:12hours

Table 3 Charging Parameter Default Setting

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled(CHG_CONFIG bit =1, I_{CC} is not 0A and /CE is low)

- No NTC COLD or HOT fault
- No safety timer fault
- BATFET is not forced to turn off(BATFET_DIS bit=0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold (selectable through VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, toggle CE pin or CHG_CONFIG bit can initiate a new charging cycle. Adapter removal and re plug will also start a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting EN_ICHG_MON bits = 11. in addition, the status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

STAT status	IC working status
Low	Normal charging (TC/CC/CV/Recharge)
High	End of charging (EOC, topoff timer maybe running) , charge disable, sleep mode, Boost Mode
1Hz Blinking	Charge suspend(VBUS OVP, NTC COLD/HOT, Safety timer out, system over voltage, VBAT OVP). Boost Mode suspend(NTC/COLD/HOT)

Table 4 STAT Pin status

10.6.1.2 Battery Charging Profile

The SC89601A charges the battery in six phases: battery short, TC,CC,CV,EOC and Recharge. At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

V_{VBAT}	Charging current	Default value	CHRG_STAT
<2.2V	I_{SHORT}	50mA	01
2.2V to 3V	I_{TC}	120mA	01
>3V	I_{CC}	2.040A	10

Table5 Charging Current Setting

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. in this case, termination is temporarily disabled and the charging safety timer is doubled.

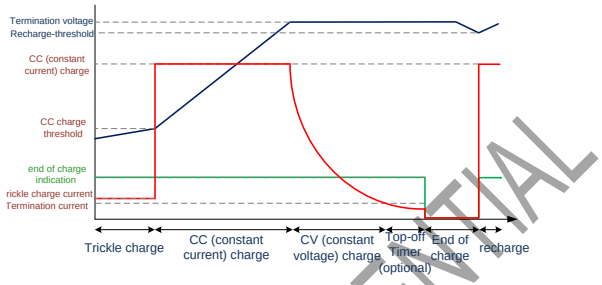


Figure 3 Battery Charging Profile

10.6.1.3 End of Charge

The SC89601A terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

When termination occurs, the status register CHRG_STAT is set to 11 and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

10.6.1.4 NTC in Buck mode

The SC89601A monitors the battery cells' temperature through NTC pin. It monitors the NTC voltage. Once it detects the temperature is below 0°C or higher than 60°C, the IC transitions to shutdown mode. Below shows the NTC operation summary. NTC function can be also disabled through shorting the pin to ground.

V_{NTC}	Temperature	Operation
$V_{NTC} > V_{COLD}$	T < 0°C	Stop charging
$V_{COLD} > V_{NTC} > V_{COOL}$	0°C < T < 10°C	$0.2*I_{CC}$
$V_{COOL} > V_{NTC} > V_{WARM}$	10°C < T < 45°C	Normal charging
$V_{WARM} > V_{NTC} > V_{HOT}$	45°C < T < 60°C	CV/4.1V
$V_{HOT} > V_{NTC} > V_{DISNTC}$	T > 60°C	Stop charging
$V_{DISNTC} > V_{NTC} >= 0$		Disable NTC

Table6 NTC Function

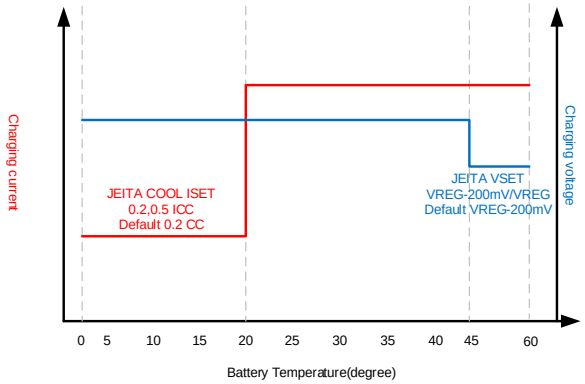


Figure 4 NTC function

10.6.1.5 NTC in Boost mode

For battery protection during boost mode, the SC89601A monitors the battery temperature to be within the V_{BCOLD} to V_{BHOT} thresholds. When temperature is outside of the temperature thresholds, the boost mode is suspended. In additional, VBUS_STAT bits are set to 000 and NTC_FAULT is reported. Once temperature returns within thresholds, the boost mode is recovered and NTC_FAULT is cleared.

10.6.1.6 Safety Timer

The SC89601A has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 4 hours when the battery is below V_{TC} threshold and 12 hours when the battery is higher than V_{TC} threshold.

The user can program CC/CV charge safety timer through I2C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled through I2C by setting EN_TIMER bit.

During input voltage, current, JEITA cool/warm or thermal regulation, the safety timer will double as the setting value.- The timer double function can be disable by writing 0 to TMR2X_EN bit.

During the fault(BAT_FAULT,NTC_FAULT), timer is suspended. Once the fault goes away, timer resumes. If user stops the current charging cycle, and start again, timer gets reset (toggle CE pin or CHRG_CONFIG bit).

10.6.2 NVDC Architecture

The SC89601A deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by V_{SYS_MIM} bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET.

When the battery charging is disabled and above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50mV above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

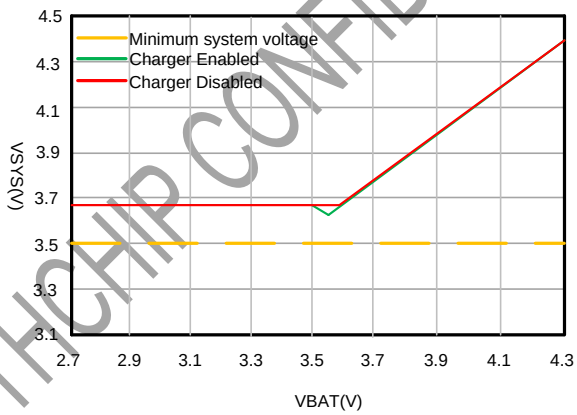


Figure 5 System Voltage vs Battery Voltage

10.6.3 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IIDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VDPM_STAT (VINDPM) or IDPM_STAT (IINDPM) goes high. Below figure shows the DPM response with 9-V/1.2-A adapter, 3.2-V battery, 2.8-A charge current and 3.5-V minimum system voltage setting.

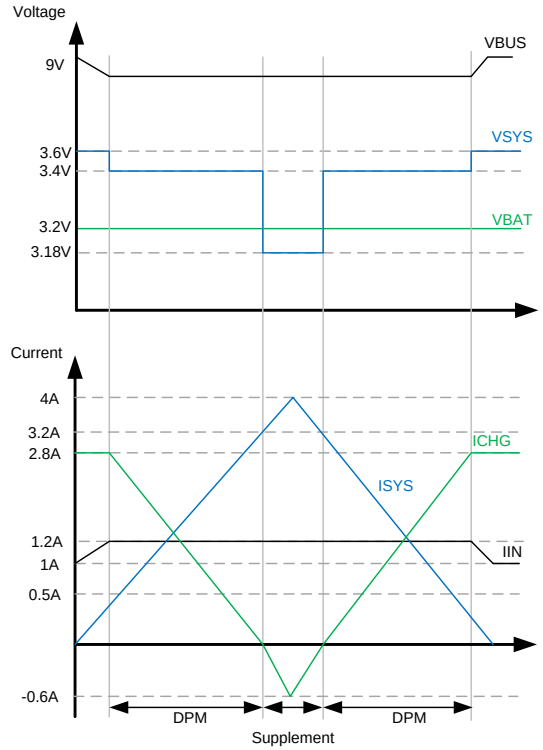


Figure 6 DPM Response

10.6.4 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET V_{DS} stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

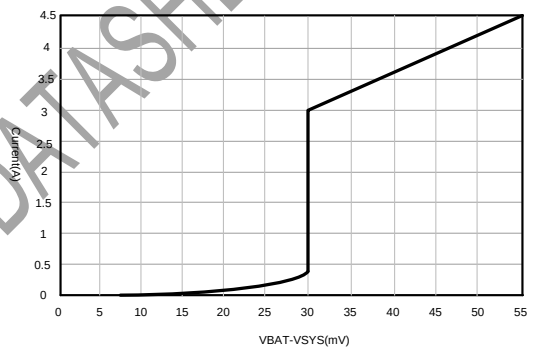


Figure 7 BATFET V-I Curve

10.7 Shipping Mode and /QON Pin

10.7.1 BATFET Disable Mode(Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configured by BATFET_DLY bit.

10.7.2 BATFET Enable(Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter

2. Clear BATFET_DIS bit

3. Set REG_RST bit to reset all registers including BATFET_DIS bit to be default 0

4. A logic high to low transition on /QON pin with $t_{SHIPMODE}$ deglitch time to enable BATFET to exit shipping mode

10.7.3 BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged–in. By changing the state of BATFET from on to off, systems connected to SYS can be effectively forced to have a power-on-reset. The /QON pin supports push-button interface to reset system power without host by changing the state of BATFET.

When the /QON pin is driven to logic low for t_{QON_RST} while input source is not plugged in and BATFET is enabled (BATFET_DIS = 0), the BATFET is turned off for t_{BATFET_RST} and then it is re-enabled to reset system power. This function can be disabled by setting BATFET_RST_EN bit to 0.

10.7.4 /QON Pin Operation

The /QON pin incorporates two functions to control BATFET.

1. BATFET Enable: A /QON logic transition from high to low with longer than $t_{SHIPMODE}$ deglitch turns on BATFET and exit shipping mode.

2. BATFET Reset: When /QON is driven to logic low by at least t_{QON_RST} while adapter is not plugged in (and BATFET_DIS = 0), the BATFET is turned off for t_{BATFET_RST}. The BATFET is re-enabled after t_{BATFET_RST} duration. This function allows systems connected to SYS to have power-on-reset. This function can be disabled by setting

BATFET_RST_EN bit to 0.

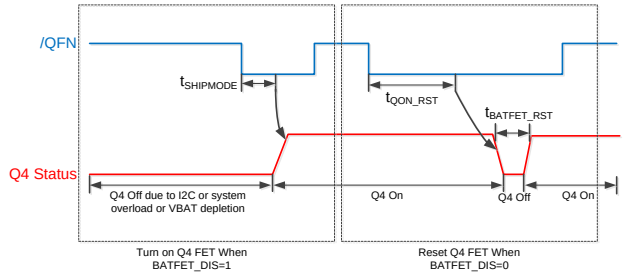


Figure 8 /QON Timing

10.8 Power Good Indicator

The PG_STAT bit goes HIGH to indicate a good input source when:

- VBUS above V_{VBUS_UVLO} below V_{VAC_OVP}
- VBUS above VBAT+V_{SLEEP} (not in sleep)
- VBUS above $V_{VBUSMin}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Completed input Source Type Detection

10.9 /INT

The SC89601A also has an alert mechanism that can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs low-state INT pulse. All of the below events can trigger an INT output:

- USB/adapter source identified
- Good input source detected as described in power good indicator
- Input Removed
- Charge Complete
- VINDPM/IINDPM event detected(can be masked)
- Watchdog timer out, Safety timer out, Boost fault (VBUS overload hiccup mode, VBUS OVP, VBAT < $V_{VBATLOW\_OTG}$), VBAT OVP, NTC COLD/HOT(Buck and Boost mode), Thermal shutdown, VBUS OVP, VBUS<$V_{VBUSMIN}$

When a fault occurs, the charger device sends out INT and keeps the fault state in REG until the host reads the fault register. The INT signal can be masked when the corresponding control bit is set. When a fault/status change occurs, the charger device sends out an INT pulse and keeps the state in REG0C until the host reads the registers. To read the current status, the host has to read REG0C two times consecutively. The first read reports the pre-existing register status and the second read reports the current register status.

10.10 Protections

10.10.1 Voltage and Current Monitoring in Buck Mode

10.10.1.1 Input Over voltage (ACOVP)

If VBUS voltage exceeds 14.2V, the device stops switching immediately. During input over voltage event (ACOV), the fault register CHRG_FAULT bits are set to 01. An INT pulse is asserted to the host. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold.

10.10.1.2 System Over voltage Protection(SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 350 mV above minimum system regulation voltage when the system is regulated at V_{SYS_MIN} and above battery regulation voltage when battery charging is terminated. Upon SYSOVP, converter stops switching immediately to clamp the overshoot. The charger provides 30 mA discharge current to bring down the system voltage.

10.10.2 Voltage and Current Monitoring in Boost Mode

10.10.2.1 VBUS Soft Start

When the boost function is enabled, the device soft-starts boost mode to avoid inrush current.

10.10.2.2 VBUS Over Load Protection

The device monitors boost output voltage and other conditions to provide output short circuit and over voltage protection. The Boost build in accurate constant current regulation to allow OTG to adaptive to various types of load. If short circuit is detected on VBUS, the Boost turns off and retry with hiccup function until the host to clear the OTG CFG.

10.10.2.3 VBUS Over Voltage Protection

When the VBUS voltage rises above regulation target and exceeds V_{OTG_OVP}, the device enters over voltage protection which stops switching, clears OTG_CONFIG bit and exits boost mode. At Boost over voltage duration, the fault register bit (BOOST_FAULT) is set high to indicate fault in boost operation. An INT is also asserted to the host.

10.10.3 Thermal Regulation and Thermal Shutdown

10.10.3.1 Thermal Protection in Buck Mode

The SC89601A monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds thermal regulation limit, the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT}. The fault register CHRG_FAULT is set to 1 and an INT is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is T_{SHUT_HYS} below T_{SHUT}.

10.10.3.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT}, the boost mode is disabled by setting OTG_CONFIG bit low and BATFET is turned off. When IC junction temperature is below T_{SHUT} - T_{SHUT_HYS}, the BATFET is enabled automatically to allow system to restart and the host can re-enable OTG_CONFIG bit to recover.

10.10.4 Battery Protection

10.10.4.1 Battery Over voltage Protection(VBATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charging. The fault register BAT_FAULT bit goes high and an INT is asserted to the host.

10.10.4.2 Battery Over discharge Protection

When battery is discharged below V_{BAT_DPL}, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge latch-off, an input source plug-in is required at VBUS. The battery is charged with I_{SHORT} (typically 50 mA) current when the VBAT < V_{SHORT}.

10.10.4.3 System Over current Protection

When the system is shorted or significantly overloaded (IBAT > I_{BATOCP}) and the current exceeds BATFET over current limit, the BATFET latches off. Section BATFET Enable (Exit Shipping Mode) can reset the latch-off condition and turn on BATFET.

10.11 I2C Interface

10.11.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x6B. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to 100kbits) and fast mode (up to 400k bits with 5 kΩ pull up resistor at SCL pin and SDA pin respectively).

10.11.2 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

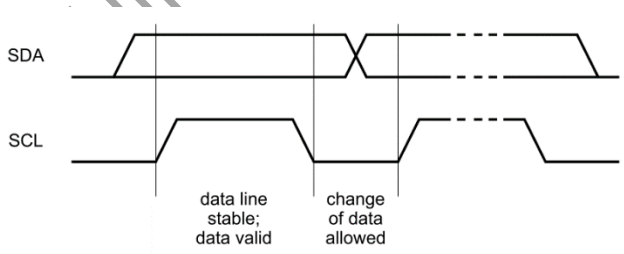


Figure9 Bit transfer on the I2C bus

10.11.3 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

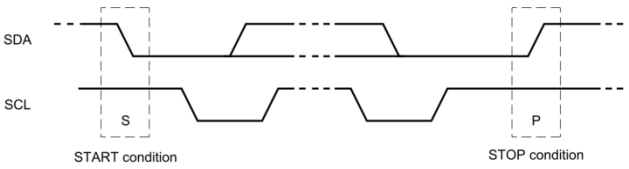


Figure 10 START and STOP conditions

10.11.4 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

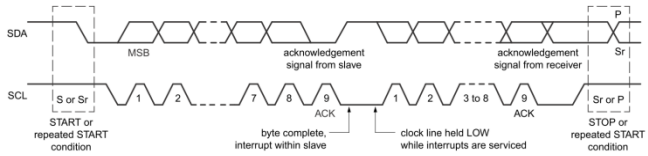


Figure 11 Data transfer on the I2C bus

10.11.5 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

10.11.6 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

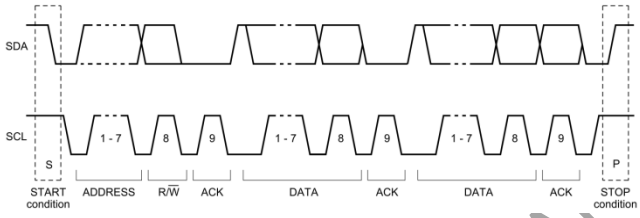


Figure 12 complete data transfer

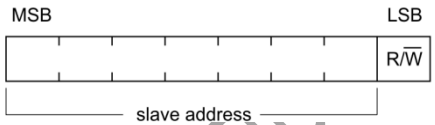


Figure 13 The first byte after the START procedure

10.11.7 Single Read and Write

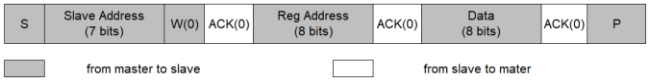


Figure 14 Single Write

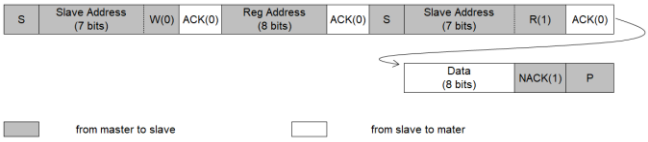


Figure 15 Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

10.11.8 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

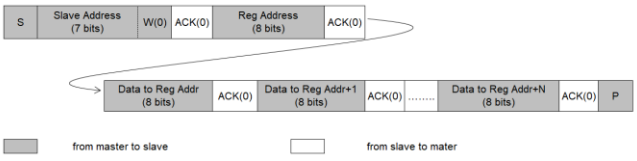


Figure 16 Multi-Write

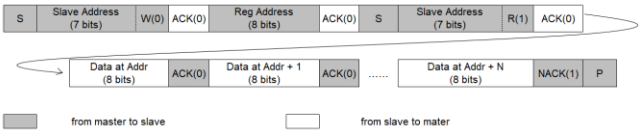


Figure 17 Multi-Read

11 Application information (TBD)

12 Register Map

Addr	Register	Type	Default value @POR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	INPUT CONTROL	R/W	0X001000	EN_HIZ	***RESERVED***	I_{IN_DPM}					
01H	DPDM CONTROL1	R/W	XXXXXXX1	***RESERVED***			***RESERVED***			***RESERVED***	VINDPM_OS
02H	DPDM CONTROL2	R/W	XXXXXX0X	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	FORCE_DPDM	***RESERVED***
03H	SYSTEM CONTROL1	R/W	X0011010	***RESERVED***	WD_RST	OTG_CFG	CHG_CFG	V_{SYS_MIN}			$V_{BAT\_OTG\_LOW}$
04H	ICC	R/W	XX100010	***RESERVED***	***RESERVED***	I_{CC}					
05H	ITC & ITERM	R/W	00010100	I_{TC}				I_{TERM}			
06H	VBAT_REG	R/W	01011110	V_{BAT_REG}						V_{BAT_LOW}	V_{RECHG}
07H	SYSTEM CONTROL2	R/W	10011101	EN_TERM	STAT_DIS	T_{WD}		EN_TIMER	T_{CHG}		JEITA_ISET
08H	TREG	R/W	XXXXXX11	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	TREG	
09H	SYSTEM CONTROL3	R/W	X10001XX	***RESERVED***	TMR2X_EN	BATFET_DIS	JEITA_ISET_WARM	BATFET_DLY	BATFET_RST_EN	***RESERVED***	***RESERVED***
0AH	BOOST CONTROL	R/W	10110011	V_{BOOST}				PFM_OTG_DIS	I_{BOOST}		
0BH	STAT1	R	XXXXXXXX	VBUS_STAT			CHRG_STAT		PG_STAT	***RESERVED***	VSYS_STAT
0CH	STAT2	R	XXXXXXXX	WD_FAULT	BOOST_FAULT	CHRG_FAULT		BAT_FAULT	NTC_FAULT		
0DH	VINDPM	R/W	00010010	FORCE_VINDPM	VINDPM						
0EH	STAT3	R	XXXXXXXX	THERMAL_STAT	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***
11H	STAT4	R	XXXXXXXX	VBUS_GD	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***
13H	STAT5	R	XXXXXXXX	VINDPM_STAT	IINDPM_STAT	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***	***RESERVED***
14H	PN	R	0X101XXX	REG_RST	***RESERVED***	PART NUMBER			***RESERVED***	***RESERVED***	***RESERVED***

REG 00H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	EN_HIZ	0	Y	Y	Enable HI-Z Mode 0: Disable 1: Enable	Reset to default value when input source is plugged-in
6	R/W	RESERVED					
5	R/W	I_{INDPM}	0	Y	N	1600mA	Input current limit Offset: 100 mA Range: 100 mA – 3.25A Default:2400 mA ,maximum input current limit, not typical. IINDPM bits are changed automatically after input source detection is completed Host can over-write IINDPM register bits after input source detection is completed.
4	R/W		0	Y	N	800mA	
3	R/W		1	Y	N	400mA	
2	R/W		0	Y	N	200mA	
1	R/W		0	Y	N	100mA	
0	R/W		0	Y	N	50mA	

REG 01H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	RESERVED					
6	R/W	RESERVED					
5	R/W	RESERVED					
4	R/W	RESERVED					
3	R/W	RESERVED					
2	R/W	RESERVED					
1	R/W	RESERVED					
0	R/W	VINDPM_OS	1	Y	N	VINDPM Offset 0: 400mV 1: 600mV	

REG 02H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	RESERVED					
6	R/W	RESERVED					
5	R/W	RESERVED					
4	R/W	RESERVED					
3	R/W	RESERVED					
2	R/W	RESERVED					
1	RW1C	FORCE_DPDM	0	Y	Y	Force DP/DM Detection 0: Not in DP/DM detection 1: Force DP/DM detection	
0	R/W	RESERVED					

REG 03H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	RESERVED					
6	RW1C	WD_RST	0	Y	Y	I2C Watchdog Timer Reset 0: Normal 1: Reset	
5	R/W	OTG_CFG	0	Y	Y	Boost Mode Configuration 0: OTG Disable 1: OTG Enable	
4	R/W	CHG_CFG	1	Y	Y	Charge Enable Configuration 0: Charge Disable 1: Charge Enable	
3	R/W	V_{SYS_MIN}	1	Y	N	000:2.6V 001:2.8V 010:3V 011:3.2V 100:3.4V 101:3.5V 110:3.6V 111:3.7V	
2	R/W		0	Y	N		
1	R/W		1	Y	N		
0	R/W	$V_{BAT\_OTG\_LOW}$	0	Y	Y	Minimum Battery Voltage (falling) to exit boost mode 0: 2.9V 1: 2.5V	

REG 04H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	RESERVED					
6	R/W	RESERVED					
5	R/W	I_{CC}	1	Y	Y	1920 mA	Fast Charge Current Offset: 0mA Range: 0mA – 3000mA Clamp to 3000mA
4	R/W		0	Y	Y	960 mA	
3	R/W		0	Y	Y	480 mA	
2	R/W		0	Y	Y	240 mA	
1	R/W		1	Y	Y	120 mA	
0	R/W		0	Y	Y	60 mA	

REG 05H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	I_{TC}	0	Y	Y	480 mA	Trickle Current Offset: 60mA Range: 60mA – 960mA
6	R/W		0	Y	Y	240 mA	
5	R/W		0	Y	Y	120 mA	
4	R/W		1	Y	Y	60 mA	
3	R/W	I_{TERM}	0	Y	Y	480 mA	Termination Current Offset: 30mA Range: 30mA – 930mA
2	R/W		1	Y	Y	240 mA	
1	R/W		0	Y	Y	120 mA	
0	R/W		0	Y	Y	60 mA	

REG 06H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	V_{BAT_REG}	0	Y	Y	512 mV	Charge Voltage Offset: 3.840V Range: 3.84V-4.848V
6	R/W		1	Y	Y	256 mV	
5	R/W		0	Y	Y	128 mV	
4	R/W		1	Y	Y	64 mV	
3	R/W		1	Y	Y	32 mV	
2	R/W		1	Y	Y	16 mV	
1	R/W	V_{BAT_LOW}	1	Y	Y	Battery TC to CC Charge Threshold 0: 2.8V 1: 3.0V	
0	R/W	V_{RECHG}	0	Y	Y	Battery Recharge Threshold (below Charge Voltage) 0: 100mV 1: 200mV	

REG 07H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	EN_TERM	1	Y	Y	Charging Termination Enable 0: Disable 1: Enable	
6	R/W	STAT_DIS	0	Y	Y	0: Enable STAT pin function 1: Disable STAT pin function	
5	R/W	T_{WD}	0	Y	Y	I2C Watchdog Timer Setting 00: Disable watchdog timer 01: 40s 10: 80s 11: 160s	
4	R/W		1	Y	Y		
3	R/W	EN_TIMER	1	Y	Y	Charging Safety Timer Enable 0: Disable 1: Enable	
2	R/W	T_{CHG}	1	Y	Y	Fast Charge Timer Setting 00: 5 hrs 01: 8 hrs 10: 12 hrs 11: 20 hrs	
1	R/W		0	Y	Y		
0	R/W	JEITA_ISET	1	Y	Y	JEITA Cool Temperature Current Setting 0: 50% of ICC 1: 20% of ICC	

REG 08H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	RESERVED					
6	R/W	RESERVED					
5	R/W	RESERVED					
4	R/W	RESERVED					
3	R/W	RESERVED					
2	R/W	RESERVED					
1	R/W	T_{REG}	1	Y	Y	Thermal Regulation 00: 60°C 01: 80°C 10: 100°C 11: 120°C	
0	R/W		1	Y	Y		

Reg 09H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	RESERVED					
6	R/W	TMR2X_EN	1	Y	Y	Safety Timer Setting during DPM or Thermal Regulation 0: Safety timer not slowed by 2X during input DPM or thermal regulation or JEITA 1: Safety timer slowed by 2X during input DPM or thermal regulation or JEITA	
5	R/W	BATFET_DIS	0	Y	N	0: Allow BATFET turn on 1: Turn off BATFET	
4	R/W	JEITA_VSET_WARM	0	Y	Y	JEITA Warm Temperature Voltage Setting 0: Set Charge Voltage to VREG-200mV during JEITA warm temperature 1: Set Charge Voltage to VREG during JEITA high temperature	
3	R/W	BATFET_DLY	0	Y	N	0: Turn off BATFET immediately when BATFET_DIS bit is set 1: Turn on BATFET after t_{BATFET_DLY} (typ. 10 s) when BATFET_DIS bit is set	
2	R/W	BATFET_RST_EN	1	Y	N	0: Disable BATFET reset function 1: Enable BATFET reset function	
1	R/W	RESERVED					
0	R/W	RESERVED					

Reg 0AH(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	V_{BOOST}	1	Y	Y	800 mV	Offset:3.9V Range:3.9V-5.4V
6	R/W		0	Y	Y	400 mV	
5	R/W		1	Y	Y	200 mV	
4	R/W		1	Y	Y	100 mV	
3	R/W	PFM_OTG_DIS	0	Y	N	PFM mode allowed in boost mode 0: Allow PFM in boost mode 1: Disable PFM in boost mode	
2	R/W	I_{BOOST}	0	Y	N	000: 0.5A 001: 0.75A 010: 1.2A 011: 1.4A 100: RESERVED 101: RESERVED 110: RESERVED 111: RESERVED	
1	R/W		1	Y	N		
0	R/W		1	Y	N		

Reg 0BH(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	VBUS STAT	X	NA	NA	VBUS Status register 000: No Input 001: USB Host SDP 010: USB CDP (1.5A) 011: USB DCP (3.25A) 100: RESERVED 101: Unknown Adapter (500mA) 110: Non-Standard Adapter (1A/2A/2.1A/2.4A) 111: OTG Note: Software current limit is reported in IINLIM register	
6	R		X	NA	NA		
5	R		X	NA	NA		
4	R	CHRG_STAT	X	NA	NA	Charging status: 00: Not Charging 01:TC Charging 10:CC Charging 11: Charge Termination	
3	R		X	NA	NA		
2	R	PG_STAT	X	NA	NA	Power Good status: 0: Power Not Good 1:Power Good	
1	R	RESERVED					
0	R	VSYS_STAT	X	NA	NA	0:Not in V_{SYS_MIN} regulation (BAT > V_{SYS_MIN}) 1:in V_{SYS_MIN} regulation (BAT < V_{SYS_MIN})	

Reg 0CH(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	WD_FAULT				0: Normal 1: Watchdog timer expiration	
6	R	BOOST_FAULT				0: Normal 1: VBUS overloaded in OTG, or VBUS OVP, or battery is too low (any conditions that we cannot start boost function)	
5	R	CHRG_FAULT				00: Normal; 01: input fault (VAC OVP or VBAT < VBUS < 3.8 V); 10: Thermal shutdown; 11: Charge Safety Timer Expiration	
4	R						
3	R	BAT_FAULT				0: Normal 1: BATOVP	
2	R	NTC_FAULT				NTC Fault Status Buck Mode: 000 – Normal 010 – TS Warm 011 – TS Cool 101 – TS Cold 110 – TS Hot Boost Mode: 000 – Normal 101 – TS Cold 110 – TS Hot	
1	R						
0	R						

Reg 0DH(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	FORCE_VINDPM	0	Y	N	VINDPM Threshold Setting Method 0: Run Relative VINDPM Threshold 1: Run Absolute VINDPM Threshold	Reset to default value when input source is plugged-in
6	R/W	VINDPM	0	Y	N	6400 mV	Absolute VINDPM Threshold Offset: 2.6V Effective Range: 3.9V-5V Reset to default value when input source is plugged-in
5	R/W		0	Y	N	3200 mV	
4	R/W		1	Y	N	1600 mV	
3	R/W		0	Y	N	800 mV	
2	R/W		0	Y	N	400 mV	
1	R/W		1	Y	N	200 mV	
0	R/W		0	Y	N	100 mV	

Reg 0EH(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	THERMAL_STAT	X	NA	NA	Thermal Regulation Status 0: Normal 1: In Thermal Regulation	
6	R	RESERVED					
5	R	RESERVED					
4	R	RESERVED					
3	R	RESERVED					
2	R	RESERVED					
1	R	RESERVED					
0	R	RESERVED					

Reg 11H(*Back to map*)

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	VBUS_GD	X	NA	NA	VBUS Good Status 0: Not VBUS attached 1: VBUS Attached	
6	R	RESERVED					
5	R	RESERVED					
4	R	RESERVED					
3	R	RESERVED					
2	R	RESERVED					
1	R	RESERVED					
0	R	RESERVED					

Reg 13H(*Back to map*)

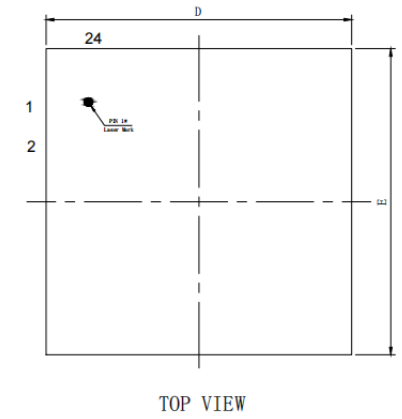
Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	VINDPM_STAT	X	NA	NA	VINDPM Status 0: Not in VINDPM 1: VINDPM	
6	R	IINDPM_STAT	X	NA	NA	IINDPM Status 0: Not in IINDPM 1: IINDPM	
5	R	RESERVED					
4	R	RESERVED					
3	R	RESERVED					
2	R	RESERVED					
1	R	RESERVED					
0	R	RESERVED					

Reg 14H(*Back to map*)

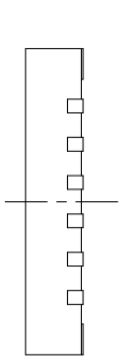
Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW1C	REG RST	0	NA	NA	Register Reset 0: Keep current register setting 1: Reset to default register value and reset safety timer	
6	R	RESERVED					
5	R	PN	1	NA	NA	Part Number	
4	R		0	NA	NA		
3	R		1	NA	NA		
2	R	RESERVED					
1	R	RESERVED					
0	R	RESERVED					

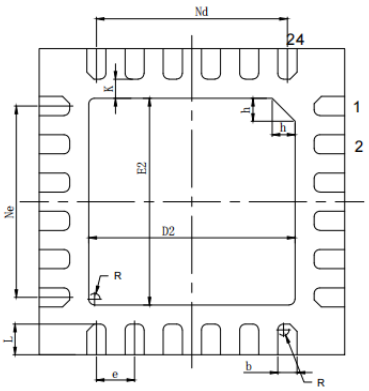
13 MECHANICAL DATA

QFN-24 4X4



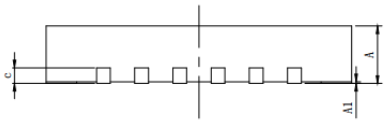
TOP VIEW





BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.50BSC		
Nd	2.50BSC		
Ne	2.50BSC		
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
h	0.25	0.30	0.35
K	0.25REF		
R	0.075REF		



SIDE VIEW

RECOMMENDED FOOTPRINT(Unit mm)