10/100 MBPS INTEGRATED PCI ETHERNET MEDIA ACCESS CONTROLLER AND PHYSICAL LAYER

DESCRIPTION

The SC92031 is a highly-integrated and cost-effective single-chip Fast Ethernet NIC controller. It fully complies with PCI 2.2 and IEEE 802.3u 100Base-T specifications. It supports both half-duplex and full -duplex operation, as well as for full-duplex flow control. It also supports Advanced Configuration Power management Interface (ACPI), PCI power management and remote wake-up events including AMD Magic Packet, Link Change, and Microsoft® wake-up frame.

The SC92031 provides glue less 32-bit bus master interface for PCI, boot ROM interface, as well as physical media interface for 100BASE-TX of IEEE 802.3u and 10BASE-T of 802.3. It also supports shared Boot ROM pins & clock run pin.

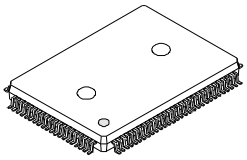
The SC92031 supports Analog Auto-Power-down, that is, the analog part of the SC92031 can be shut down temporarily according to user requirement or when the SC92031 is in a power down state with the wakeup function disabled.

PCI Vital Product Data (VPD) is also supported to provide the information that uniquely identifies hardware. The information may consist of part number, serial number, and other detailed information.

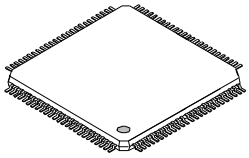
To provide cost down, the SC92031 is capable of using a 25MHz crystal or OSC as its internal clock source.

The SC92031 includes a PCI and Expansion Memory Share Interface for a boot ROM and can be used in diskless workstations, providing maximum network security and ease of management.

The SC92031 provides a flexible multi-function mode to incorporate other PCI master devices. When in multi-function mode, the SC92031 acts as an arbiter to distinguish LAN signals from those of other devices.



QFP-100-14x20-0.65



LQFP-100-14x14-0.5

ORDERING INFORMATION

Device	Package
SC92031	QFP-100-14 X 20-0.65
SC92031L	LQFP-100-14 X 14-0.5

APPLICATIONS

* 10/100Mbps PCI fast Ethernet adaptor

FEATURES

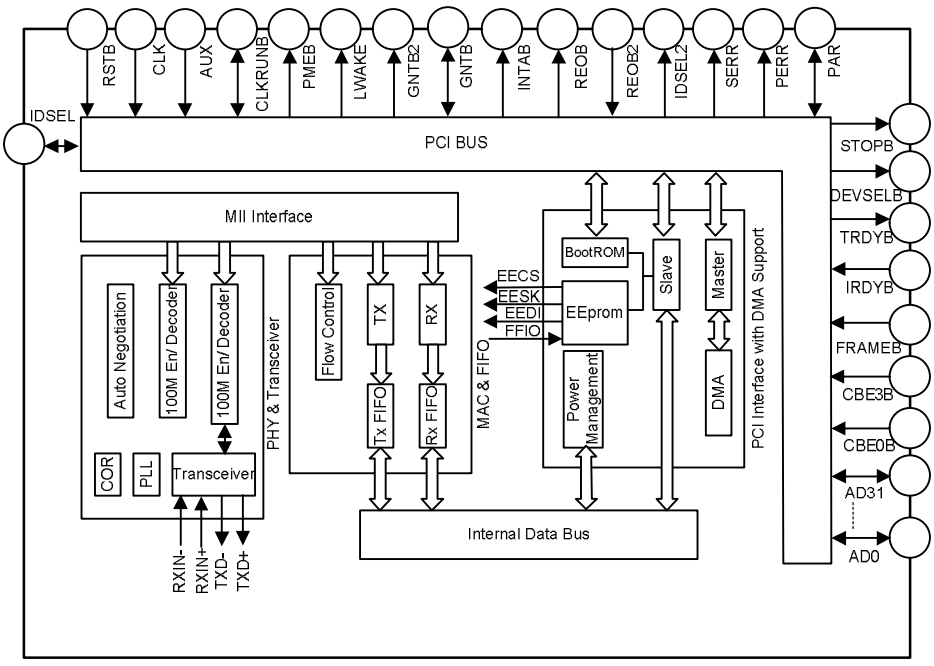
* Integrated Fast Ethernet MAC, Physical layer and transceiver in one chip
* 10 Mbps and 100 Mbps data rates
* Both half duplex and full duplex available
* IEEE 802.3 compliant Auto-Negotiation
* Supports PCI multi-function capabilities
* PCI local bus
  - Ø Compliant to PCI Revision 2.2
  - Ø Supports PCI clock 15 MHz-40 MHz
  - Ø Supports PCI target fast back-to-back transaction
  - Ø Provides PCI bus master data transfers and PCI memory space or I/O space mapped data transfers of

SC92031's operational registers

- Ø Supports PCI VPD (Vital Product Data)
- Ø Supports ACPI 1.0 and PCI power management Ver.1.1 compliant
- Ø Supports PCI multi-function to incorporate with other PCI master device

* Supports 25MHz crystal or 25MHz OSC as the internal clock source.
* Compliant to PC99 and PC2001 standards
* Supports Wake-On-LAN function and remote wake-up (Magic Packet*, Link Change and Microsoft® wake-up frame)
* Supports 4 Wake-On-LAN (WOL) signals (active high, active low, positive pulse, and negative pulse)
* Supports auxiliary power auto-detect, and sets the related capability of power management registers in PCI configuration space
* Includes a programmable, PCI burst size and early Tx/Rx threshold
* Supports a 32-bit general-purpose timer with the external PCI clock as clock source, to generate timer-interrupt
* Contains two large (2Kbyte) independent receive and transmit FIFOs
* Advanced power saving mode when LAN function or wakeup function is not used
* Uses serial EEPROM to store resource configuration, ID parameter, and VPD data
* Extensive LED status support
* Supports loop back capability
* Supports Full Duplex Flow Control
* Low-power 0.25u CMOS technology
* 3.3V power supply with 5V tolerant I/Os
* 100-pin QFP/LQFP package
* Third-party brands and names are the property of their respective owners.

BLOCK DIAGRAM



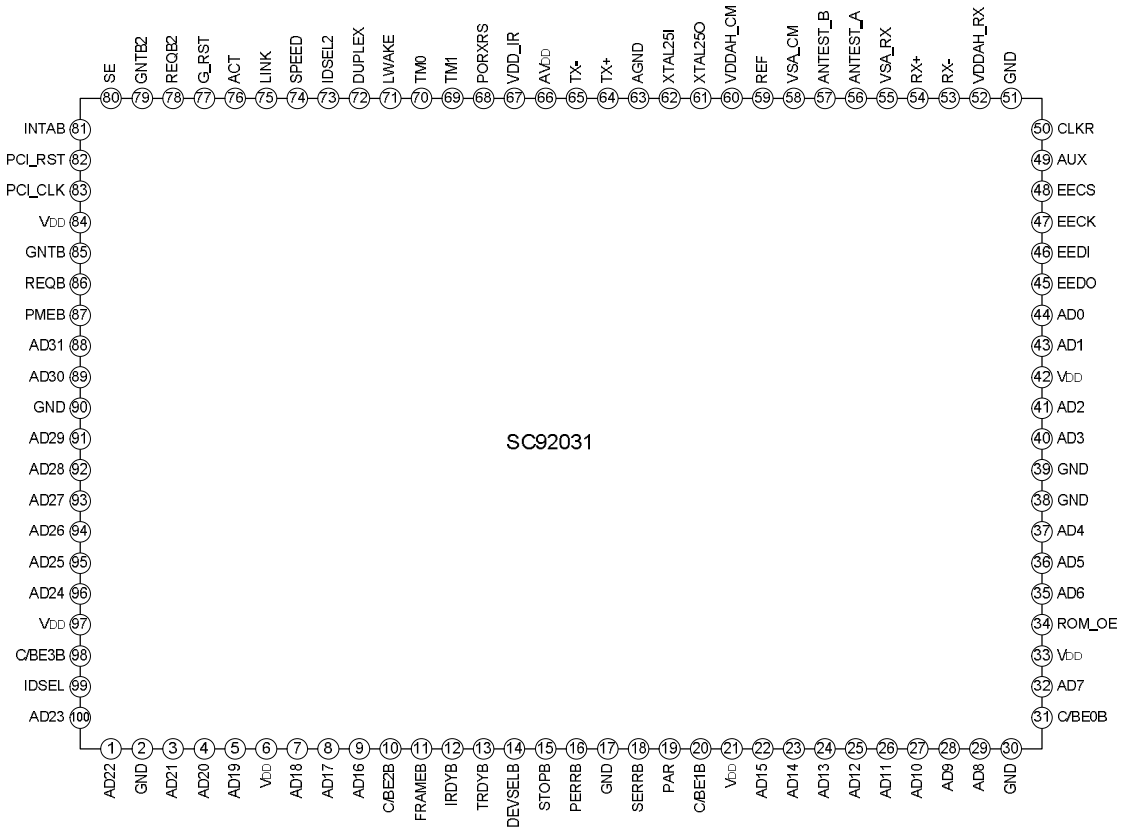
ABSOLUTE MAXIMUM RATINGS (unless otherwise stated, T_{amb}=25°C, V_{SS}=0V)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	0 ~ 4.0	V
Input/Output Voltage	V_I , V_O	-0.5 ~ V_{DD}+0.5	V
Operating Temperature	T_{opr}	0 ~ 70	℃
Storage Temperature	T_{stg}	-40 ~ 125	℃

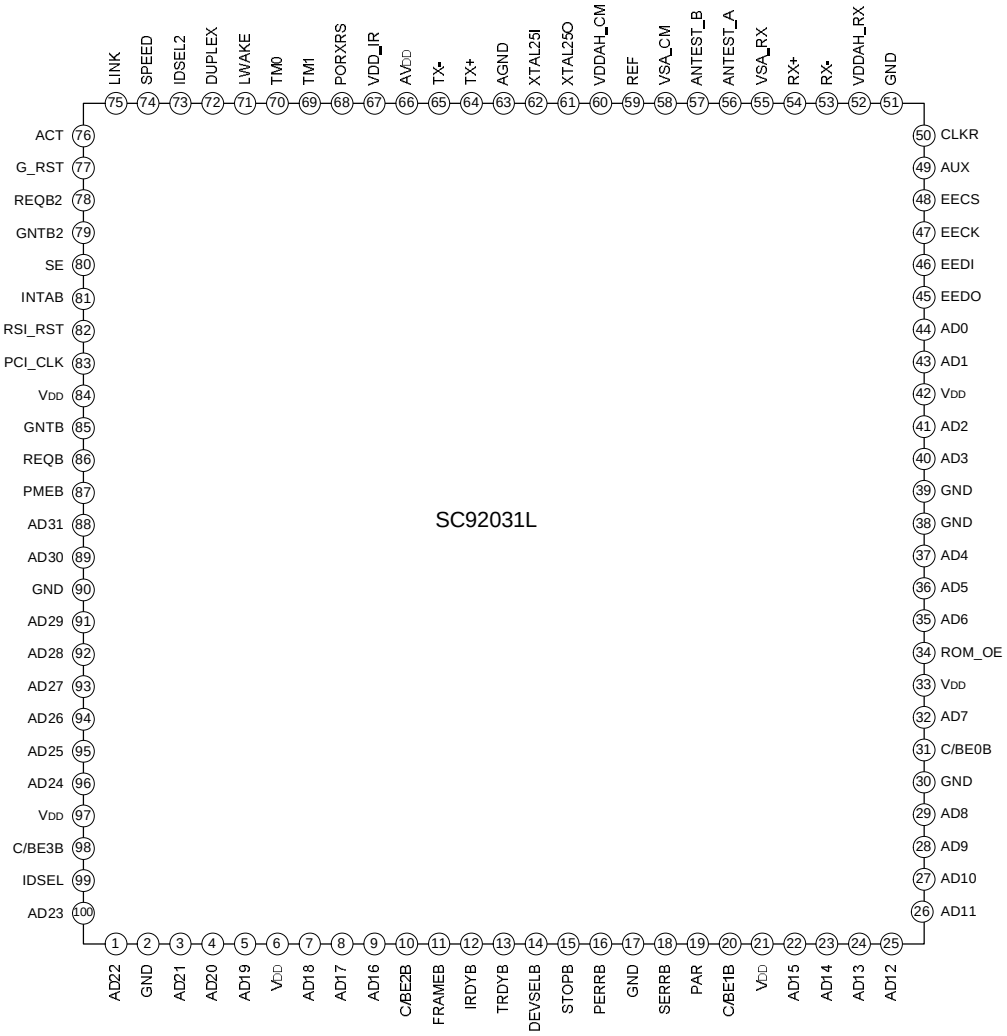
DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply voltage V_{DD}=3.0V min. to 3.6V max.						
Minimum High Level Output Voltage	V_{OH}	I_{OH}=-8mA	0.9V_{DD}		V_{DD}	V
Maximum Low Level Output Voltage	V_{OL}	I_{OL}=8mA			0.1V_{DD}	V
Minimum High Level Input Voltage	V_{IH}		0.5V_{DD}		V_{DD}+0.5	V
Minimum Low Level Input Voltage	V_{IL}		-0.5		0.3V_{DD}	V
Input Current	I_{IN}	V_{IN}=V_{DD} or GND	-1.0		1.0	μA
Tri-state Output Leakage Current	I_{OZ}	V_{OUT}=V_{DD} or GND	-1.0		10	μA
Average operating Supply Current	I_{CC}	I_{OUT}=0mA			330	mA

PIN CONFIGURATION



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Symbol	Description
PCI Interface		
82	PCI_RST	When RSTB is asserted low, the SC92031 performs internal system hardware reset. RSTB must be held for a minimum of 120 ns.
83	PCI_CLK	This PCI Bus clock provides timing for all transactions and bus phases, and is input to PCI devices. The rising edge defines the start of each phase. The clock frequency ranges from 0 to 33MHz.
88, 89, 91-96, 100, 1, 3-5, 7-9, 22-29, 32, 35-37, 40, 41, 43, 44	AD31-0	PCI address and data multiplexed pins. Pins AD31-24 are shared with Boot ROM data pins, while AD16-0 are shared with Boot ROM address pins.

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Pin No.	Symbol	Description
98, 10, 20, 31	C/BE3-0B	PCI bus command and byte enables.
14	DEVSELB	Device Select, target is driving to indicate the address is decoded.
11	FRAMEB	Begin and duration of bus access, driven by master device.
85	GNTB	PCI bus granted. This signal indicates that the PCI bus request of SC92031 has been accepted.
86	REQB	PCI bus request, the SC92031 will assert this signal low to request the ownership of the bus from the central arbiter.
99	IDSEL	Initialization Device Select. This pin allows the SC92031 to identify when configuration read/write transactions are intended for it.
81	INTAB	PCI interrupt request. It is asserted low when an interrupt condition occurs, as defined by the Interrupt Status, Interrupt Mask and Interrupt Enable registers.
12	IRDYB	Master device is ready to data transaction.
13	TRDYB	Slave device is ready to data transaction.
19	PAR	Parity, this signal indicates even parity across AD31-0 and C/BE3-0 including the PAR pin. As a master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.
16	PERRB	Data parity error is detected, driven by the agent receiving data.
18	SERRB	Address parity error.
15	STOPB	The current target is requesting the master to stop the current transaction.
Power Management/Isolation Interface		
87	PMEB	Power Management Event, Open drain, active low. Used by the SC92031 to request a change in its current power management state and/or to indicate that a power management event has occurred.
71	LWAKE	LAN WAKE-UP signal, This signal is used to inform the motherboard to execute the wake-up process. The motherboard must support Wake-On-LAN (WOL). There are 4 choices of output, including active high, active low, positive pulse, and negative pulse, that may be asserted from the LWAKE pin.
EEPROM Interface		
49	AUX	This pin is used to notify the SC92031 of the existence of Aux. power during initial power-on or a PCI reset. This pin should be pulled high to the Aux. power via a resistor to detect the Aux. power. Doing so, will enable wakeup support from ACPI D3 cold or APM power-down. If this pin is not pulled high, the SC92031 assumes that no Aux. power exists.
EEPROM Interface		
47	EECK	EEPROM chip serial clock
46	EEDI	EEPROM chip serial data in
45	EEDO	EEPROM chip serial data out
48	EECS	EEPROM chip select

(To be continued)

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Pin No.	Symbol	Description
Power Pins		
6,21,33,42, 84,97	VDD	+3.3V (Digital)
67	VDD_IR	
52,60,66	VDDAH_RX VDDAH_CM AVDD	+3.3V (Analog)
2,17, 30,38,39, 51	GND	Ground
55, 58, 63	VSA_RX VSA_CM AGND	Ground (Analog)
LED Interface		
76,75,74,72	ACT, LINK, SPEED,DUPLEX	LED0 displays for activity status. This pin will be driven with 5 Hz frequency when either effective receiving or transmitting is detected. LED1 displays for link status. LED2 displays for 100 M link status. LED3 displays for full-duplex mode.
64 65	TX+ TX-	100/10BASE-T transmit (Tx) data
54 53	RX+ RX-	100/10BASE-T receive (Rx) data
62	XTAL25I	25 MHz crystal/OSC. Input
61	XTAL25O	Crystal feedback output, This output is used in crystal connection only. It must be left open when X1 is driven with an external 25 MHz oscillator.
Multi-Function Interface		
78	REQB2	Request2, The 2nd device will assert this pin low to request the ownership of the PCI bus.
79	GNTB2	Grant2, This signal is asserted low to indicate that the central arbiter has granted ownership of the bus to the 2nd device.
73	IDSEL2	Initialization device select 2, Used as a chip-select during configuration read and write transactions to the 2nd device.
Test And Other Pins		
70 69	TM0 TM1	Chip test pin
34	ROM_OE	ROM Chip Select and Output Enable, This is the chip select signal and output enable for the Boot PROM.

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Pin No.	Symbol	Description
50	CLKR	Clock run for PCI system. In normal operation situation, Host should assert this signal to indicate SC92031 about the normal situation. On the other hand, when the host will dessert this signal when the clock is going down to a non-operating frequency. When SC92031 recognizes the de-asserted status of clockrun, then it will assert clockrun to request host to maintain the normal clock operation. When clockrun function is disabled then the SC92031 will set clockrun in tri-state.
80	SE	Scan chain test enable
56 57	ANTEST_A ANTEST_B	Analog test pin
68	PORXRS	Power on reset output
77	G_RST	Global reset input pin

REGISTER DESCRIPTION

The chip provides the following set of operational registers mapped into PCI memory space or I/O space.

Offset	R/W	Tag	Bit Width	Description
0x00	R/W	CONFIG0	32	Software Reset
0x04	R/W	CONFIG1	32	Select Rx Buffer Size
0x08	R	RBW_PTR	32	Rx buffer write pointer
0x0C	R	INT_STATUS	32	Interrupt status register
0x10	R/W	INT_MASK	32	Interrupt mask register
0x14	R/W	RBSA	32	Rx buffer start address
0x18	R/W	RBR_PTR	32	Rx buffer read pointer
0x1C	R	TX_STATUS	32	Transmit Status of All Descriptors
0x20	R	TX_ STATUS0	32	Transmit Status of Descriptor 0
0x24	R	TX_ STATUS1	32	Transmit Status of Descriptor 1
0x28	R	TX_ STATUS2	32	Transmit Status of Descriptor 2
0x2C	R	TX_ STATUS3	32	Transmit Status of Descriptor 3
0x30	R/W	TX_ADDR0	32	Transmit Start Address of Descriptor 0
0x34	R/W	TX_ADDR1	32	Transmit Start Address of Descriptor 1
0x38	R/W	TX_ADDR2	32	Transmit Start Address of Descriptor 2
0x3C	R/W	TX_ADDR3	32	Transmit Start Address of Descriptor 3
0x40	R/W	RX_CONFIG	32	Receive Configuration Register
0x44	R/W	MAC_ADDR0	32	MAC Address 0
0x48	R/W	MAC_ADDR1	32	MAC Address 1
0x4C	R/W	MULTI_GROUP0	32	Multicast Group 0
0x50	R/W	MULTI_GROUP1	32	Multicast Group 1
0x54	R	RX_STATUS0	32	Receive Status Register 0
0x58	-	-	32	Reserved

(To be continued)

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Offset	R/W	Tag	Bit Width	Description
0x5C	R/W	TX_CONFIGURATION	32	Transmit Configuration Register
0x60	-	-	32	Reserved
0x64	R/W	FLOW_CONTROL	32	Flow Control Configuration Register
0x68	R/W	MIIM_COMMAND0	32	MIIM Command Register 0
0x6C	R/W	MIIM_COMMAND1	32	MIIM Command Register 1
0x70	R	MIIM_STATUS	32	MIIM Status Register
0x74	R/W	TimerCnt	32	Timer Counter Register
0x78	R/W	TimerInt	32	Timer Interrupt Register
0x7C	R/W	PM_CONFIG	32	Power Management configuration register
0x80	R/W	CRC	32	Power Management CRC reg - crc3~crc0
0x84	R/W	CRC	32	Power Management CRC reg - crc7~crc4
0x88	R/W	WAKEUP0	32	Power Management reg - wakeup0[31:0]
0x8C	R/W	WAKEUP0	32	Power Management reg - wakeup0[63:32]
0x90	R/W	WAKEUP1	32	Power Management reg - wakeup1[31:0]
0x94	R/W	WAKEUP1	32	Power Management reg – wakeup1[63:32]
0x98	R/W	WAKEUP2	32	Power Management reg – wakeup2[31:0]
0x9C	R/W	WAKEUP2	32	Power Management reg – wakeup2[63:32]
0xA0	R/W	WAKEUP3	32	Power Management reg – wakeup3[31:0]
0xA4	R/W	WAKEUP3	32	Power Management reg – wakeup3[63:32]
0xA8	R/W	WAKEUP4	32	Power Management reg – wakeup4[31:0]
0xAC	R/W	WAKEUP4	32	Power Management reg – wakeup4[63:32]
0xB0	R/W	WAKEUP5	32	Power Management reg – wakeup5[31:0]
0xB4	R/W	WAKEUP5	32	Power Management reg – wakeup5[63:32]
0xB8	R/W	WAKEUP6	32	Power Management reg – wakeup6[31:0]
0xBC	R/W	WAKEUP6	32	Power Management reg – wakeup6[63:32]
0xC0	R/W	WAKEUP7	32	Power Management reg – wakeup7[31:0]
0xC4	R/W	WAKEUP7	32	Power Management reg – wakeup7[63:32]
0xC8	R/W	LastByte	32	Power Management Lastbyte reg
0xCC	R/W	LastByte	32	Power Management Lastbyte reg
0xD0	-	-	32	Reserved
0xD4	-	-	32	Reserved
0xD8	-	-	32	Reserved
0xDC	-	-	32	Reserved
0xE0	-	-	32	Reserved
0xE4	-	-	32	Reserved
0xE8	-	-	32	Reserved
0xEC	-	-	32	Reserved
0xF0	-	-	32	Reserved
0xF4	-	-	32	Reserved
0xF8	-	-	32	Reserved
0xFC	-	-	32	Reserved

1 Config 0: Configuration Register 0 (Offset 0000h, R/W)

Bit	R/W	Symbol	Description
31	R/W	Software Reset	Reset: Setting to 1 forces the chip to a software reset state which disables the transmitter and receiver, reinitializes the FIFOs, resets the system buffer pointer to the initial value (Tx buffer is at TSAD0, Rx buffer is empty). The values of IDR0-5 and MAR0-7 and PCI configuration space will have no changes. This bit is 1 during the reset operation, and is cleared to 0 by the driver when the reset operation is complete.
30	R/W	Analog Power Down	Analog Power Down: 1: Turn off the analog power of the chip internally. 0: Normal working state. This is also power-on default value.
29	R/W	Power Saving	Power Saving Mode: 1: Disable. 0: Enable. When cable is disconnected, the analog part will power down itself automatically except PHY Rx part and part of twister to monitor SD signal in case that cable is re-connected and Link should be established again.
28-0	-	-	Reserved

2 Config 1: Configuration Register 1 (Offset 0004h, R/W)

Bit	R/W	Symbol	Description
31	R/W	Early Reception	Set to 1 indicates enable early reception
30	R/W	Early Transmission	Set to 1 enable early transmission when reach TX threshold
29-24	-	-	Reserved
23-21	R/W	Rx FIFO Threshold	Rx FIFO Threshold: Specifies Rx FIFO Threshold level. When the number of the received data bytes from a packet, which is being received into Rx FIFO, has reached to this level (or the FIFO has contained a complete packet), the receive PCI bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following fomula: Threshold_Level = 16 * 2 ** Rx_FIFO_Threshold The chip begins the transfer of data after having received a whole packet in the FIFO.
20-4	-	-	Reserved
3-0	R/W	Rx Buffer Length	Rx Buffer Length: This field indicates the size of the Rx ring buffer. 0000 = 8k Bytes 0001 = 16k Bytes 0011 = 32k Bytes 0111 = 64k Bytes 1111 = 128k Bytes

3 Interrupt Status Register (Offset 000Ch, R)

The interrupt Status Register reflects all current pending interrupts, regardless of the state of the corresponding mask bit in the IMR. Reading the ISR clears all interrupts. Writing to the ISR has no effect.

Bit	R/W	Symbol	Description
31	R	Link fail	Link Status is changed to Failure
30	R	Link OK	Link Status is changed to Success
29	R	Time Out	Time Out: Set to 1 when the TCTR register reaches to the value of the TimerInt register.
28-7	-	-	Reserved
6	R	Rx Buffer Overflow	Receive Buffer Overflow
5	R	Rx OK	Receive OK
4-1	-	-	Reserved
0	R	Tx OK	Transmit OK

4 Interrupt Mask Register (Offset 0010h, R/W)

Bit	R/W	Symbol	Description
31	R	Link fail	Link Fail Interrupt: 1 => Enable, 0 => Disable.
30	R	Link OK	Link OK Interrupt: 1 => Enable, 0 => Disable.
29	R	Time Out	Time Out Interrupt: 1 => Enable, 0 => Disable.
28-7	-	-	Reserved
6	R	Rx Buffer Overflow	Receive Buffer Overflow: 1 => Enable, 0 => Disable.
5	R	Rx OK	Receive OK Interrupt: 1 => Enable, 0 => Disable.
4-1	-	-	Reserved
0	R	Tx OK	Transmit OK Interrupt: 1 => Enable, 0 => Disable.

5 Receive Buffer Start Address Register (Offset 0014h, R/W)

Bit	R/W	Symbol	Description
31-0	R/W	RBSTART	Receive Buffer Start Address

6 TX_STATUS: Transmit Status of All Descriptors (Offset 001Ch, R)

Bit	R/W	Symbol	Description
31-16	-	-	Reserved
15	R	TOK3	TOK bit of Descriptor3
14	R	TOK2	TOK bit of Descriptor2
13	R	TOK1	TOK bit of Descriptor1
12	R	TOK0	TOK bit of Descriptor0
11	R	TUN3	TUN bit of Descriptor3
10	R	TUN2	TUN bit of Descriptor2
9	R	TUN1	TUN bit of Descriptor1
8	R	TUN0	TUN bit of Descriptor0
7	R	TABT3	TABT bit of Descriptor3

(To be continued)

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Bit	R/W	Symbol	Description
6	R	TABT2	TABT bit of Descriptor2
5	R	TABT1	TABT bit of Descriptor1
4	R	TABT0	TABT bit of Descriptor0
3	R	OWN3	OWN bit of Descriptor3
2	R	OWN2	OWN bit of Descriptor2
1	R	OWN1	OWN bit of Descriptor1
0	R	OWN0	OWN bit of Descriptor0

7 Tansmit Status Register (TX_STATUS0-3)(Offset 0020h-002Fh, R/W)

The read-only bits will be cleared by the chip when the Transmit Byte Count (bits 12-0) in the corresponding Tx descriptor is written. It is not affected when software writes to these bits.

Bit	R/W	Symbol	Description
31-30	-	-	Reserved
29	R	CRS	Carrier Sense Lost: This bit is set to 1 when the carrier is lost during transmission of a packet.
28	R	TABT	Transmit Abort: This bit is set to 1 if the transmission of a packet was aborted.
27	R	Later Collision	Later Collision: This bit is set to 1 if the chip encountered an later collision during the transmission of a packet.
26	-	-	Reserved
25-22	R	Collision Counter	Collision Count: Indicates the number of collisions encountered during the transmission of a packet.
21-16	R/W	Early Tx Threshold	Early Tx Threshold: Specifies the threshold level in the Tx FIFO to begin the transmission. When the byte count of the data in the Tx FIFO reaches this level, (or the FIFO contains at least one complete packet) the chip will transmit this packet. These fields count from 000001 to 111111 in unit of 32 bytes.
15	R	TOK	Transmit Success: This bit is set to 1 if the transmission of a packet was successed.
14	R	TUN	Tx FIFO Underrun: Set to 1 if the Tx FIFO was exhausted during the transmission of a packet.
13	R/W	OWN	OWN: The chip sets this bit to 1 when the Tx DMA operation of this descriptor was completed. The driver must set this bit to 0 when the Transmit Byte Count (bits 0-12) is written. The default value is 1.
12-0	R/W	SIZE	Descriptor Size: The total size in bytes of the data in this descriptor.

8 Tansmit Start Address of Descriptor Register (TX_ADDR0-3)(Offset 0030h-003Fh, R/W)

Bit	R/W	Symbol	Description
31-0	R/W	TSAD	Transmit Start Address of Descriptor

9 Receive Configuration Register (Offset 0040h, R/W)

Bit	R/W	Symbol	Description
31	R/W	Rx_FullDX	Set to 1 indicates work in full duplex mode
30	R/W	En_Rx	Receive Enable
29	R/W	Rcv Small	Set to 1 indicates receive small packets (less than 64 bytes)
28	R/W	Rcv_Huge	Set to 1 indicates receive long packets (more than 1518 bytes)
27	R/W	Rcv_Error_Frame	Set to 1 indicates receive error packets
26	R/W	Rcv_All	Set to 1 indicates receive all packets seen
25	R/W	Rcv_Multi	Set to 1 indicates receive multicast packets
24	R/W	Rcv_Broad	Set to 1 indicates receive broadcast packets
23-22	R/W	Lp_Bck	“00” indicates normal mode, else indicates loop back mode
21-12	R/W	Low_Threshold	Low Threshold of Rx FIFO
11-2	R/W	High_Threshold	High Threshold of Rx FIFO
1-0	-	-	Reserved

10 MAC Address Register (Offset 0044h-004Bh, R/W)

Bit	R/W	Symbol	Description
63-16	R/W	Eth_Addr	Ethernet MAC Address
15-0	-	-	Reserved

11 Multicast Address Group Register (Offset 004Ch-0053h, R/W)

Bit	R/W	Symbol	Description
63-0	R/W	Multi_Group	Multicast Address Group Configuration Register

12 Receive Status Register 0 (Offset 0054h, R)

Bit	R/W	Symbol	Description
31-17	R	FIFO_Over_Cnt	FIFO Overflow Counter
15-0	R	Lost_Cnt	Rx Lost Frame Counter

13 Transmit Configuration Register (Offset 005Ch, R/W)

Bit	R/W	Symbol	Description
31	R/W	Tx_Fulldx	Set to 1 indicates work in full duplex mode
30	R/W	En_Tx	Transmit Enable
29	R/W	En_PAD	Set to 1 indicates PAD when transmit small packets
28	R/W	En_Huge	Set to 1 indicates enable long packets transmission
27	R/W	En_FCS	Setting to 1 means that there is CRC appended at the end of a packet.
26	R/W	No_Backoff	Set to 1 indicates retransmit at once after a collision
25	R/W	En_Premble	Set to 1 indicates always transmit preamble before valid data
24-0	-	-	Reserved

14 Flow Control Configuration Register (Offset 0064h, R/W)

Bit	R/W	Symbol	Description
31	R/W	Fulldx	Set to 1 indicates work in full duplex mode
30	R/W	En_FC	Enable Flow Control
29	R/W	PASSALL	Set to 1 indicates that flow control function is implemented by software
28	R/W	En_Pause	Set to 1 indicates prohibit send packets
27	R/W	Tx_Pause_F	Set to 1 will send a PAUSE packet with parameter FFFF
26	R/W	Tx_Pause_0	Set to 1 will send a PAUSE packet with parameter 0000
25-0	-	-	Reserved

15 MIIM Command Register 0 (Offset 0068h, R/W)

Bit	R/W	Symbol	Description
31-24	R/W	Divider	Clock Divider to generate MDC signal
23	R/W	No_Pre	Set to 1 indicates send frame without preamble
22	R/W	Write	Uprise indicates send a write command
21	R/W	Read	Uprise indicates send a read command
20	R/W	Scan	Uprise indicates send a scan command
19	R/W	Tx_Mode	Set to 1 indicates turn around time is 2 bits, else 1.5 bits
18-0	-	-	Reserved

16 MIIM Command Register 1 (Offset 006Ch, R/W)

Bit	R/W	Symbol	Description
31-27	R/W	PHY_Addr	PHY Address
26-11	R/W	Ctrl_Data	Control Data
10-6	R/W	Reg_Addr	Register Address
5-0	-	-	Reserved

17 MIIM Status Register (Offset 0070h, R)

Bit	R/W	Symbol	Description
31	R	Busy	Set to 1 indicates MIIM module is busy
30-29	-	-	Reserved
28-13	R	Status	Status of PHY
12-0	-	-	Reserved

18 Power Management Configuration Register (Offset 007Ch, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>31</td><td>R/W</td><td>PMEn</td><td>Power Management Enable: Writable only when the motherboard is detected support aux power.</td></tr>
<tr><td>30</td><td>R/W</td><td>En_LongWF</td><td>Enable Long Wake-up Frame:
Set to 1: The chip supports up to 5 wake-up frames, each with 16-bit CRC algorithm for MS Wakeup Frame.
Set to 0: The chip supports up to 8 wake-up frames, each with 8-bit CRC algorithm for MS Wakeup Frame.</td></tr>
<tr><td>29</td><td>R/W</td><td>En_Magic</td><td>Magic Packet: This bit is valid when the PMEn bit is set. The chip will assert the PMEB signal to wakeup the operating system when the Magic Packet is received.</td></tr>
<tr><td>28</td><td>R/W</td><td>LANWake</td><td>LANWake signal enable/disable:
1: Enable LANWake signal.
0: Disable LANWake signal.</td></tr>
<tr><td>27-26</td><td>R/W</td><td>LOST</td><td>Lwake Output Signal Type: According to the combination of these two bits, there may be 4 choices of LWAKE signal, i.e., active high, active low, positive (high) pulse, and negative (low) pulse. The output pulse width is about 150ms. The default value of each of these two bits is 0, i.e., the default output signal of LWAKE pin is an active high signal.
<table>
<tr><td>LOST</td><td>LWAKE output</td></tr>
<tr><td>00</td><td>Active high</td></tr>
<tr><td>01</td><td>Active low</td></tr>
<tr><td>10</td><td>Positive pulse</td></tr>
<tr><td>11</td><td>Negative pulse</td></tr>
</table></td></tr>
<tr><td>25</td><td>R/W</td><td>LinkUp</td><td>Link Up:
This bit is valid when the PWEn bit is set. The chip, in adequate power state, will assert the PMEB signal to wakeup the operating system when the cable connection is reestablished.</td></tr>
<tr><td>24</td><td>R/W</td><td>WakeUp</td><td>Wakeup Packet: This bit is valid when the PMEn bit is set. The chip will assert the PMEB signal to wakeup the operating system when a valid Wakeup Packet is received.</td></tr>
<tr><td>23-0</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

INTERNAL PHY REGISTER DESCRIPTION

Basic Mode Control Register (Offset 00, R/W)

Bit	R/W	Name	Description/Usage
15	R/W	Reset	This bit sets the status and control registers of the PHY (register 00) in a default state. This bit is self-clearing. 1=software reset; 0=normal operation.
14	-	-	Reserved
13	R/W	Spd_Set	This bit sets the network speed. 1=100Mbps; 0=10Mbps. This bit's initial value comes from 93C46.
12	R/W	Auto negotiation Enable (ANE)	This bit enables/disables the Nway auto-negotiation function. Set to 1 to enable auto-negotiation, bit13 will be ignored. Set to 0 disables auto-negotiation, bit13 and bit8 will determine the link speed and the data transfer mode, respectively. This bit's initial value comes from 93C46.
11-10	-	-	Reserved
9	R/W	Restart Auto Negotiation	This bit allows the Nway auto-negotiation function to be reset. 1=re-start auto-negotiation; 0=normal operation.
8	R/W	Duplex Mode	This bit sets the duplex mode. 0=normal operation; 1=full-duplex. This bit's initial value come from 93C46. If bit12 = 1, read = status write = register value. If bit12 = 0, read = write = register value.
7-0	-	-	Reserved

Basic Mode Status Registers (Offset 01, R)

Bit	R/W	Name	Description/Usage
15	R	100Base-T4	1 = enable 100Base-T4 support; 0 = suppress 100Base- T4 support.
14	R	100Base_TX_FD	1 = enable 100Base-TX full duplex support; 0 = suppress 100Base-tx full duplex support;
13	R	100BASE_TX_HD	1 = enable 100Base-TX half-duplex support; 0 = suppress 100Base-TX half-duplex support;
12	R	10Base_T_FD	1 = enable 10Base_T full duplex support; 0 = suppress 10Base_T full duplex support;
11	R	10BASE_T_HD	1 = enable 10BASE_T half-duplex support; 0 = suppress 10BASE_T half-duplex support;
10-6	-	-	Reserved
5	R	Auto Negotiation Complete	1 = auto-negotiation process completed; 0 = auto-negotiation process not completed.
4	R	Remote Fault	1 = remote fault condition detected (cleared on read); 0 = no remote fault condition detected.

(To be continued)

(Continued)

Bit	R/W	Name	Description/Usage
3	R	Auto Negotiation	1 = link had not been experienced fail state. 0 = link had been experienced fail state.
2	R	Link Status	1 = valid link established; 0 = no valid link established.
1	R	Jabber Detect	1 = jabber condition detected; 0 = no jabber condition detected.
0	R	Extended Capability	1 = extended register capability; 0 = basic register capability only.

Auto-negotiation Advertisement Register (Offset 04, R/W)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during Auto-negotiation.

Bit	R/W	Name	Description/Usage
15	R	NP	Next Page bit. 1 = transmitting the protocol specific data page; 0 = transmitting the primary capability data page.
14	R	ACK	1 = acknowledge reception of link partner capability data word.
13	R/W	RF	1 = advertise remote fault detection capability; 0 = do not advertise remote fault detection capability.
12-10	-	-	Reserved
9	R	T4	1 = 100Base-T4 is supported by local node; 0 = 100Base-T4 not supported by local node.
8	R/W	TXFD	1 = 100Base-TX full duplex is supported by local node; 0 = 100Base-TX full duplex not supported by local node.
7	R/W	TX	1 = 100Base-TX is supported by local node; 0 = 100Base-TX not supported by local node.
6	R/W	10FD	1 = 10Base-T full duplex supported by local node; 0 = 10Base-T full duplex not supported by local node.
5	R/W	10	1 = 10Base-T is supported by local node; 0 = 10Base-T not supported by local node;
4-0	R	Selector	Binary encoded selector supported by this node. Currently only CSMA/CD<00001> is specified. No other protocols are supported.

Auto-Negotiation Link Partner Ability Register (Offset 05, R)

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. The content changes after the successful Auto-negotiation if Next-pages are supported.

Bit	R/W	Name	Description/Usage
15	R	NP	Next Page bit. 1 = transmitting the protocol specific data page; 0 = transmitting the primary capability data page.
14	R	ACK	1 = link partner acknowledge reception of local node's capability data word.
13	R	RF	1 = link partner is indicating a remote fault.
12-10	-	-	Reserved
9	R	T4	1 = 100Base-T4 is supported by link partner; 0 = 100Base-T4 not supported by link partner.
8	R	TXFD	1 = 100Base-TX full duplex is supported by link partner; 0 = 100Base-TX full duplex not supported by link partner.
7	R	TX	1 = 100Base-TX is supported by link partner; 0 = 100Base-TX not supported by link partner.
6	R	10FD	1 = 10Base-T full duplex supported by link partner; 0 = 10Base-T full duplex not supported by link partner.
5	R	10	1 = 10Base-T is supported by link partner; 0 = 10Base-T not supported by link partner;
4-0	R	Selector	Link Partner's binary encoded node selector. Currently only CSMA/CD<00001> is specified.

Auto-negotiation Expansion Register (Offset 06, R)

This register contains additional status for Nway auto-negotiation.

Bit	R/W	Name	Description/Usage
15－4	-	--	Reserved, This bit is always set to 0.
3	R	LP_NP_ABLE	Status indicating if the link partner supports Next Page negotiation. 1 = supported; 0 = not supported.
2	R	NP_ABLE	This bit indicates if the local node is able to send additional Next Pages.
1	R	PAGE _RX	This bit is set when a new Link Code Word Page has been received. The bit is automatically cleared when the auto-negotiation link partner's ability register (register 5) is read by management.
0	R	LP_NW_ABLE	1 = link partner supports NWay auto-negotiation.

Disconnect Counter (Offset 10, R)

Bit	R/W	Name	Description/Usage
15－0	R	DCNT	This 16-bit counter increments by 1 for every disconnect event. It rolls over when becomes full. It is cleared to zero by read command.

False Carrier Sense Counter (Offset 11, R)

This counter provides information required to implement the “FalseCarriers” attribute within the MAU managed object class of Clause 30 of IEEE 802.3u specification.

Bit	R/W	Name	Description/Usage
15－0	R	FCSCNT	This 16-bit counter increments by 1 for each false carrier event. It is cleared to zero by read command.

Nway Test Register (Offset 13, R/W)

Bit	R/W	Name	Description/Usage
15-8	-	--	Reserved
7	R/W	NWLPBK	1 = set Nway to loopback mode.
6-4	-	--	Reserved
3	R/W	ENNWLE	1 = LED0 Pin indicates link pulse
2	R	FLAGABD	1 = Auto-neg experienced ability detect state
1	R	FLAGPDF	1=Auto-neg experienced parallel detection fault state
0	R	FLAGLSC	1 = Auto-neg experienced link status check state

RX_ER Counter (Offset 14, R)

Bit	R/W	Name	Description/Usage
15－0	R	RXERCNT	This 16-bit counter increments by 1 for each valid packet received. It is cleared to zero by read command.

CS Configuration Register (Offset 15, R/W)

Bit	R/W	Name	Description/Usage
15-9	-	-	Reserved
8	R/W	HEART BEAT	1 = HEART BEAT enable, 0 = HEART BEAT disable. HEART BEAT function is only valid in 10Mbps mode.
7	R/W	JBEN	1 = enable jabber function; 0 = disable jabber function.
6	R/W	F_LINK_100	Used to login force good link in 100Mbps for diagnostic purposes. 1 = DISABLE, 0 = ENABLE.
5	R/W	F_Connect	Assertion of this bit forces the disconnect function to be bypassed.
4-3	-	-	Reserved
2	R/W	Con_status_En	Assertion of this bit configures LED1 pin to indicate connection status.
1	-	-	Reserved
0	R/W	PASS_SCR	Bypass Scramble

FUNCTION DESCRIPTION

Ø Transmit operation

The host CPU initiates a transmission by storing an entire packet of data in one of the descriptors in the main memory. When the entire packet has been transferred to the Tx buffer, the SC92031 is instructed to move the data from the Tx buffer to the internal transmit FIFO in PCI bus master mode. When the transmit FIFO contains a complete packet or is filled to the programmed threshold level, the SC92031 begins packet transmission.

Ø Receive Operation

The incoming packet is placed in the SC92031's Rx FIFO. Concurrently, the SC92031 performs address filtering of multicast packets according to its hash algorithms. When the amount of data in the Rx FIFO reaches the level defined in the Receive Configuration Register, the SC92031 requests the PCI bus to begin transferring the data to the Rx buffer in PCI bus master mode.

Ø Auto-negotiation

The Auto-Negotiation function is designed to provide the means to exchange information between the transceiver and the network partner to automatically configure both to take maximum advantage of their abilities, and both are setup accordingly. The Auto-Negotiation exchanges information with the network partner using the Fast Link Pulses (FLPs) - a burst of link pulses. There are 16 bits of signaling information contained in the burst pulses to advertise all remote partner's capabilities which are determined by PHY register 4. According to this information they find out their highest common capability by following the priority sequence as below:

1. 100BASE-TX full duplex
2. 100BASE-TX half duplex
3. 10BASE-T full duplex
4. 10BASE-T half duplex

During power-up or reset, if Auto-Negotiation is found enabled then FLPs will be transmitted and the Auto-Negotiation function will process. Otherwise, the Auto-Negotiation will not occur. When the Auto-Negotiation is disabled, then the Network Speed and Duplex Mode are selected by programming PHY register 0.

Ø Transceiver

The transmitter operation in 100 Mbps mode consists of a MLT-3 encoder, waveform generator and line driver. The MLT-3 encoder converts the NRZI data into a three level MLT-3 code required by IEEE 802.3u. MLT-3 coding uses three levels and converts 1's to transitions between the three levels, and converts 0's to no transitions or changes in level. The purpose of the waveform generator is to shape the transmit output pulse. The waveform generator eliminates the need for any external filters on the TP transmit output. The line driver converts the shaped and smoothed wave-form to a current output that can drive 100 meters of category 5 unshielded twisted pair cable or 150 Ohm shielded twisted pair cable.

The transmitter operation in 10 Mbps mode is much different than the 100 Mbps transmitter. Even so, the transmitter still consists of a waveform generator and line driver.

The receiver either in 10Mbps or 100Mbps mode is mainly a reverse procedure of transmitter

Ø Clock and Data Recovery

The Clock and Data Recovery (CDR) module uses a DPLL to lock onto the incoming data stream and to extracts the recovered clock that will be used to re-time the data stream and set the data boundaries.

Ø Loopback Operation

Loopback mode is normally used to verify that the logic operations up to the Ethernet cable function correctly. In loopback mode for 100Mbps, the SC92031 takes frames from the transmit descriptor and transmits them up to internal Twister logic.

Ø Tx En/decoder

While operating in 100Base-TX mode, the SC92031 performs typically encoding steps of 4B5B encoder, scrambler, parallel-to-serial converter, NRZ-to-NRZI converter and NRZI-to-MLT3. While operating in 10Base-T mode, the SC92031 typically performs parallel-to-serial converter and Manchester process which combines clock and NRZ data such that the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data.

The decoder procedure either in 10Mbps or 100Mbps mode is just a reverse of encoder.

Ø Collision

If the SC92031 is not in the full-duplex mode, a collision event occurs when the receive input is not idle while the SC92031 transmits. If the collision was detected during the preamble transmission, the jam pattern is transmitted after completing the preamble (including the JK symbol pair).

Ø Flow Control

The SC92031 supports IEEE802.3X flow control to improve performance in full-duplex mode. It detects PAUSE packet to achieve flow control task.

1. Control Frame Transmission

When the SC92031 detects that its free receive buffer is less than 3K bytes, it sends a PAUSE packet with pause_time(=FFFFh) to inform the source station to stop transmission for the specified period of time. After the driver has processed the packets in the receive buffer and updated the boundary pointer, the SC92031 sends the other PAUSE packet with pause_time(=0000h) to wake up the source station to restart transmission.

2. Control Frame Reception

The SC92031 enters a back off state for a specified period of time when it receives a valid PAUSE packet with pause_time(=n). If the PAUSE packet is received while the SC92031 is transmitting, the SC92031 starts to back off after current transmission completes. The SC92031 is free to transmit the next packets when it receives a valid PAUSE packet with pause_time(=0000h) or the back off timer(=n*512 bit time) elapses.

EEPROM (93C46) Contents

The 93C46 is a 1K-bit serial EEPROM, it can be organized by 64 words or 128 bytes. Now we list its contents by words showed as below for convenience. After the valid duration of the RSTB pin or auto-load command in the 93C46, the SC92031 performs a series of EEPROM read operations from the 93C46 addresses 00H to 3FH.

Words	Contents	Description
00h 01h	1904 2031	These 4 bytes contain the ID code word for the SC92031
02h	Device ID	These 4 bytes contain the ID code word for the chip. The chip will load the contents of EEPROM into the corresponding location if the ID word is right, otherwise, the chip will not proceed with the EEPROM autoload process.
03h	Vendor ID	
04h	MAXLAT MINGNT	PCI Maximum Latency Timer, PCI configuration space offset 3Fh. PCI Minimum Grant Timer, PCI configuration space offset 3Eh.
05h	INTR PIN INTR LINE	Interrupt Pin Interrupt Line Selection.
06h	Sub ID	PCI Subsystem ID, PCI configuration space offset 2Eh-2Fh.
07h	Sub Vendor ID	PCI Subsystem Vendor ID, PCI configuration space offset 2Ch-2Dh.
08h-0Ah	-	Reserved
0Bh-0Dh	Ethernet Address	Ethernet ID, After auto-load command or hardware reset, the chip loads Ethernet ID to I/O registers.
0Eh-1Fh	-	Reserved
20h-3Fh	VPD DATA	VPD data field. Offset 20h is the start address of the VPD data.

PCI Configuration Space Registers

1 PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	PERRSP	0	0	-	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	FBTBEN	SERREN
		W	-	-	-	-	-		-	SERREN
06h	Status	R	FBBC	0	0	NewCap	0	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	DST1	DST0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08H	Revision ID	R	0	0	0	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R	0	0	0	0	0	0	0	0
0Dh	LTR	R	LTR7	LTR6	LTR5	LTR4	LTR3	LTR2	LTR1	LTR0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTR2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0

(To be continued)

(Continued)

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		R/W	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		R/W	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		R/W	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h	MEMAR	R	0	0	0	0	0	0	0	MEMIN
		W	-	-	-	-	-	-	-	-
15h		R/W	MEM15	MEM14	MEM13	MEM12	MEM11	MEM10	MEM9	MEM8
16h	MEMAR	R/W	MEM23	MEM22	MEM21	MEM20	MEM19	MEM18	MEM17	MEM16
17h		R/W	MEM31	MEM30	MEM29	MEM28	MEM27	MEM26	MEM25	MEM24
18h-2Bh	Reserved									
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		R/W	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap_Ptr	R	0	1	0	1	0	0	0	0
35h-3Bh	Reserved									
3Ch	ILR	R/W	IRL7	IRL6	IRL5	IRL4	IRL3	IRL2	IRL1	IRL0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h-4Fh	Reserved									
50h	PMID	R	0	0	0	0	0	0	0	1
51h	NextPtr	R	0	1	1	0	0	0	0	0
52h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
53h		R	PME_D3_c	PME_D3_h	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2

(To be continued)

(Continued)

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
55h	PMCSR	R	PME_ status	-	-	-	-	-	-	PME_En
		W	PME_ status	-	-	-	-	-	-	PME_En
56h-5Fh	Reserved									
60h	VPDID	R	0	0	0	0	0	0	1	1
61h	NextPtr	R	0	0	0	0	0	0	0	0
62h	Flag VPD Address	R/W	VPDADDR7	VPDADDR6	VPDADDR5	VPDADDR4	VPDADDR3	VPDADDR2	VPDADDR1	VPDADDR0
63h		R/W	Flag	VPDADDR14	VPDADDR13	VPDADDR12	VPDADDR11	VPDADDR10	VPDADDR9	VPDADDR8
64h	VPD Data	R/W	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
65h		R/W	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
66h		R/W	Data23	Data22	Data21	Data20	Data19	Data18	Data17	Data16
67h		R/W	Data31	Data30	Data29	Data28	Data27	Data26	Data25	Data24
68h-FFh	Reserved									

2 PCI Configuration Space functions

The PCI configuration space is intended for configuration, initialization, and catastrophic error handling functions. The functions of the SC92031's configuration space are described below.

VID: Vendor ID. This field will default to a value of SILAN Semiconductor's PCI Vendor ID.

DID: Device ID. This field will default to a value of SILAN Semiconductor's PCI Device ID.

Command: The command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

Bit	Symbol	Description
15-10	-	Reserved
9	FBTBEN	Fast Back-To-Back Enable: When <FBTBEN>=0, read as a zero. write operation has no effect. The SC92031 will not generate Fast Back-to-back cycles. When <FBTBEN>=1, This read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of one means the master is allowed to generate fast back-to-back transaction to different agents. A value of zero means fast back-to-back transactions are only allowed to the same agent. This bit's state after RSTB is zero.
8	SERREN	System Error Enable: When set a one, the SC92031 drive the SERRB line when it detects a parity error on the address phase (AD<31:0> and CBEB<3:0>); A zero disables the SC92031's SERRB output driver.
7	ADSTEP	Address/Data Stepping: Read as zero, write operation has no effect. The SC92031 disable to perform address/data stepping.
6	PERRSP	Parity Error Response: When set to a one, the SC92031 will assert the PERRB pin on the detection of a data parity error when acting as the target, and will sample the PERRB pin as the master. When cleared to a zero, any detected parity error is ignored and the SC92031 continues normal operation. Parity checking is disabled after hardware reset (RSTB).
5	VGASNOOP	VGA palette SNOOP: Read as a zero, write operation has no effect.
4	MWIEN	Memory Write and Invalidate cycle Enable: Read as a zero, write operation has no effect.
3	SCYCEN	Special Cycle Enable: Read as a zero, write operation has no effect. The SC92031 ignores all special cycle operation.
2	BMEN	Bus Master Enable: When set to a one, the SC92031 is capable of acting as a bus master. When cleared to a zero, it is prohibited from acting as a PCI bus master. For the normal operation, this bit must be set by the system BIOS.
1	MEMEN	Memory Space Access: When set to a one, the SC92031 responds to memory space accesses. When cleared to a zero, the SC92031 ignores memory space accesses.
0	IOEN	I/O Space Access: When set to a one, the SC92031 responds to I/O space access. When cleared to a zero, the SC92031 ignores I/O space access.

Status: The status register is a 16-bit register used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

Bit	Symbol	Description
15	DPERR	Detected Parity Error: When set indicates that the SC92031 detected a parity error, even if parity error handling is disabled in command register PERRSP bit.
14	SSERR	Signaled System Error: When set indicates that the SC92031 asserted the system error pin, SERRB. Writing a one clears this bit to zero.
13	RMABT	Received Master Abort: When set indicates that the SC92031 terminated a master transaction with master abort. Writing a one clears this bit to zero.
12	RTABT	Received Target Abort: When set indicates that the SC92031 master transaction was terminated due to a target abort. Writing a one clears this bit to zero.
11	STABT	Signaled Target Abort: Set to a one whenever the SC92031 terminates a transaction with target abort. Writing a one clears this bit to zero.
10-9	DST1-0	Device Select Timing: These bits encode the timing of DEVSELB. They are set to 01b (medium), indicating the SC92031 will assert DEVSELB two clocks after FRAMEB is asserted.
8	DPD	Data Parity error Detected: This bit sets when the following conditions are met: Ø The SC92031 asserts parity error (PERRB pin) or it senses the assertion of PERRB pin by another device. Ø The SC92031 operates as a bus master for the operation that caused the error. Ø The Command register PERRSP bit is set. Writing a one clears this bit to zero.
7	FBBC	Fast Back-To-Back Capable: <FBTBEN>=0, Read as zero, write operation has no effect. <FBTBEN>=1, Read as one.
6	UDF	User Definable Features Supported: Read as zero, write operation has no effect. The SC92031 does not support UDF.
5	66MHz	66 MHz Capable: Read as zero, write operation has no effect. The SC92031 has no 66MHz capability.
4	NewCap	New Capability: <PMEN>=0, Read as zero, write operation has no effect. <PMEN>=1, Read as one.
3-0	-	Reserved

RID: Revision ID Register

The Revision ID register is an 8-bit register that specifies the SC92031 controller revision number.

PIFR: Programming Interface Register

The programming interface register is an 8-bit register that identifies the programming interface of the SC92031 controller. Because the PCI version 2.1 specification does not define any specific value for network devices, PIFR = 00h.

SCR: Sub-Class Register

The Sub-class register is an 8-bit register that identifies the function of the SC92031. SCR = 00h indicates that the SC92031 is an Ethernet controller.

BCR: Base-Class Register

The Base-class register is an 8-bit register that broadly classifies the function of the SC92031. BCR = 02h indicates that the SC92031 is a network controller.

CLS: Cache Line Size

Read will return a zero, write are ignored.

LTR: Latency Timer Register

Specifies, in units of PCI bus clocks, the value of the latency timer of the SC92031.

When the SC92031 asserts FRAMEB, it enables its latency timer to count. If the SC92031 deasserts FRAMEB prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the SC92031 initiates transaction termination as soon as its GNTB is deasserted. Software is able to read or write, and the default value is 00H.

HTR: Header Type Register

Read will return a zero, write are ignored.

BIST: Built-in Self Test

Read will return a zero, write are ignored.

IOAR: This register specifies the BASE I/O address which is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into I/O space.

Bit	Symbol	Description
31-8	IOAR31-8	BASE I/O Address: This is set by software to the Base I/O address for the operational register map.
7-2	IOSIZE	Size Indication: Read back as a zero. This allows the PCI bridge to determine that the SC92031 requires 256 bytes of I/O space.
1	-	Reserved
0	IOIN	IO Space Indicator: Read only. Set to a one by the SC92031 to indicate that it is capable of being mapped into IO space.

MEMAR: This register specifies the base memory address for memory accesses to the SC92031 operational registers. This register must be initialized prior to accessing any SC92031's register with memory access.

Bit	Symbol	Description
31-8	MEM31-8	Base Memory Address: This is set by software to the base address for the operational register map.
7-4	MEMSIZE	Memory Size: These bits return a zero, which indicates that the SC92031 requires 256 bytes of Memory Space.
3	MEMPF	Memory Prefetchable: Read only. Set to a zero by the SC92031.
2-1	MEMLOC	Memory Location Select: Read only. Set to a zero by the SC92031. This indicates that the base register is 32-bit wide and can be placed anywhere in the 32-bit memory space.
0	MEMIN	Memory Space Indicator: Read only. Set to a zero by the SC92031 to indicate that it is capable of being mapped into memory space.

SVID: Subsystem Vendor ID. This field will be set to a value corresponding to PCI Subsystem Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of SILAN Semiconductor's PCI Subsystem Vendor ID.

SMID: Subsystem ID. This field will be set to value corresponding to PCI Subsystem ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 2031h.

BMAR: This register specifies the base memory address for memory accesses to the SC92031 operational registers. This register must be initialized prior to accessing any SC92031 's register with memory access.

Bit	Symbol	Description
31-18	BMAR31-18	Boot ROM Base Address
17-11	ROMSIZE	These bits indicate how many Boot ROM spaces to be supported. The Relationship between <BS2:0> and BMAR17-11 is the following: BS2 BS1 BS0 Description 0 0 0 No Boot ROM, BROMEN=0 (R) 0 0 1 8K Boot ROM, BROMEN (R/W), BMAR12-11 = 0 (R), BMAR17-13 (R/W) 0 1 0 16K Boot ROM, BROMEN (R/W), BMAR13-11 = 0 (R), BMAR17-14 (R/W) 0 1 1 32K Boot ROM, BROMEN (R/W), BMAR14-11 = 0 (R), BMAR17-15 (R/W) 1 0 0 64K Boot ROM, BROMEN (R/W), BMAR15-11 = 0 (R), BMAR17-16 (R/W) 1 0 1 128K Boot ROM, BROMEN(R/W), BMAR16-11=0 (R), BMAR17 (R/W) 1 1 0 unused 1 1 1 unused
10-1	-	Read back a zero
0	BROMEN	Boot ROM Enable: This is used by the PCI BIOS to enable accesses to Boot ROM.

ILR: Interrupt Line Register

The Interrupt Line Register is an 8-bit register used to communicate with the routing of the interrupt. It is written by the POST software to set interrupt line for the SC92031.

IPR: Interrupt Pin Register

The Interrupt Pin register is an 8-bit register indicating the interrupt pin used by the SC92031. The SC92031 uses INTA interrupt pin. Read only. IPR = 01H.

MNGNT: Minimum Grant Timer: Read only

Specifies how long a burst period the SC92031 needs at 33 MHz clock rate in units of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

MXLAT: Maximum Latency Timer: Read only

Specifies how often the SC92031 needs to gain access to the PCI bus in unit of 1/4 microsecond. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

3 The Default Value after Power-on (RSTB asserted)

The Default Value of PCI Configuration

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	0	0	0	-	0	0	0
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-		-	SERREN

(To be continued)

(Continued)

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	Status	R	0	0	0	NewCap	0	0	0	0
07h		R	0	0	0	0	0	0	1	0
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08H	Revision ID	R	0	0	0	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R	0	0	0	0	0	0	0	0
0Dh	LTR	R	0	0	0	0	0	0	0	0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTR2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	1
11h		R/W	0	0	0	0	0	0	0	0
12h		R/W	0	0	0	0	0	0	0	0
13h		R/W	0	0	0	0	0	0	0	0
14h	MEMAR	R	0	0	0	0	0	0	0	0
15h		R/W	0	0	0	0	0	0	0	0
16h		R/W	0	0	0	0	0	0	0	0
17h		R/W	0	0	0	0	0	0	0	0
18h-2Bh	Reserved (All 0)									
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	BROMEN
31h		R	0	0	0	0	0	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	0	0	0	0	0	0	0	0
33h		R/W	0	0	0	0	0	0	0	0

(To be continued)

(Continued)

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34h	Cap_Ptr	R	Ptr7	Ptr6	Ptr5	Ptr4	Ptr3	Ptr2	Ptr1	Ptr0
35h-3Bh	Reserved (All 0)									
3Ch	ILR	R/W	0	0	0	0	0	0	0	0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h-FFh	Reserved (All 0)									

PCI Power Management functions

The SC92031 supports power management mechanism, it complies with the ACPI Specification Rev 1.1, PCI Power Management Rev 1.1, and Device Class Power Management Reference Specification V1.0a, such as to support OS Directed Power Management (OSPM) environment.

These features allow a PCI device to save power when programmed to do so, and to signal the system that the device needs the system to return to a normal operating state to service a wake event. This document details the hardware operation of the family of devices. Software operation (i.e. drivers or operating systems) should comply with this document.

The Power Management Specification presents a low-level hardware interface to PCI devices for the purpose of saving power. The SC92031 supports power states D0, D1, D2, D3hot, and D3cold as defined in the PCI Power Management Specification.

In PCI Power Management mode, three Wake-up events are supported, including Wake-up Frame Received, Magic Packet Received and Link Status Changed.

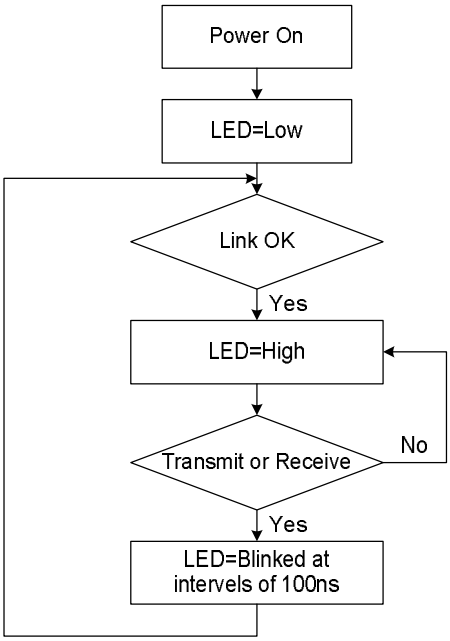
When the PME Enable bit is set to 1, incoming packets are filtered based on settings in the Receive Configuration Register. If the device detects a wake event while in Power Management mode, it will assert the PMEB pin low to signal the system that a wake event has occurred and the device requires service. The system should then bring the device out of Power Management mode.

The chip also supports LAN WAKE-UP function. The LWAKE pin is used to notify the motherboard to execute wake-up process whenever the chip receives a wakeup event, such as Magic Packet.

LED INTERFACE

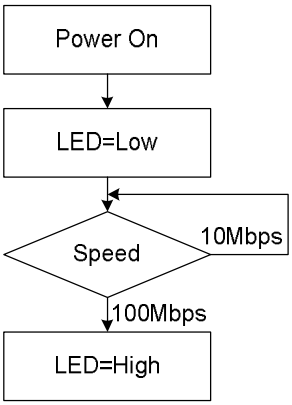
1 LED_ACTIVE

The LED_ACTIVE pin indicates the presence of transmit or receive activity.



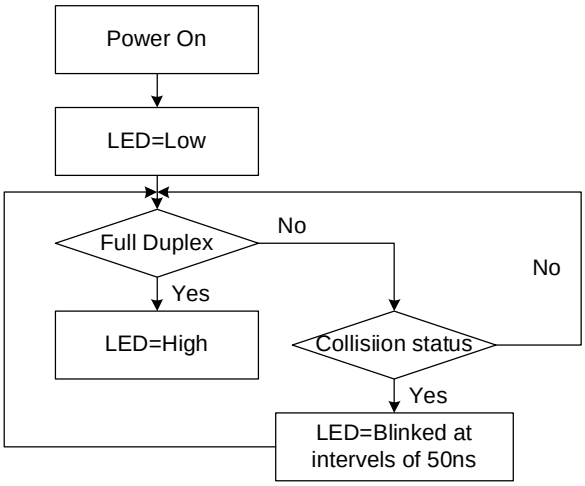
2 LED_SPEED

The LED_SPEED pin indicates a good link at 100 Mb/s data rate.



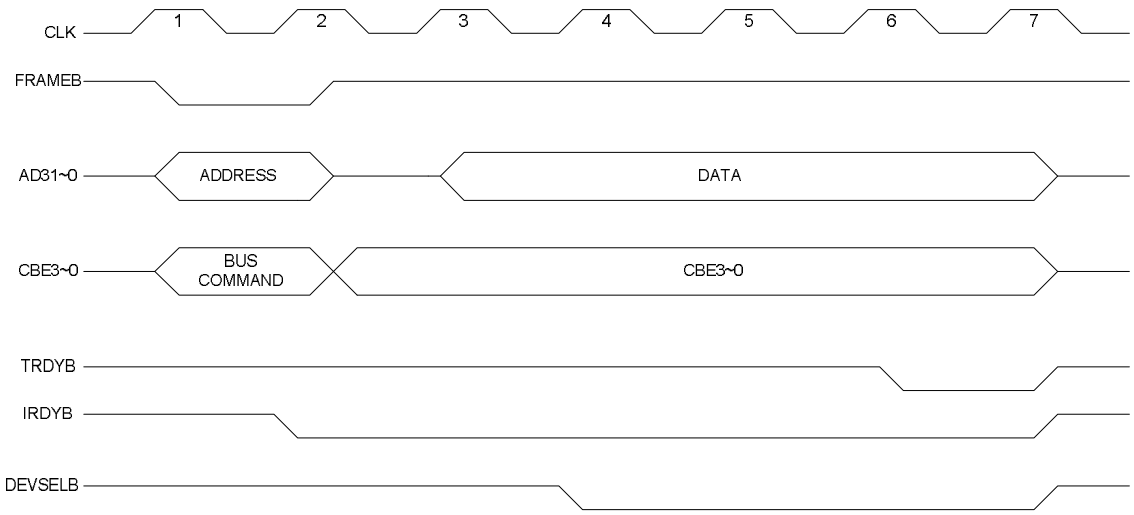
3 LED_DUPLEX_COL

The LED_DUPLEX_COL pin indicates a FULL DUPLEX link or collisions in a HALF DUPLEX link.

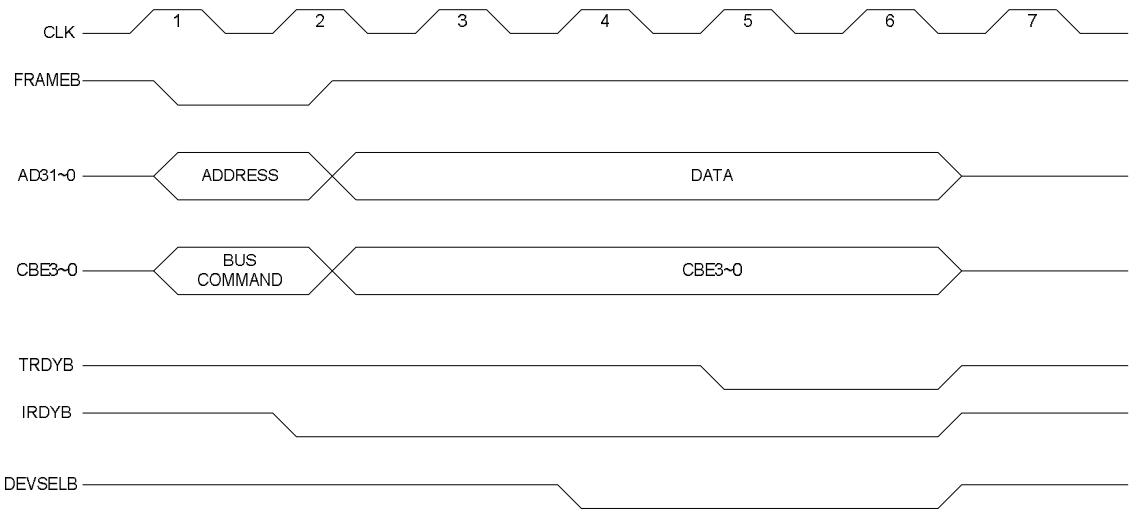


PCI BUS OPERATION TIMING

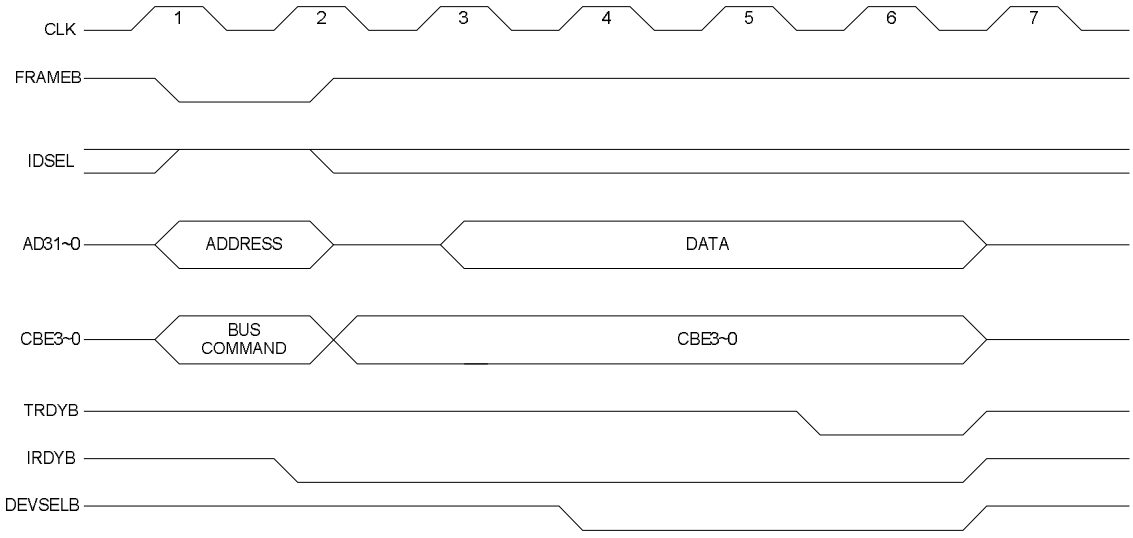
Target Read



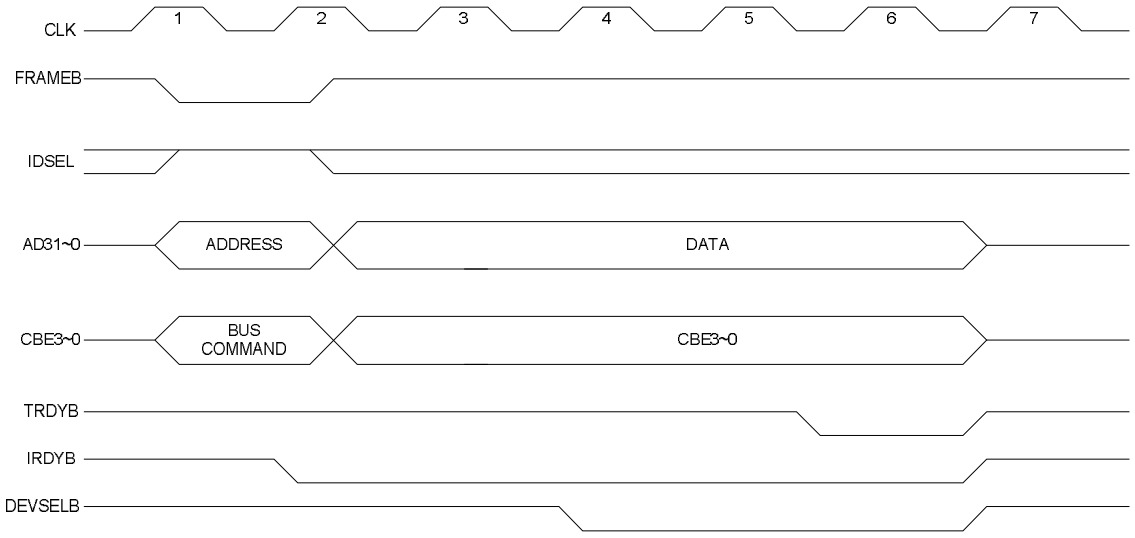
Target Write



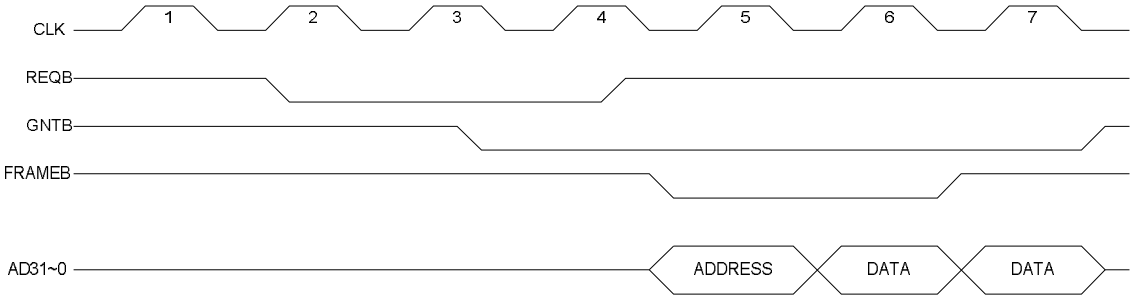
Configuration Read



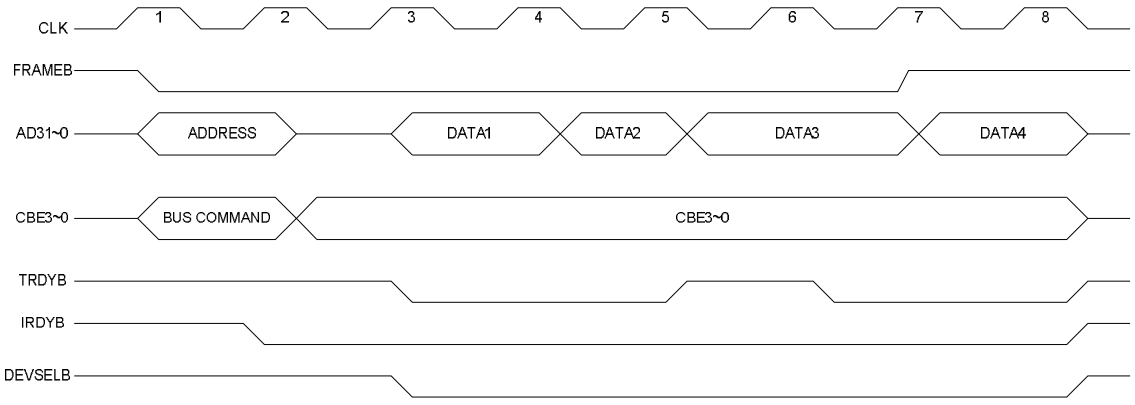
Configuration Write



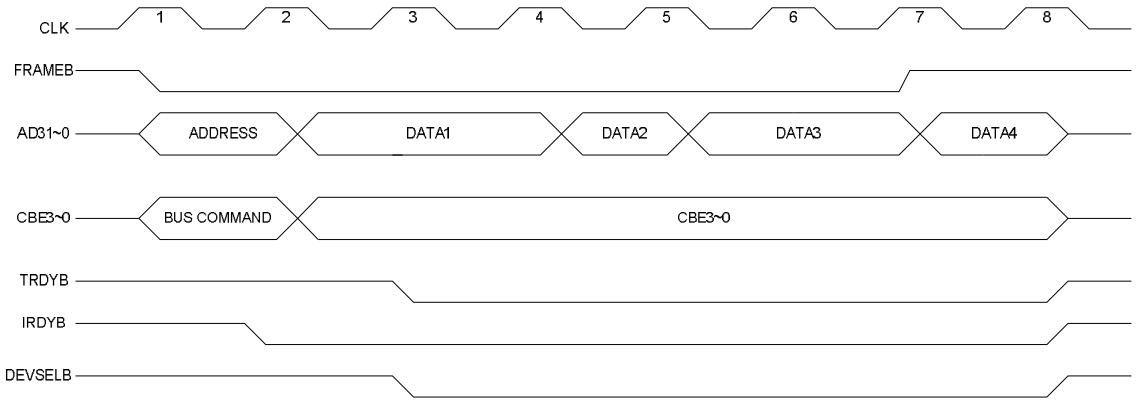
Bus Arbitration



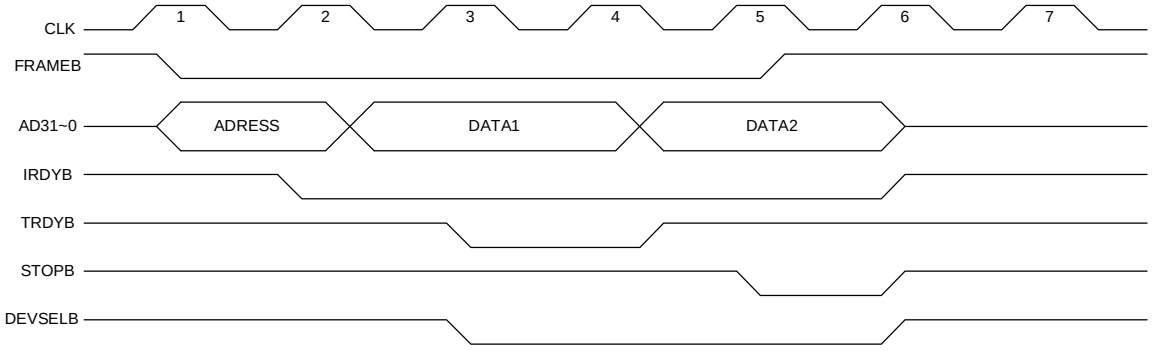
Memory Read



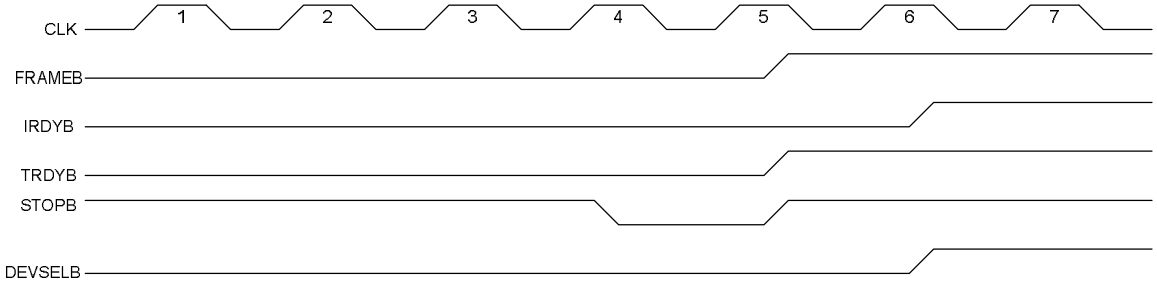
Memory Write



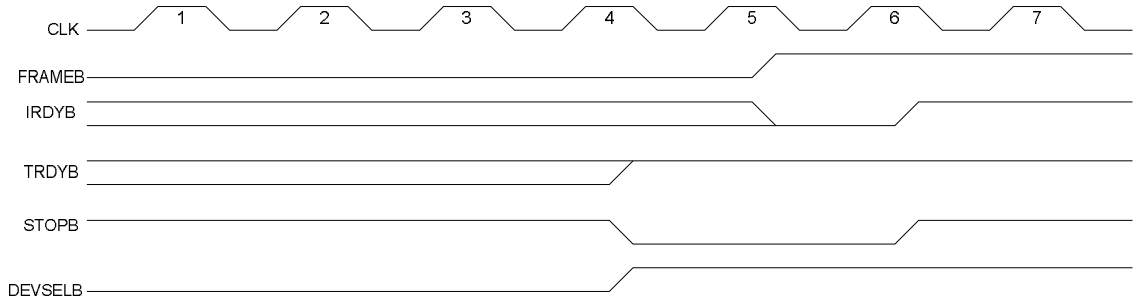
Target Initiated Termination - Retry



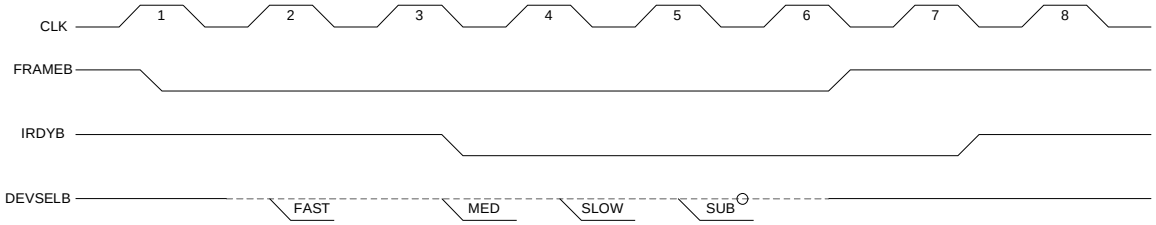
Target Initiated Termination - Disconnect



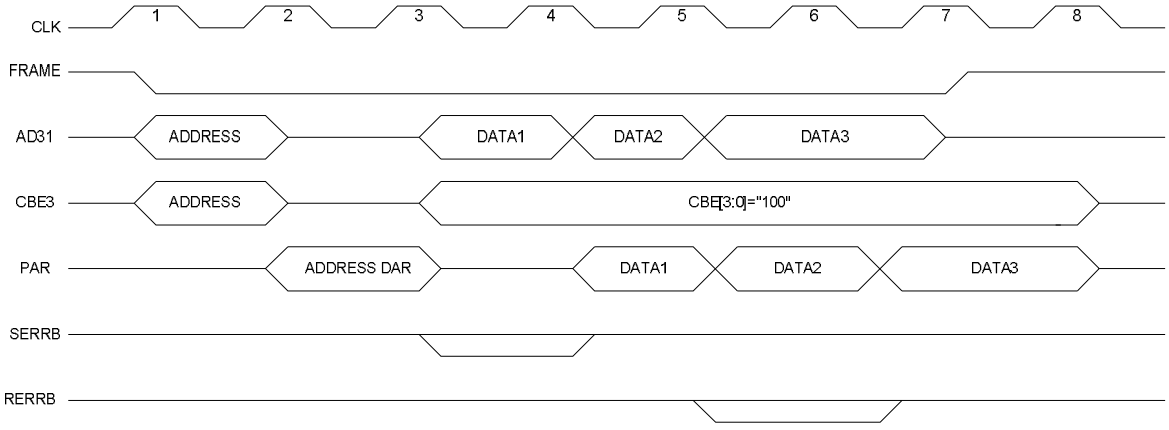
Target Initiated Termination - Abort



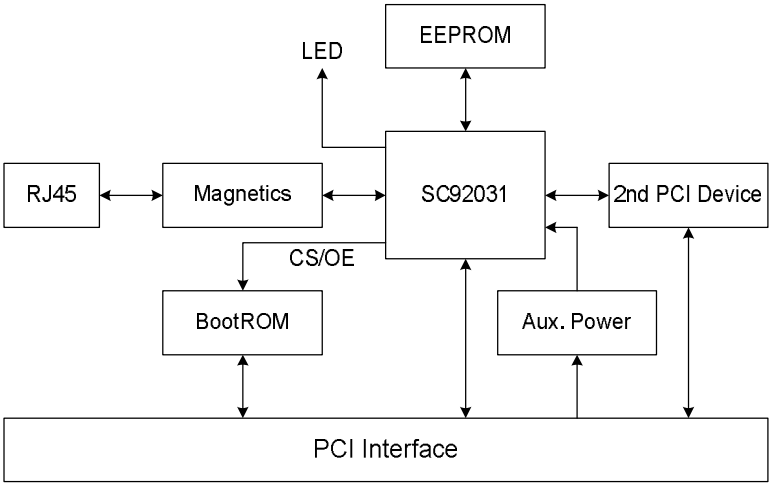
Master Initiated Termination - Abort



Parity Operation - one example

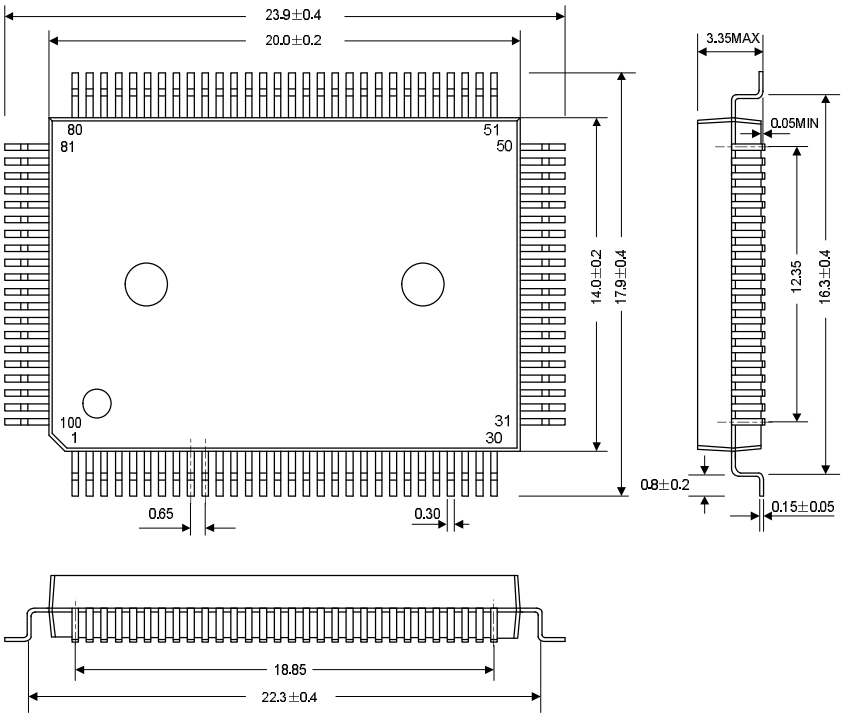


TYPICAL APPLICATION CIRCUIT

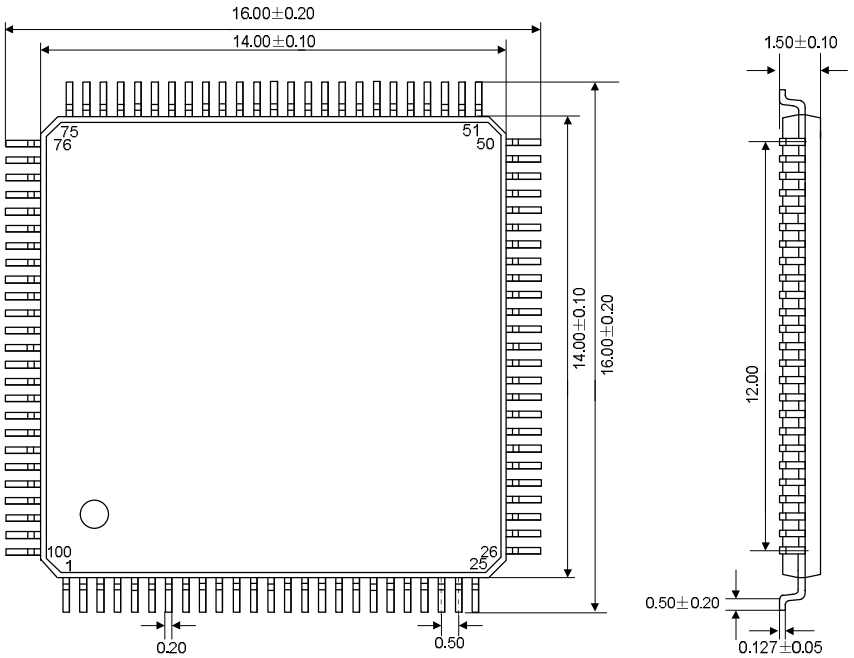


PACKAGE OUTLINE

QFP-100-14×20-0.65 UNIT: mm



LQFP-100-14×14-0.50 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.