15W Wireless Power Transmitter SOC

1 Descriptions

The SC9608 is a highly integrated wireless power transmitter SOC solution that contains both digital microcontroller and analog front end (AFE). The microcontroller includes a high performance 32-bit digital core, rich memory and peripherals. The AFE includes a full-bridge power MOSFETs, current sense amplifier, communication demodulator, linear regulator and protection circuit. The SC9608 supports various type of transmitter include both Extended Power Profile (EPP) and Baseline Power Profile (BPP) defined in WPC V1.2.4.

The SC9608 integrates DP/DM interface. To implement an EPP transmitter system, the SC9608 can request a high voltage from the adapter through CC1/CC2 or DP/DM interface. The SC9608 supports foreign object detection (FOD) by continuously monitoring the input voltage and input DC current. Besides, the SC9608 also supports input under-voltage lockout (UVLO), over-current protection (OCP) and over-temperature protection (OTP). These protections further enhance the reliability of the total wireless power transmitter system.

The SC9608 is available in a compact 4x4 mm FCQFN package.

2 Features

- 4.0V to 14.0V AVIN input voltage range
- 2.0V to 14.0V PVIN input voltage range
- Support up to 15W output power
- Integrated voltage and current demodulation
- Integrated low R_{DSON} power FETs
- Integrated FET driver and bootstrap circuit
- Integrated accurate current sense for FOD
- Support DP/DM fast charging interface
- Support USB Power Delivery
- UVLO/OVP/OCP/OTP
- 4mm x 4mm FCQFN package

3 Applications

- WPC Compliant Wireless Power Transmitter
- Proprietary Wireless Chargers and Transmitter

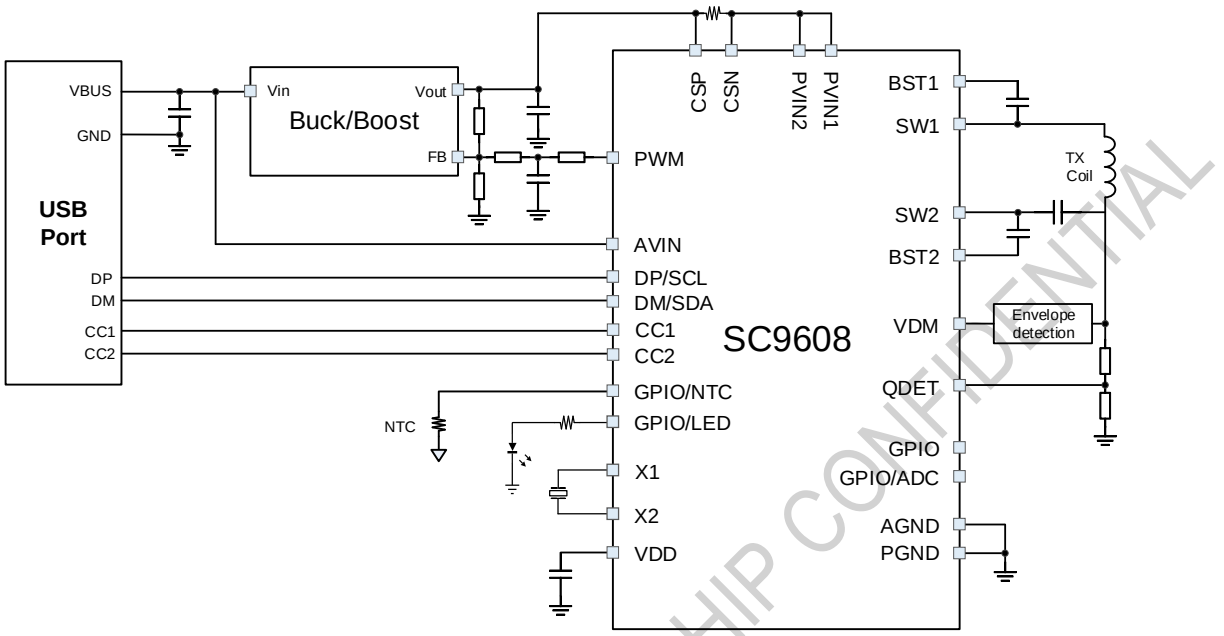
4 Device Information

Part Number	Package	Dimension
SC9608QFER	FCQFN25	4mm x 4mm x0.75mm

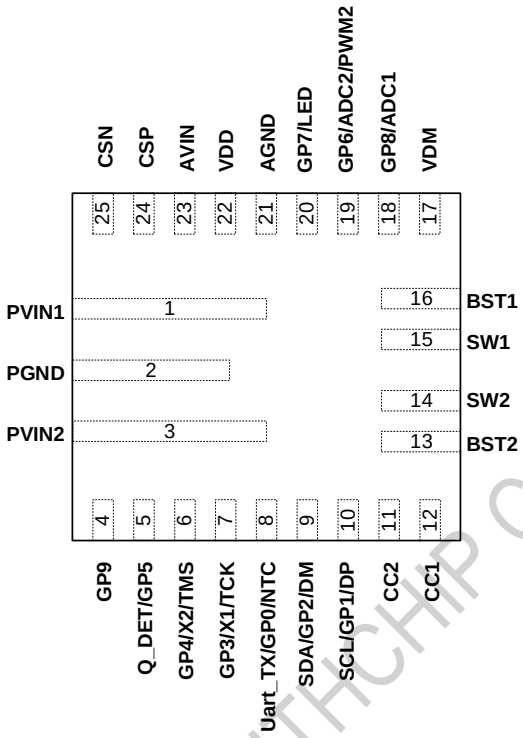
Revision History

Version	Date	Owner	Description
0.0.1	2021/6		initial draft

5 Typical Application Circuit



6 Terminal Configuration and Functions



Pin Map (Top View)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	PVIN1	PWR	Input voltage for half-bridge MOSFET. Bypass with a 22 µF ceramic capacitor to PGND.
2	PGND	PWR	Power ground.
3	PVIN2	PWR	Input voltage for half-bridge MOSFET. Bypass with a 22 µF ceramic capacitor to PGND.
4	GP9	I/O	GPIO
5	Q_DET/GP5	I/O	Quality factor detection input/ GPIO
6	GP4/X2/TMS	I/O	GPIO/ external crystal output/ TMS
7	GP3/X1/TCK	I/O	GPIO/ external crystal input/ TCK
8	UART/GP0/NTC	I/O	UART/GPIO/NTC
9	SDA/GP2/DM	I/O	I2C Serial data line/ GPIO/ DM pin for type A USB port interface
10	SCL/GP1/DP	I/O	I2C Serial clock line/ GPIO/ DP pin for type A USB port interface

11	CC2	I/O	CC2 line of USB Type-C port
12	CC1	I/O	CC1 line of USB Type-C port
13	BST2	I/O	Connect a 0.1 µF capacitor between BST2 and SW2 to bootstrap a voltage to provide the bias for high side MOSFET driver.
14	SW2	PWR	Switch node of the half-bridge MOSFET.
15	SW1	PWR	Switch node of the half-bridge MOSFET.
16	BST1	I/O	Connect a 0.1 µF capacitor between BST1 and SW1 to bootstrap a voltage to provide the bias for high side MOSFET driver.
17	VDM	I	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation
18	GP8/ADC1	I/O	GPIO/ ADC
19	GP6/ADC2/PWM	I/O	GPIO/ ADC/ PWM generator output pin
20	GP7/LED	I/O	GPIO/ LED driver
21	AGND	PWR	Analog Ground
22	VDD	O	Output of internal regulator to provide 5.0V power supply to internal gate drivers and control circuits. Connect a 1 µF ceramic capacitor from VDD to AGND pin.
23	AVIN	PWR	Input voltage for internal LDO converter, Bypass with a 4.7 µF ceramic capacitor to GND
24	CSP	I	Input current sense amplifier positive input
25	CSN	I	Input current sense amplifier negative input

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	PVIN1, PVIN2, SW1, SW2, AVIN, CC1, CC2	-0.3	16	V
	BST1, BST2	-0.3	21	V
	Others	-0.3	5.5	V
Temperature Range	Operating Junction, T_J	-40	125	°C
	Storage temperature range, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage(2)	-2000	2000	V
	Charged device model (CDM) ESD stress voltage (3)	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{PVIN1}, V_{PVIN2}	Input voltage range	2		14	V
V_{AVIN}	Input voltage range for internal LDO convertor	4		14	V
C_{PVIN1}, C_{PVIN2}	PVIN1, PVIN2 Ceramic Capacitor		22		µF
C_{BST1}, C_{BST2}	BST1-SW1, BST2-SW2 Ceramic Capacitor		0.1		µF
C_{AVIN}, C_{VDD}	AVIN, VDD Ceramic Capacitor		2.2		µF
T_A	Operating ambient temperature	0		85	°C
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL RESISTANCE(1)		QFN-23 (4mm x 4mm)	UNIT
Θ_{JA}	Junction to ambient thermal resistance	44	°C/W

Θ_{JC}	Junction to case resistance	11	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.5 Electrical Characteristic

T_J= 25°C, V_{AVIN} =V_{PVIN1} = V_{PVIN2} = 9.0V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{AVIN}	Operating voltage		4		14	V
V_{AVIN_UVLO}	Under voltage lockout threshold	Rising edge	3.65	3.8	3.95	V
		Hysteresis		200		mV
I_Q	Quiescent current into AVIN	Normal mode, no switching		5	10	mA
I_{LP}	Low power current into AVIN	Low power mode			200	μA
VOLTAGE REGULATOR (VDD)						
V_{DD}	VDD output voltage	V_{AVIN} = 9.0V, I_{VDD} =10mA	4.75	5	5.25	V
I_{VDD_LIM}	VDD current limit	V_{DD} = 5.0V		30		mA
V_{DROP}		V_{AVIN} = 4V, I_{VDD} =10mA		200	400	mV
PROTECTION						
V_{AVIN_DPM}	Dynamic power management	DAVDPM_COFG[1:0]=0		4.2		V
		DAVDPM_COFG[1:0]=1		4.4		V
		DAVDPM_COFG[1:0]=2		4.6		V
		DAVDPM_COFG[1:0]=3		4.8		V
V_{DPM_HYS}	AVIN DPM Hysteresis	DAVDPMHYS=0		0.2		V
		DAVDPMHYS=0		0.4		V
V_{AVIN_DROP}	AVIN drop protection	DAVDROP_CFG=0		8.5		V
		DAVDROP_CFG=0		11.5		V
V_{DROP_HYS}	AVIN drop Hysteresis			0.25V		V
V_{AVIN_OV}	AVIN over voltage warning	DAVOV_CFG[1:0]=0		6		V
		DAVOV_CFG[1:0]=1		10		V
		DAVOV_CFG[1:0]=2		13		V
		DAVOV_CFG[1:0]=3		15		V
$V_{AVIN\_OV\_HYS}$	AVIN over voltage warning hysteresis			1		V
V_{PVIN_OV}	PVIN over voltage warning			15		V
$V_{PVIN\_OV\_HYS}$	PVIN over voltage warning hysteresis			1		V
I_{COIL_P}	Coil peak current OCP	DTX_HSOC_SET[2:0]=0		6		A
		DTX_HSOC_SET[2:0]=1		7		A
		DTX_HSOC_SET[2:0]=2		8		A
		DTX_HSOC_SET[2:0]=3		9		A

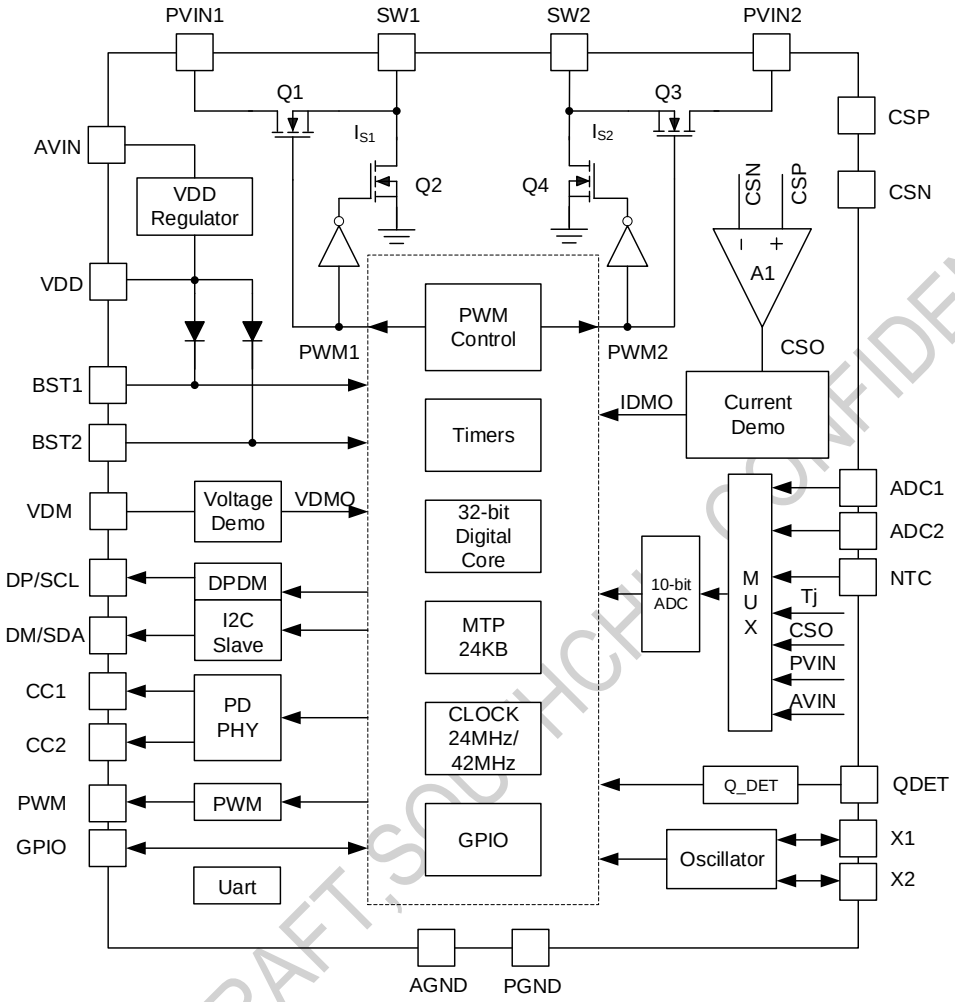
		DTX_HSOC_SET[2:0]=4	10	A
		DTX_HSOC_SET[2:0]=5	11	A
		DTX_HSOC_SET[2:0]=6	12	A
		DTX_HSOC_SET[2:0]=7	13	A
$I_{COIL\_P\_CNT}$	Coil peak current OCP deglitch count	DTX_HSOC_CNTSEL=0	4	
		DTX_HSOC_CNTSEL=0	8	
t_hiccup	hiccup time after OCP		10	ms
POWER SWITCH				
$R_{DS(on)}$	Q1/Q2/Q3/Q4 $R_{DS(on)}$	V_{DD} = 5.0V	22	mΩ
Slew_rate	MOSFET driver slew rate	DCFGSR_DRV[1:0]=0	0.5	V/ns
		DCFGSR_DRV[1:0]=1	0.75	V/ns
		DCFGSR_DRV[1:0]=2	1	V/ns
		DCFGSR_DRV[1:0]=3	1.25	V/ns
T_{DEAD}	dead time	DTX_DEADT[2:0]=0	15	ns
		DTX_DEADT[2:0]=1	25	ns
		DTX_DEADT[2:0]=2	35	ns
		DTX_DEADT[2:0]=3	45	ns
		DTX_DEADT[2:0]=4	55	ns
		DTX_DEADT[2:0]=5	65	ns
		DTX_DEADT[2:0]=6	75	ns
		DTX_DEADT[2:0]=7	85	ns
Voltage Demodulation				
V_{DM_HYS}	VDM input hysteresis voltage	DVDM_HYS[2:0]=0	5	mV
		DVDM_HYS[2:0]=1	10	mV
		DVDM_HYS[2:0]=2	20	mV
		DVDM_HYS[2:0]=3	30	mV
		DVDM_HYS[2:0]=4	40	mV
		DVDM_HYS[2:0]=5	60	mV
		DVDM_HYS[2:0]=6	80	mV
		DVDM_HYS[2:0]=7	100	mV
Current Demodulation				
I_{DM_HYS}	IDM input hysteresis voltage	DIDM_HYS[2:0]=0	5	mV
		DIDM_HYS[2:0]=1	10	mV
		DIDM_HYS[2:0]=2	20	mV
		DIDM_HYS[2:0]=3	30	mV
		DIDM_HYS[2:0]=4	40	mV
		DIDM_HYS[2:0]=5	60	mV
		DIDM_HYS[2:0]=6	80	mV

		DIDM_HYS[2:0]=7		100	mV
Q_DET					
V_{Q_BIAS}	Bias voltage on SW1			2.5	V
$V_{Q\_TH\_HIGH}$	Q detection comparator High TH			200	mV
$V_{Q\_TH\_LOW}$	Q detection comparator Low TH			100	mV
GPIO					
V_{IH}	Input logic high		1.2		V
V_{IL}	Input logic low			0.4	V
V_{OH}	Output logic high	source 5mA	0.9* V_{DD}		V
V_{OL}	Output logic low	sink 5mA		0.1* V_{DD}	V
R_{PU}	Pull up resistor value at GPIO pin			5.5	kΩ
R_{PD}	Pull down resistor value at GPIO pin			5.5	kΩ
I_{LKG_GPIO}	Input leakage current	V_{IN}=5V		1	μA
ADC					
N	Resolution Guarantee 9 bit			10	bit
F_{SAMPLE}				20	kSa/s
Channel	Number of channels			7	
V_{FS}	Full scale voltage			2.048	V
CURRENT SENSE					
I_{IN}	input current range		0	2.5	A
Gain	R_{SENSE}=10mohm	DCSNS_SEL20X=0		0.7	V/A
	R_{SENSE}=20mohm	DCSNS_SEL20X=1		0.7	V/A
	Gain error	I_{SENSE}>0.5A	-2%	2%	
V_{OO}	Sampling output offset voltage	V_{CSP}=V_{CSN}		0.25	V
VOLTAGE SENSE					
$V_{PVINSENSE}$	PVIN sense range		0.5	15.5	V
	sense accuracy	V_{PVIN}>3.5V	-0.5	0.5	%
$V_{AVINSENSE}$	AVIN sense range		3.5	15.5	V
	sense accuracy		-0.5	0.5	%
TDIE SENSOR					
T_{DIE}	TDIE sense range		-40	150	°C
	sense accuracy		-5	5	°C
FPWM					
F_{SW}	PWM switching frequency		105	210	kHz
Duty	PWM duty cycle		0%	100%	
External PWM					

F_{PWM2}	PWM frequency			24		kHz
D_{PWM2}	PWM duty range		0		100	%
	Resolution			0.1		%
DP/DM						
R_{DM_DWN}	DP/DM pull down resistance			20		kΩ
R_{DP_LKG}	DP pin leakage resistance			500		kΩ
V_{DPDM_OVP}	DP/DM OVP threshold		4.6	4.7	4.82	V
CC						
R_{PD_CC}	CC1/2 pull down resistor	$V_{CC1/2}$ = 0V to 2.5V	4.59	5.1	5.61	kΩ
R_{CC_OPEN}	CC1/2 open impedance	CC1/2 in disable status or error status	126			kΩ
V_{CC_OVP}	CC1/2 OVP threshold		5.8	6.1	6.4	V
External Crystal						
F_{XTAL}			24		48	MHz
Start time				2		ms
SDA,SCL						
V_{IH}	Input Threshold High		1.4			V
V_{IL}	Input Threshold Low				0.4	V
I_{LKG}	Input Leakage Current		-1		1	μA
V_{OL}	Sink = 3mA				0.4	V
F_{SCL}					400	kHz
T_{LOW}	Clock low			1.3		μs
T_{HIGH}	Clock high			0.6		μs
C_B	Capacitive Load for SCL and SDA			150		pF
C_I	SCL, SDA Input Capacitance			5		pF
CLOCK						
F_{SYSTEM}	System OSC frequency			24		MHz
	System OSC frequency error		-3%		3%	
F_{PWM}	Full bridge PWM clock			42		MHz
	Full bridge PWM clock error		-2%		2%	
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			150		°C
T_{SD_HYS}	Thermal shutdown hysteresis			20		°C
T_{WN}	Thermal warning temperature	DTSW_CFG[2:0]=0		65		°C
		DTSW_CFG[2:0]=1		75		°C
		DTSW_CFG[2:0]=2		85		°C
		DTSW_CFG[2:0]=3		95		°C

		DTSW_CFG[2:0]=4	105	°C
		DTSW_CFG[2:0]=5	115	°C
		DTSW_CFG[2:0]=6	125	°C
		DTSW_CFG[2:0]=7	135	°C
T_{WN_HYS}	Thermal warning hysteresis		10	°C

8 Functional Block Diagram



9 Detailed Description

The SC9608 device is a highly integrated wireless power transmitter SOC solution supporting up to 15W power output.

9.1 Power Supply

The SC9608 integrates a high-voltage low-dropout (LDO) voltage regulator powered from AVIN. It feeds the internal power drivers and control circuits. The VDD pin supplies a regulated 5.0V voltage supply. Decouple this pin to power ground with a 2.2μF low ESR ceramic capacitor placed close to the IC.

The internal LDO works once AVIN is above the UVLO threshold. The load capability of VDD regulator is about 30mA. Please do not power up other load from the internal LDO.

9.2 Under-Voltage Lockout (UVLO)

The UVLO function protects the chip from operating at insufficient power supply. The chip disables all the function if AVIN voltage is lower than 3.6V (typical) and it does not start up again until input voltage is higher than 3.8V (typical).

9.3 Current Sense

To support foreign object detection (FOD), the SC9608 integrates a lossless current sense amplifier to senses the average input current. User should always monitor the voltage of ADC channel 5 to calculate the input current. Gain of the input current to the sampling output voltage is 0.7V/A.

When the input current is zero, the sampling output has an offset voltage. The offset voltage is about 0.25V.

The offset may have some variation. For accurate measurement of the input current, MCU need to calibrate the offset before power stage switching.

9.4 Full-Bridge invertor

The SC9608 integrates a high efficiency full-bridge invertor with ultra-low R_{DS} to convert the DC power signal to AC power. The drive ability of FET is adjustable bring more convenience for EMI test.

The SC9608 also integrates a PWM peripheral to control the full-bridge invertor. The PWM1 controls the internal MOSFET Q1 and Q2, and PWM2 controls the internal MOSFET Q3 and Q4 as shown in the Block Diagram. The invertor also can work in half-bridge mode by disenable PWM1 or PWM2.

There are four configuration registers for customer to configure: PWM_PERIOD [15:0], PWM_DUTY [15:0], PWM_DEADTIME [15:0] and PWM_PHASE [15:0]. For a target switching frequency F_{SW} (Hz), the PWM_PERIOD [15:0] register should be configured to PWM_CLOCK/F_{SW}. The internal 24MHz oscillator and 42MHz oscillator are alternative for PWM CLOCK. PWM_DUTY [15:0] register should always be programmed to half of the PWM_PERIOD [15:0] register.

PWM_DEADTIME [15:0] register is used for the duty cycle control of full-bridge. The formula is as follows:

Duty=50%- PWM_DEADTIME [15:0]/PWM_PERIOD [15:0]

PWM_PHASE [15:0] register is used for phase shift mode.

Phase=(PWM_PHASE [15:0]/PWM_PERIOD [15:0])*360°

For duty cycle control mode, to set 50% duty cycle, the PWM_DEADTIME [15:0] should be configure to 0. To set 10% duty cycle, the PWM_DEADTIME [15:0] should be configure to 0.4* PWM_PERIOD [15:0]. The generation theory of PWM1/2 is as below figure 1.

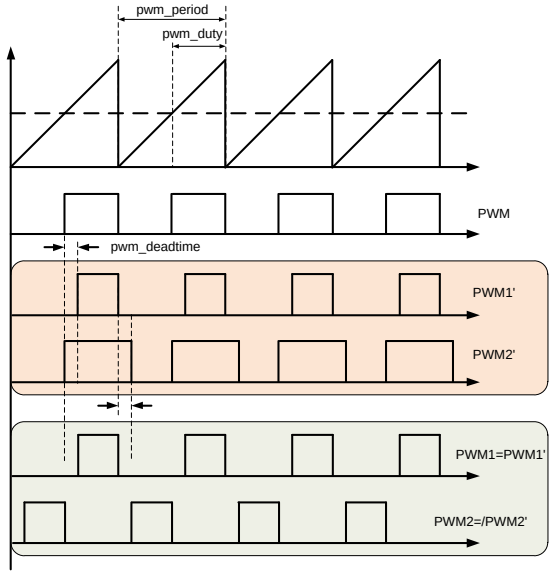


Fig1. Duty cycle control mode

For phase shift control mode, to set 30° phase shift, the PWM_PHASE [15:0] should be configure to PWM_PHASE [15:0]/12. The phase shift control method is as below figure 2.

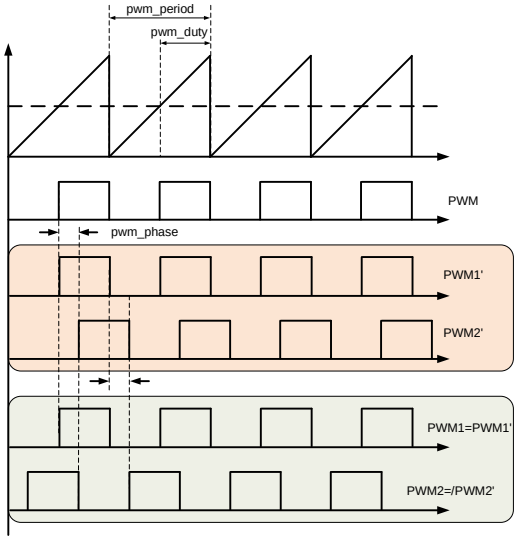


Fig2. Phase shift control mode

9.5 ASK Demodulation

To increase the communication reliability in any load condition, the SC9608 has integrated two demodulation schemes, one based on input average current information and the other based on coil voltage information. The ASK voltage envelope detector is implemented using a discrete solution as depicted on figure 3. This simple implementation achieves the envelope detector function low-pass filter as well as the DC filter function.

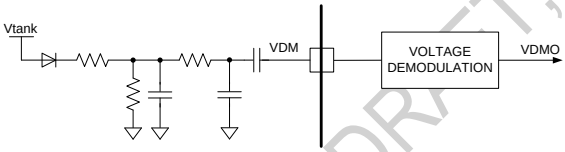


Fig3. Voltage Demodulation

The current demodulation module takes the modulation information from the internal CSO output signal indicated the average input current. The MCU can detect the demodulation results on internal VDMO and IDMO signals and then implement the packet decode. The MCU can select either voltage-mode or current-mode signals depending upon which produces the best demodulated signal.

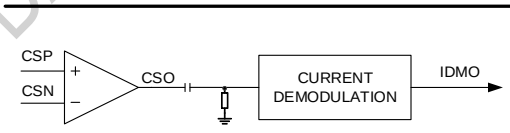


Fig4. Current Demodulation

The comparator hysteresis of voltage-mode and current-mode demodulation circuits are both adjustable to achieve better system communication performance.

9.6 ADC

The SC9608 integrates a 10-bit SAR ADC to sense the external and internal voltages. The full-scale of ADC reference voltage is 2.048V, which means 2mV/LSB.

Table1. ADC channels

Channel	Signal	Description
CH1	ADC1	External voltage sense
CH2	ADC2	External voltage sense
CH3	NTC	External voltage sense
CH4	TDIE	Die temperature sense
CH5	CSO voltage	CSO voltage sense
CH6	PVIN voltage	PVIN voltage sense
CH7	AVIN voltage	AVIN voltage sense

9.7 Q Factor Detection

The SC9608 integrates an accurate Q factor detection circuit to implement foreign objects detection before the selection phase. The formula is as follows:

$Q=\Delta T*\pi/10/\ln 2$

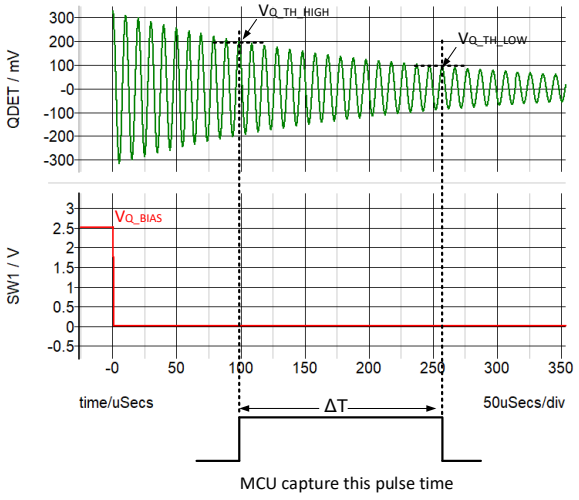


Fig5. Operation principle of Q factor detection

9.8 External PWM generator

The SC9608 integrates an external PWM generator used to adjust the DC-DC convertor output voltage. The fixed frequency of PWM is 24 kHz, and PWM duty is programmable from 0% to 100%. The adjustment resolution of PWM duty is about 0.1%.

9.9 External crystal oscillator

The SC9608 integrates a crystal driver for high precision and steady clock. This module provides more accuracy reference clock for full bridge PWM driver control. The range of crystal should be 24MHz to 48MHz.

9.10 DPDM Interface

The SC9608 integrates DPDM interface with different kind of fast charge protocols supported. The DPDM interface is available for Micro-B and Type-C port applications. It supports the mainstream fast charging protocols, such as BC1.2, DCP, HVDCP, FC, AFC and FCP etc.

9.11 CC1/2 Interface

The SC9608 integrates CC1/2 interface meeting the Type-C protocol and providing USB PD physical layer for PD protocol communication. User can easily implement the Type-C sink protocol and PD protocol through the packaged software interface.

9.12 Over-Current Protection (OCP)

The SC9608 integrates an over-current protection function which monitoring the peak current through the full-bridge and coil cycle by cycle. The device senses the current of the high-side FET and compare to the current-limit threshold during every switching cycle. When the sensed current reaches the current-limit threshold, the over-current fault counter is incremented. If the over-current fault counter reaches the setting value (DTX_HSOC_CNTSEL), all the full-bridge FETs are turned off regardless of the PWM inputs. The IC remains in hiccup mode for a period equal to 10ms typically and then attempts to restart. Once the OCP condition removed, SC9608 exits hiccup mode and goes back to normal operation. The over current point is programmable by register (DTX_HSOC_SET).

9.13 Over-Voltage Protection (OVP)

Both the AVIN and PVIN pins implement the over-voltage protection function. When an OVP fault triggered, generate the interrupt signal to inform MCU the OVP condition for the further processing. The AVIN over-voltage protection is adjustable for 6V to 15V by register DAVOV_CFG [1:0]. The PVIN over voltage is about 15V with 1V hysteresis.

9.14 Over Temperature Protection (OTP)

The SC9608 over temperature protection includes OT warning and OT shutdown. When the die temperature rises over the thermal warning temperature, an alert signal will indicate the OT status. The OT warning point is programmable by register DTSW_CFG [2:0].

When the silicon die temperature exceeds 150℃, the SC9608 shuts down and it does not recover until the die temperature drop below 130℃.

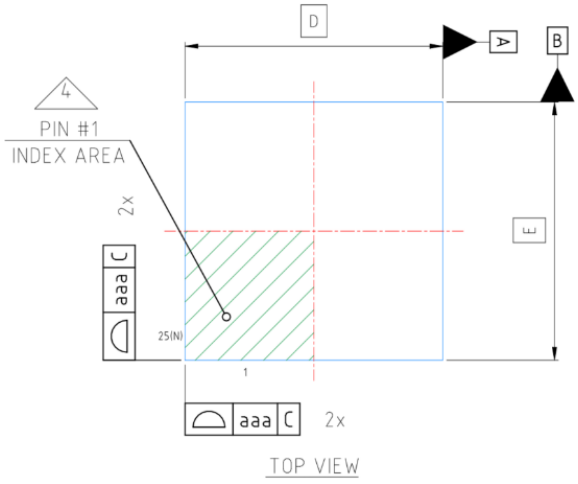
10 Register Maps

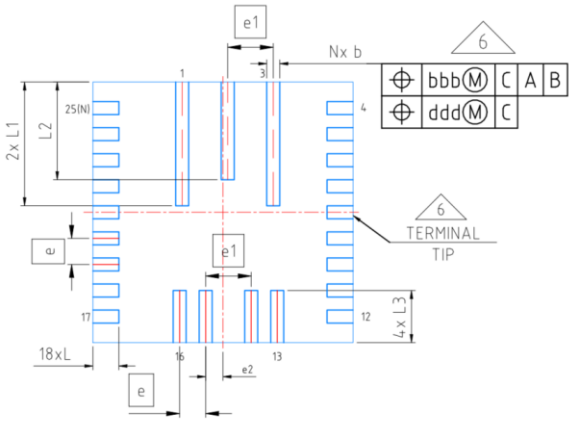
MODULE	REGISTER NAME	ADDRESS	REGISTER DESCRIPTION
TIMER0	T0CTRL		Timer0 control register
	T0CNT		Timer0 count register
	T0CCR0		Timer0 compare register
TIMER1	T1CTRL		Timer1 control register
	T1CNT		Timer1 count register
	T1CCR0		Timer1 compare register 0
	T1CCR1		Timer1 compare register 1
TIMER2	T2CTRL		Timer2 control register
	T2CNT		Timer2 count register
	T2CCR0		Timer2 compare register 0
	T2CCR1		Timer2 compare register 1
PWMA	PWMA_CTRL		PWM control register
	PWMA_CNT		PWM count register
	PWMA_PERIOD		PWM period register
	PWMA_DUTY		PWM duty register
	PWMA_DEADTIME		PWM dead time register
	PWMA_PHASE		PWM phase register
GPIO	GPIOIN		GPIO input status register
	GPIOOUT		GPIO output status register
	GPIODIR		GPIO direction register
	GPIOAEN		GPIO analog function enable register
	GPIORPU		GPIO pull-up enable register
	GPIORPD		GPIO pull-down enable register
	GPIOIE		GPIO interrupt enable register
	GPIOIF		GPIO interrupt flag register
	GPIOM0		GPIO interrupt mode configure register
	GPIOM1		GPIO interrupt mode configure register
	IO_MUX		GPIO output MUX register
WDT	WDT_CNT		Watch dog count register
	WDT_CTRL		Watch dog control register
	WDT_LOCK		Watch dog lock register
	WDT_INIT		Watch dog count value register
UART	UART_SBUF		UART buffer register
	UART_CTRL		UART control register
ADC	ADC_CTRL		ADC control register
	CH1_DATA		ADC channel 1 result register
	CH2_DATA		ADC channel 2 result register
	CH3_DATA		ADC channel 3 result register

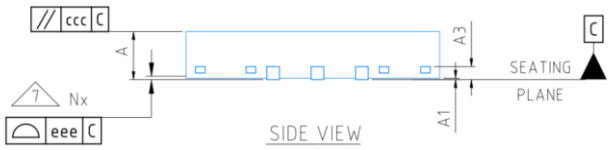
	CH4_DATA		ADC channel 4 result register
	CH5_DATA		ADC channel 5 result register
	CH6_DATA		ADC channel 5 result register
	CH7_DATA		ADC channel 5 result register
IIC_SLAVE	DATA0		IIC DATA register
	DATA1		IIC DATA register
	DATA2		IIC DATA register
	DATA3		IIC DATA register
	IIC_S_IE		Write IIC DATA interrupt register
	IIC_S_IF		Write IIC DATA flag register
	IIC_S_REG_ADDR		IIC operating register address
	IIC_S__REG_ADDR		IIC slave device address
	IIC_S_CTRL		IIC slave control address
PMU	PMU_CTRL		MCU configuration register
	WAKEUP_EN		MCU sleep mode wakeup register
	CLK_CTRL		Block clock enable register
	DUMMY_REG		Dummy register
	CHIP_ID		Chip ID register
ANA_IF	ANA_CTRL		
	ANA_OSC		
	ANA_QDET		
	ANA_ISENSE		
	ANA_BRIDGE		
	ANA_PROTECTION		

11 MECHANICAL DATA

FCQFN25L (4x4x0.75)







Dimension Table

Thickness / Symbol	W			V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM	
A	0.70	0.75	0.80	0.80	0.90	1.00	
A1	0.00	0.02	0.05	0.00	0.02	0.05	
A3	---	0.203 Ref.	---	---	0.203 Ref.	---	
b	0.15	0.20	0.25	0.15	0.20	0.25	6
D		4.00 BSC			4.00 BSC		
E		4.00 BSC			4.00 BSC		
e		0.40 BSC			0.40 BSC		
e1		0.70 BSC			0.70 BSC		
e2		0.27 BSC			0.27 BSC		
L	0.30	0.40	0.50	0.30	0.40	0.50	
L1	1.80	1.90	2.00	1.80	1.90	2.00	
L2	1.40	1.50	1.60	1.40	1.50	1.60	
L3	0.70	0.80	0.90	0.70	0.80	0.90	
aaa		0.05			0.05		
bbb		0.10			0.10		
ccc		0.10			0.10		
ddd		0.05			0.05		
eee		0.08			0.08		
N		25					3
ND		3/4					5
NE		9					5
NOTES		1, 2					
LF PART NO.		446251					