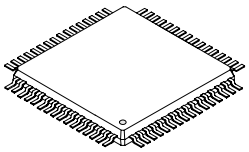
CAR-CD DIGITAL SERVO SIGNAL PROCESSOR(SLAVE MODE)

DESCRIPTION

The SC9642 is a single-chip CD processor for digital servo and ASIC circuit. This LSI incorporates CD servo controller, CD signal processor, digital audio DAC and built-in CPU interface.



LQFP-64-10x10-0.5

FEATURES

* Supports 1X to 2X speed playback
* Command and sub code transmission adopts tri-line communication or parallel communication.
* Built-in MCU controls the CD and state feedback by communication instructions of the communication bus.
* Supports format of CD-A/V, CD-R, CD-R/W and CD-ROM

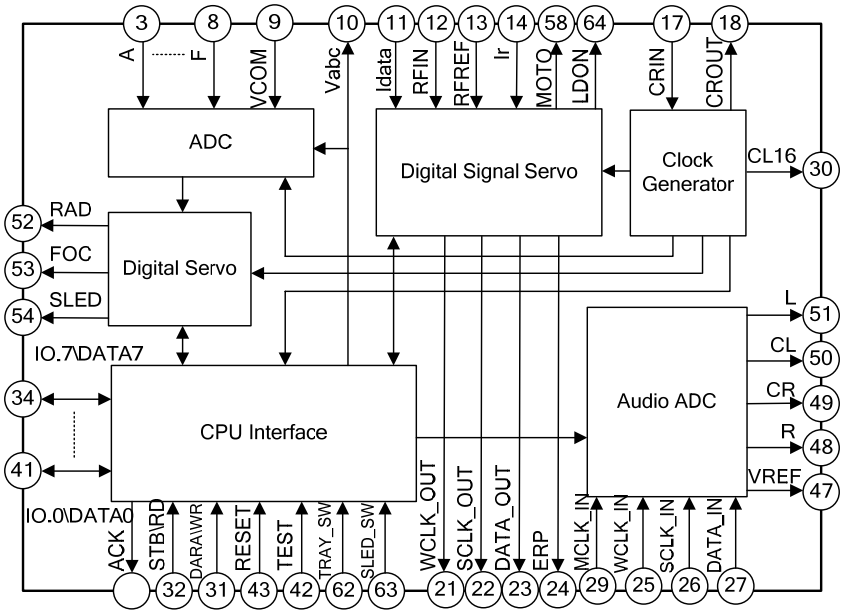
APPLICATIONS

* CD, VCD and MP3 player
* Desk audio system

ORDERING INFORMATION

Device	Package
SC9642	LQFP-64-10X10-0.5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Tamb=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.5 ~ +5.5	V
Input Voltage On Pins	V_{IN}	-0.5 ~ V_{DD} + 0.5	V
Operating Temperature	Tmax	-40 ~ +85	°C

ELECTRICAL CHARACTERISTICS(V_{DD}=3.4~5.5V;V_{SS}=0V;Tamb=-10~+60°C)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current	I_{DD}	5V; 1X Speed	—	45	—	mA
RFIN Input Signal	V_{RFIN}		—	1.0	—	V
Reference Voltage	V_{Ir}		—	0.5V_{DD}	—	V
Common Mode DC	V_{VCOM}		2.0	2.5	—	V
Output ADC Reference Voltage	V_{Vadc}		V_{VCOM}+ 0.462	—	V_{VCOM}+ 2.313	V
Input Current Of Central Diode B	I_B		0	—	10	μA
Input Current Of Central Diode A	I_A		0	—	10	μA
Input Current Of Central Diode C	I_C		0	—	10	μA
Input Current Of Central Diode D	I_D		0	—	10	μA
Input Current Of Satellite Diode F	I_F		0	—	5	μA
Input Current Of Satellite Diode F	I_E		0	—	5	μA
Data Slicer Feed-back Current Output	Iidata		1.9	—	5.5	μA
LDON Low Level Output Current	I_{LDON}		0	—	2	mA
ERR Output Current	I_{ERR}		0	1	—	mA
DATA_OUT WCLK_OUT SCLK_OUT Output Current	I_{OH1} I_{OL1}		0	1	—	mA
DATA_OUT WCLK_OUT SCLK_OUT Low Level Output Voltage	V_{OL1}	IOL1=1mA	0	—	0.4	V
DATA_OUT WCLK_OUT SCLK_OUT High Level Output Voltage	V_{OH1}	IOH1=-1mA	V_{DD}-0.4	—	V_{DD}	V
RAD Output Current	I_{RAD}		0	1	—	mA
FOC Output Current	I_{FOC}		0	1	—	mA
SLED Output Current	I_{SLED}		0	1	—	mA

(To be continued)

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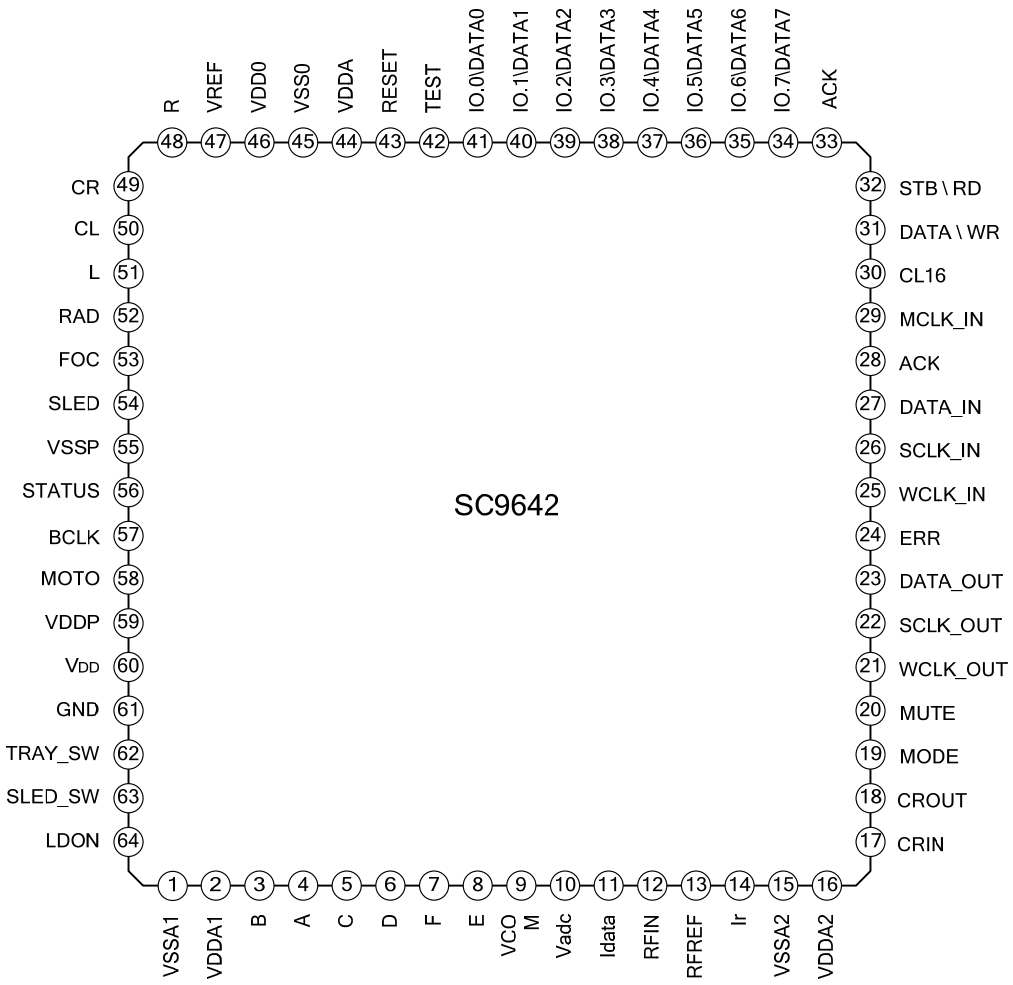
Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
MOTO Output Current	IMOTO		0	10	—	mA
RAD, FOC, SLED Low Level Output Voltage	VOL	IOL=1mA	0	—	0.4	V
RAD, FOC, SLED High Level Output Voltage	VOH	IOH=-1mA	VDD-0.4	—	VDD	V
Moto Low Level Output Voltage	VOLmoto	IOLmoto=10mA	0	—	1.0	V
Moto high Level Output Voltage	VOHmoto	IOHmoto=-10mA	VDD-1	—	VDD	V
RAD, FOC, SLED, MOTO Output 3-state Leakage Current	IZO		-10	0	+10	μA
ACK, WR, RD, DATA0～7, High Level Input Voltage	VILH		2.8	3.0	-	V
ACK, WR, RD, DATA0～7, Low Level Input Voltage	VIHL		0.6	—	0.7	V
DATA_IN, WCLK_IN, SCLK_IN, High Level Input Voltage	VOHda		0.7VDD	—	VDD+0.5	V
DATA_IN, WCLK_IN, SCLK_IN, Low Level Input Voltage	VOLda		-0.5	—	0.3VDD	V
DAC Total Harmonic Distortion Plus Noise	(THD+N)/S		60	65	70	dB
DA Filter Attenuation	Filter_DA	0~19 kHz	-	-	0.001	dB
		19~20 kHz	-	-	0.03	dB
		24KHz	25	-	-	dB
		25 ~ 35 KHz	40	-	-	dB
		35 ~ 64 KHz	50	-	-	dB
		64 ~68 KHz	31	-	-	dB
		68KHz	35	-	-	dB
		69~ 88KHz	40	-	-	dB
Crystal Frequency	Fsystem		—	16.9344	—	MHz
SCLK Frequency	FSCLK_IN		—	2.8224	—	MHz
WCLK Frequency	FWCLK_IN		—	44.1	—	KHz

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin name	Descriptions
1	VSSA1	Analog Ground 1
2	VDDA1	Analog Supply 1
3	B	Central diode current signal input
4	A	Central diode current signal input
5	C	Central diode current signal input
6	D	Central diode current signal input
7	F	Satellite diode current signal input
8	E	Satellite diode current signal input
9	VCOM	DC voltage input
10	Vadc	ADC reference voltage output
11	Idata	Data signal feed-back current output

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Pin No.	Pin name	Descriptions
12	RFIN	EFM signal input
13	RFREF	Comparator common mode input
14	Ir	Reference current output
15	VSSA2	Analog ground 2
16	VDDA2	Analog supply 2
17	CRIN	Crystal oscillation circuit input. When the master clock is input externally, input it from this pin.
18	CROUT	Crystal oscillation circuit output.
19	MODE	Connect ground.
20	MOT_CTRL	Control the spindle motor (during focusing and jumping, if MOT_CTRL output high level signal, it can control the MOT control port of SA9529 after through 3 voltage drop diodes, then prevent the spindle reverse; in other condition, the MOT-CTRL output low level).
21	WCLK_OUT	D/A interface. LR clock output.
22	SCLK_OUT	D/A interface. Bit clock output.
23	DATA_OUT	D/A interface. Serial data output
24	ERR	C2 error flag
25	WCLK_IN	D/A interface. LR clock input.
26	SCLK_IN	D/A interface. Bit clock input.
27	DATA_IN	D/A interface. Serial data input
28	ACK	Acknowledge Signal output pin (drain open, with pull up resistor).
29	MCLK_IN	DAC system clock input (16.9344MHz)
30	CL16	16.9344MHZ clock output
31	DATA \ WR	Data I/O port, it is shared with write port of parallel communication.
32	STB \ RD	Control I/O port, it is shared with read port of parallel communication.(drain open, with internal pull-up resistor).
33	ACK	Acknowledge signal port (drain open, with internal pull-up resistor).
34	IO.7 \ DATA7	General I/O port, it is shared with data bit 7 (drain open, with internal pull up resistor).
35	IO.6 \ DATA6	General I/O port, it is shared with data bit 6 (drain open, with internal pull up resistor).
36	IO.5 \ DATA5	General I/O port, it is shared with data bit 5 (drain open, with internal pull up resistor).
37	IO.4 \ DATA4	General I/O port, it is shared with data bit 4 (drain open, with internal pull up resistor).
38	IO.3 \ DATA3	General I/O port, it is shared with data bit 3 (drain open, with internal pull up resistor).
39	IO.2 \ DATA2	General I/O port, it is shared with data bit 2 (drain open, with internal pull up resistor).
40	IO.1 \ DATA1	General I/O port, it is shared with data bit 1 (drain open, with internal pull up resistor).
41	IO.0 \ DATA0	General I/O port, it is shared with data bit 0 (drain open, with internal pull up resistor).
42	TEST	Test pin.
43	RESET	Reset pin (active low)
44	VDDA	Analog Supply
45	VSSO	Analog Ground
46	VDD0	Analog Supply

(To be continued)

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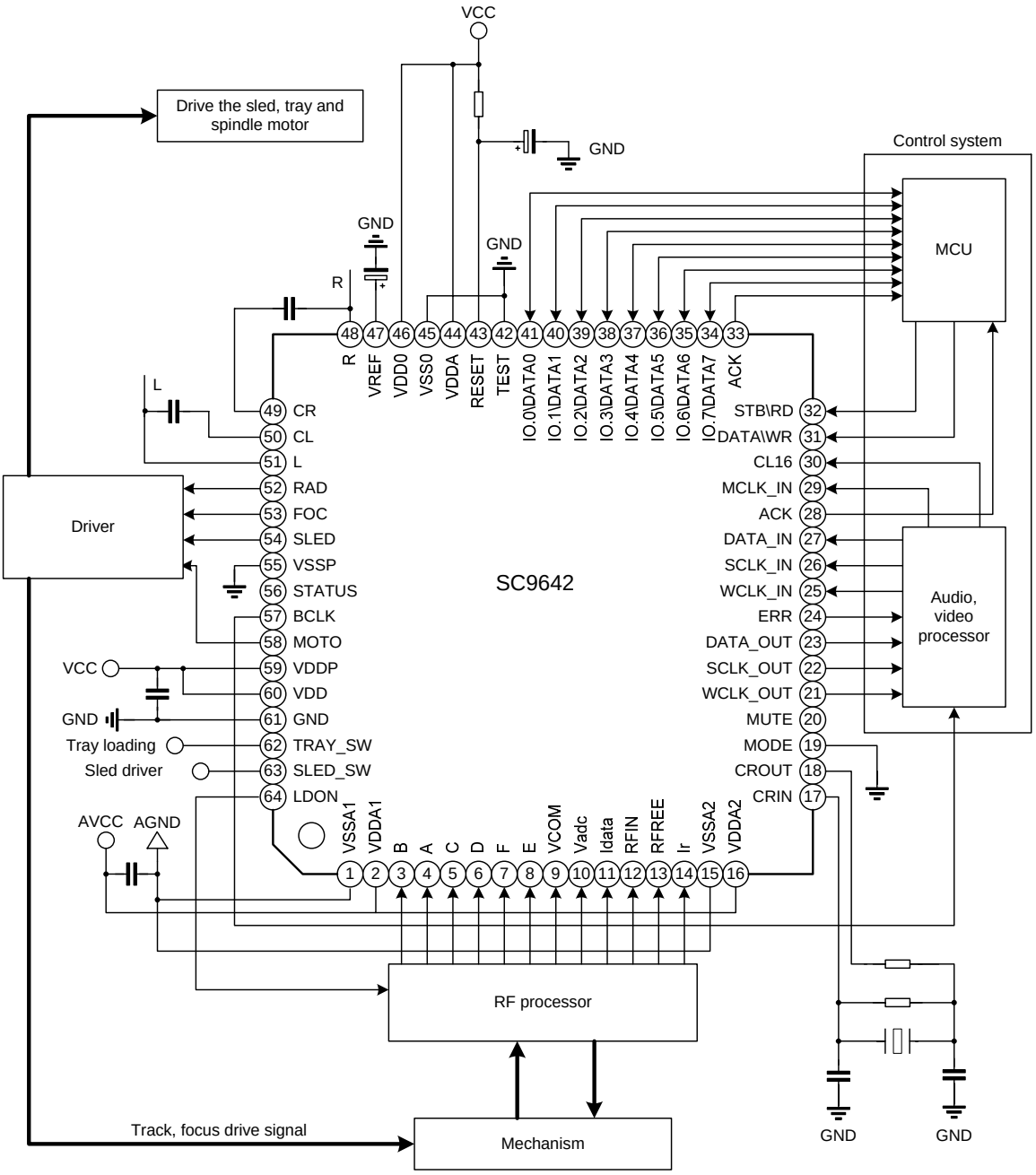
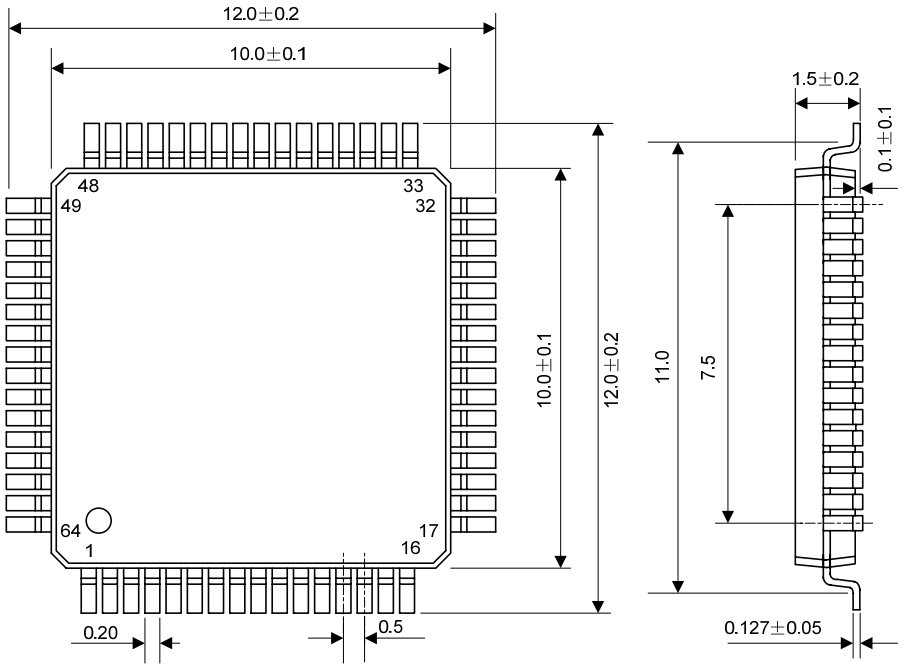
Pin No.	Pin name	Descriptions
47	VREF	Internal reference voltage for output channels
48	R	Digital audio right channel output pin.
49	CR	Digital audio right channel filter pin.
50	CL	Digital audio left channel filter pin.
51	L	Digital audio left channel output pin.
52	RAD	Tracking drive output
53	FOC	Focus drive output
54	SLED	Sled drive output
55	VSSP	Ground
56	STATUS	Shake signal output (high active, used for anti-seismic system)
57	BCLK	75Hz frame sync signal output pin.
58	MOTO	Spindle drive output.
59	VDDP	Digital power supply.
60	VDD	Digital power supply.
61	GND	Digital ground.
62	TRAY_SW	Tray loading position monitor signal input
63	SLED_SW	Sled motor position monitor signal input
64	LDON	Laser control signal output (active high)

TYPICAL APPLICATIONS CIRCUIT



PACKAGE OUTLINE

LQFP-64-10x10-0.5 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.