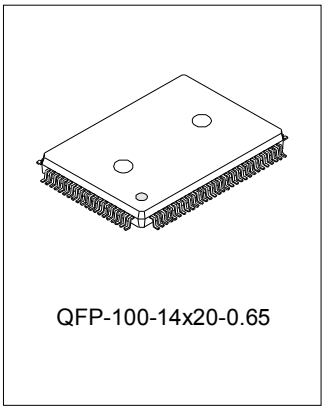
CD SERVO CONTROLLER WITH MCU (WITH DTS AND CLOCK)

DESCRIPTIONS

SC9699P is a desktop audio controller with mature function. The circuit includes CD digital servo control, CD signal processor, and reception frequency counting display, audio DAC and serial interface.



QFP-100-14x20-0.65

FEATURES

* CD play function
* Audio DAC function
* Clock function
* Reception frequency counting
* Serial interface control

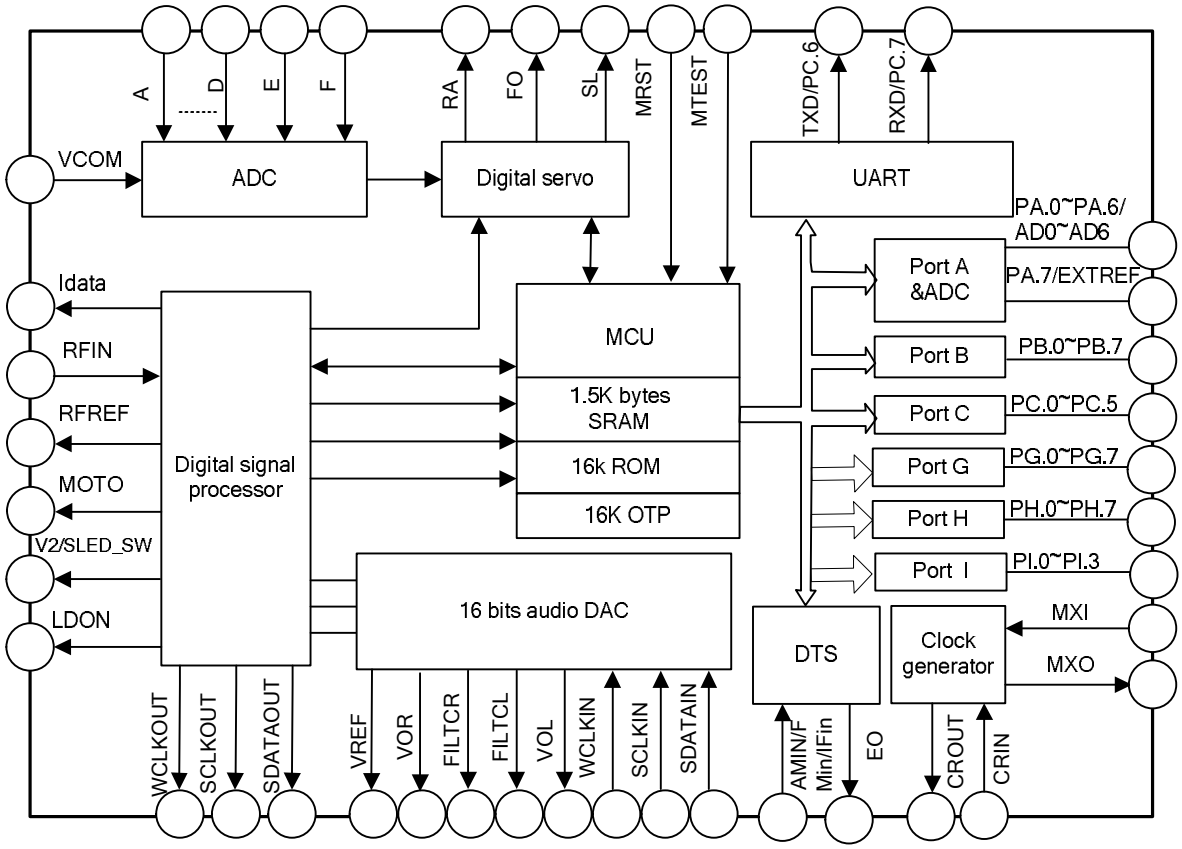
APPLICATIONS

* Desktop audio system

ORDERING INFORMATION

Device	Package
SC9699P	QFP-100-14x20-0.65

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Tamb=25°C)

Characteristics	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.5 ~ +5.5	V
Input Voltage on Pins	V_{IN}	-0.5 ~V_{DD} + 0.5	V
Operating Temperature	Topr	-20 ~ +75	°C

ELECTRICAL CHARACTERISTICS（V_{DD}=4.5~5.5V; V_{SS}=0V; Tamb=-10~+50°C）

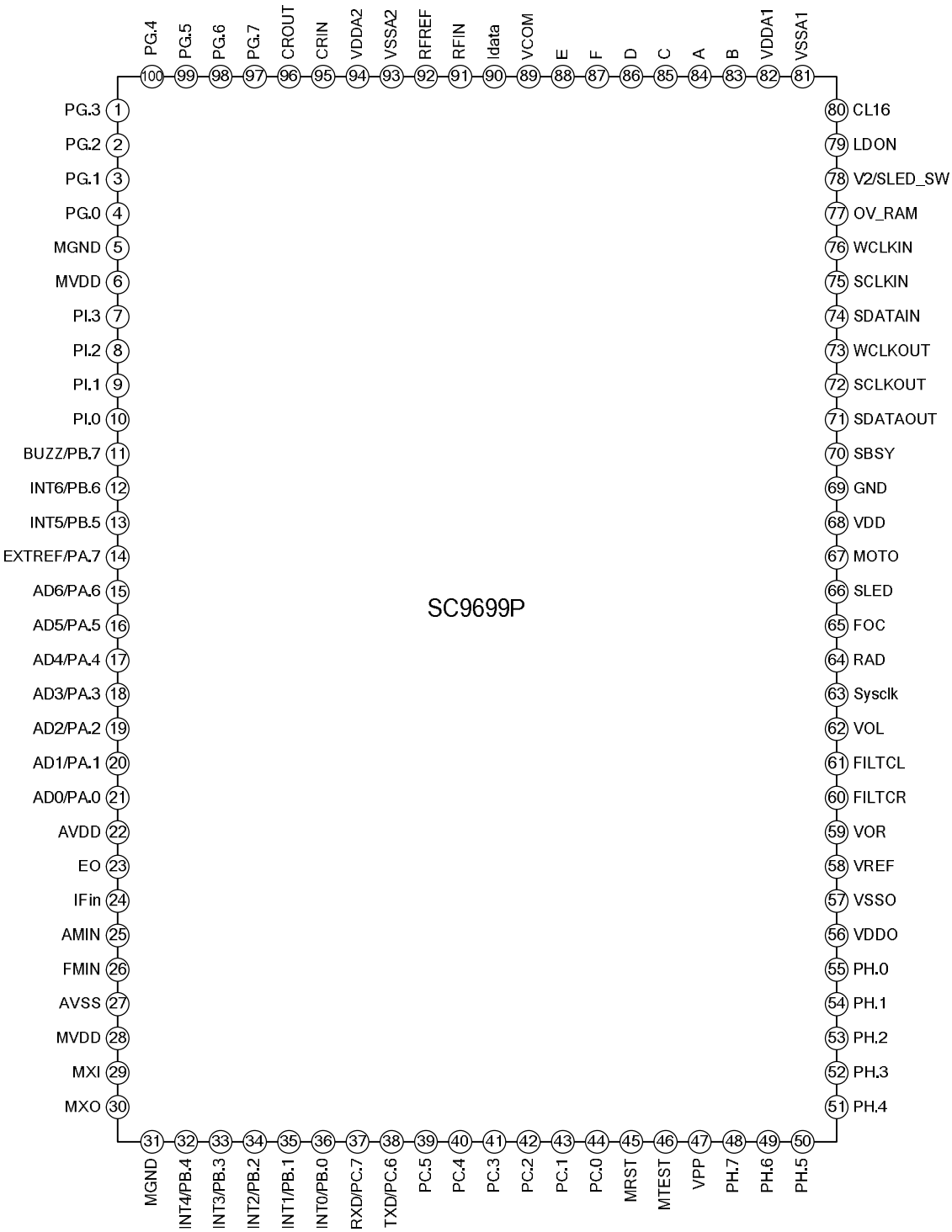
Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Power Supply	V_{DD}	—	4.5	5.0	5.5	V
Power Dissipation	I_{DD}	5V(CD operating)	—	50	—	mA
RFIN Input Signal	V_{RFIN}	—	—	1	—	V
Reference Voltage	V_{Ir}	—	—	0.5V_{DD}	—	
Photoelectricity Signal Bias Input	V_{com}	—	—	2.5	—	V
Input Current Of Central Diode B	I_{DB}	—	0	—	9	μA
Input Current Of Central Diode A	I_{DA}	—	0	—	9	μA
Input Current Of Central Diode C	I_{DC}	—	0	—	9	μA
Input Current Of Central Diode D	I_{DD}	—	0	—	9	μA
Input Current Of Satellite Diode F	I_{RF}	—	0	—	4.5	uA
Input Current Of Satellite Diode E	I_{RE}	—	0	—	4.5	μA
Low-level Input Current at PA Port.	$I_{OL(A)}$	—	—	10	—	mA
High-level Output Current at PA Port.	$I_{OH(A)}$	—	—	5	—	mA
Low-level Input Current at PB Port.	$I_{OL(B)}$	—	—	10	—	mA
High-level Output Current at PB Port.	$I_{OH(B)}$	—	—	5	—	mA
Low-level Input Current at PC Port.	$I_{OL(C)}$	—	—	10	—	mA
High-level Output Current at PC Port.	$I_{OH(C)}$	—	—	5	—	mA
Low-level Input Current at PG Port.	$I_{OL(G)}$	—	—	10	—	mA
High-level Output Current at PG Port.	$I_{OH(G)}$	—	—	5	—	mA

(To be continued)

(Continued)

Characteristics	Symbol	Test condition	Min.	Typ.	Max.	Unit
Low-level Input Current at PH Port.	$I_{OL(H)}$	—	—	10	—	mA
High-level Output Current at PH Port.	$I_{OH(H)}$	—	—	5	—	mA
Low-level Input Current at PI Port.	$I_{OL(I)}$	—	—	10	—	mA
High-level Output Current at PI Port.	$I_{OH(I)}$	—	—	5	—	mA
LDON Low-level Input Current	I_{LDON}	—	0	—	2	mA
Load Resistance DAC	RL	Left channel is the same as the right.	5	—	—	KΩ
Full-Scale DAC Output Voltage	V_{FS}	Left channel is the same as the right.	0.9	1.1	1.2	V
RAD Output Current	I_{RAD}	High level is the same as the low level.	0	1	—	mA
FOC Output Current	I_{FOC}	High level is the same as the low level.	0	1	—	mA
SLED Current	I_{SLED}	High level is the same as the low level.	0	1	—	mA
MOTO Output Current	I_{MOTO}	High level is the same as the low level.	0	5	10	mA
Low Level Output Driving Voltage	$V_{OLDRIVE1}$	RAD, FOC, SELD	0	—	0.4	V
High Level Output Driving Voltage	$V_{OHDRIVE1}$	RAD, FOC, SELD	V_{DD}-0.4	—	V_{DD}	V
Moto Low Level Output Voltage	V_{OLmoto}	—	0	—	1.0	V
Moto High Level Output Voltage	V_{OHmoto}		V_{DD}-1	-	V_{DD}	V
Driving Current of high impedance	$I_{ZODRIVE}$	RAD, FOC, SELD, MOTO	-10	0	+10	μA
DAC Total Harmonic Distortion	THD	0dB 1Khz Signal Input	-	-65	-	dB
DAC output Signal to Noise	S/N	No signal input	-	90	100	dB
DA Filter Attenuation	Filter_DA	0 to 19 KHz	-	-	0.001	dB
		19 to 20 KHz	1	-	2	dB
		24KHz	25	-	-	dB
		25 to 35 KHz	40	-	-	dB
		35 to 64 KHz	50	-	-	dB
		64 to 68 KHz	31	-	-	dB
		68KHz	35	-	-	dB
		69 to 88KHz	40	-	-	dB
OSC Frequency	Fsystem		—	8.4672	—	MHz

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin no.	Pin name	I/O	Descriptions
1	PG.3	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close
2	PG.2	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close
3	PG.1	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close
4	PG.0	I/O	General purpose IO port, input bit by bit control with pull-up, output forced to pull-up
5	MGND	I	MCU and periphery ground
6	MVDD	I	MCU and periphery power supply
7	PI.3	I/O	Common IO port without pull-up or pull-down
8	PI.2	I/O	Common IO port without pull-up or pull-down
9	PI.1	I/O	Common IO port without pull-up or pull-down
10	PI.0	I/O	Common IO port without pull-up or pull-down
11	BUZZ/PB.7	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close, Schmitt input
12	INT6/PB.6	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close, Schmitt input
13	INT5/PB.5	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close, Schmitt input
14	EXTREF/PA.7	I/O	General purpose IO port Also used as AD reference voltage input
15	AD6/PA.6	I/O	General purpose IO port Also used as AD switch channel 6
16	AD5/PA.5	I/O	General purpose IO port Also used as AD switch channel 5
17	AD4/PA.4	I/O	General purpose IO port Also used as AD switch channel 4
18	AD3/PA.3	I/O	General purpose IO port Also used as AD switch channel 3
19	AD2/PA.2	I/O	General purpose IO port Also used as AD switch channel 2
20	AD1/PA.1	I/O	General purpose IO port Also used as AD switch channel 1
21	AD0/PA.0	I/O	General purpose IO port Also used as AD switch channel 0
22	AVDD	I	Power supply for DTS PLL
23	EO	O	DTS PLL error output signal EO

(To be continued)

(Continued)

Pin no.	Pin name	I/O	Descriptions
24	IFin	I	IF signal input
25	AMIN	I	AM frequency counting signal input
26	FMIN	I	FM frequency counting signal input
27	AVSS	I	Ground for DTS PLL
28	MVDD	I	MCU and periphery power supply
29	MXI	I	75K oscillator input port
30	MXO	O	75K oscillator output port
31	MGND	I	MCU and periphery ground
32	INT4/PB.4	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close, Schmitt input
33	INT3/PB.3	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close, Schmitt input
34	INT2/PB.2	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close, Schmitt input
35	INT1/PB.1	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close, Schmitt input
36	INT0/PB.0	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close, Schmitt input
37	RXD/PC.7	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close and also used as serial data receiving.
38	TXD/PC.6	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close and also used as serial data receiving.
39	PC.5	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close
40	PC.4	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close
41	PC.3	I/O	General purpose IO port, open-drain, input bit by bit control with pull-up, output forced to pull-up
42	PC.2	I/O	General purpose IO port, open-drain, input bit by bit control with pull-up, output forced to pull-up
43	PC.1	I/O	General purpose IO port, open-drain, input bit by bit control with pull-up, output forced to pull-up
44	PC.0	I/O	General purpose IO port, open-drain, input bit by bit control with pull-up, output forced to pull-up
45	MRST	I	MCU reset
46	MTEST	I	MCU test port, connect to ground when normal working
47	VPP	I	OTP high voltage download
48	PH.7	I/O	Common IO port without pull-up or pull-down

(To be continued)

(Continued)

Pin no.	Pin name	I/O	Descriptions
49	PH.6	I/O	Common IO port without pull-up or pull-down
50	PH.5	I/O	Common IO port without pull-up or pull-down
51	PH.4	I/O	Common IO port without pull-up or pull-down
52	PH.3	I/O	Common IO port without pull-up or pull-down
53	PH.2	I/O	Common IO port without pull-up or pull-down
54	PH.1	I/O	Common IO port without pull-up or pull-down
55	PH.0	I/O	Common IO port without pull-up or pull-down
56	VDDO	I	DAC analog power supply
57	VSSO	I	DAC analog ground
58	VREF	O	DAC reference voltage output
59	VOR	O	DAC right channel output
60	FILTCR	O	DAC right channel filter capacitor.
61	FILTCL	O	DAC left channel filter capacitor.
62	VOL	O	DAC left channel output
63	Sysclk	I	DAC system clock input
64	RAD	O	Tracking drive output
65	FOC	O	Focus drive output
66	SLED	O	Sled drive output
67	MOTO	O	Spindle drive output
68	VDD	I	Core digital voltage
69	GND	I	Core digital ground
70	SBSY	O	Sub code sync output signal
71	SDATAOUT	O	Audio data output
72	SCLKOUT	O	Data bit clock output
73	WCLKOUT	O	Data word clock output
74	SDATAIN	I	Audio data input
75	SCLKIN	I	Data bit clock input
76	WCLKIN	I	Data word clock input
77	OV_RAM	O	Internal sram overflow signal
78	V2/SLED_SW	I	Sledge motor position monitor signal input
79	LDON	O	Laser control signal output
80	CL16	O	16M clock output
81	VSSA1	I	Ground
82	VDDA1	I	Power supply

(To be continued)

(Continued)

Pin no.	Pin name	I/O	Descriptions
83	B	I	Central diode current signal input 1
84	A	I	Central diode current signal input 2
85	C	I	Central diode current signal input 3
86	D	I	Central diode current signal input 4
87	F	I	Satellite diode current signal input 1
88	E	I	Satellite diode current signal input 2
89	VCOM	I	Photoelectricity Signal Bias Input
90	Idata	O	Data Slice feed-back current output
91	RFIN	I	Reference Signal.
92	RFREF	O	Reference Signal reference voltage/level adjustment reference current output
93	VSSA2	I	Ground
94	VDDA2	I	Power supply
95	CRIN	I	8M oscillator input
96	CROUT	O	8M oscillator output
97	PG.7	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close
98	PG.6	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close
99	PG.5	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close
100	PG.4	I/O	General purpose IO port, input bit by bit control with pull-up, output pull-up close

FUNCTION DESCRIPTIONS

1. MCU

8-bit MCU is the kernel of SC9699P which includes 1.5K EMS memory, 32K program space, where 16K is programmable; Abundant IO ports can be configured flexibly. The details refer to 《SC9699 program guide》.

2. CD servo decoder

CD servo decoder is the main module of SC9699P. It finishes the CD servo and decoder function. Support single and double speed switch, and comply with CD/CD-R/CD-RW.

3. 16-bit audio DAC

Support I^2S data input with maximum word length of 20bit (f_{sys}=256fs) and EIAJ data input with word length of 16, 18, and 20bit (f_{sys}=384fs).

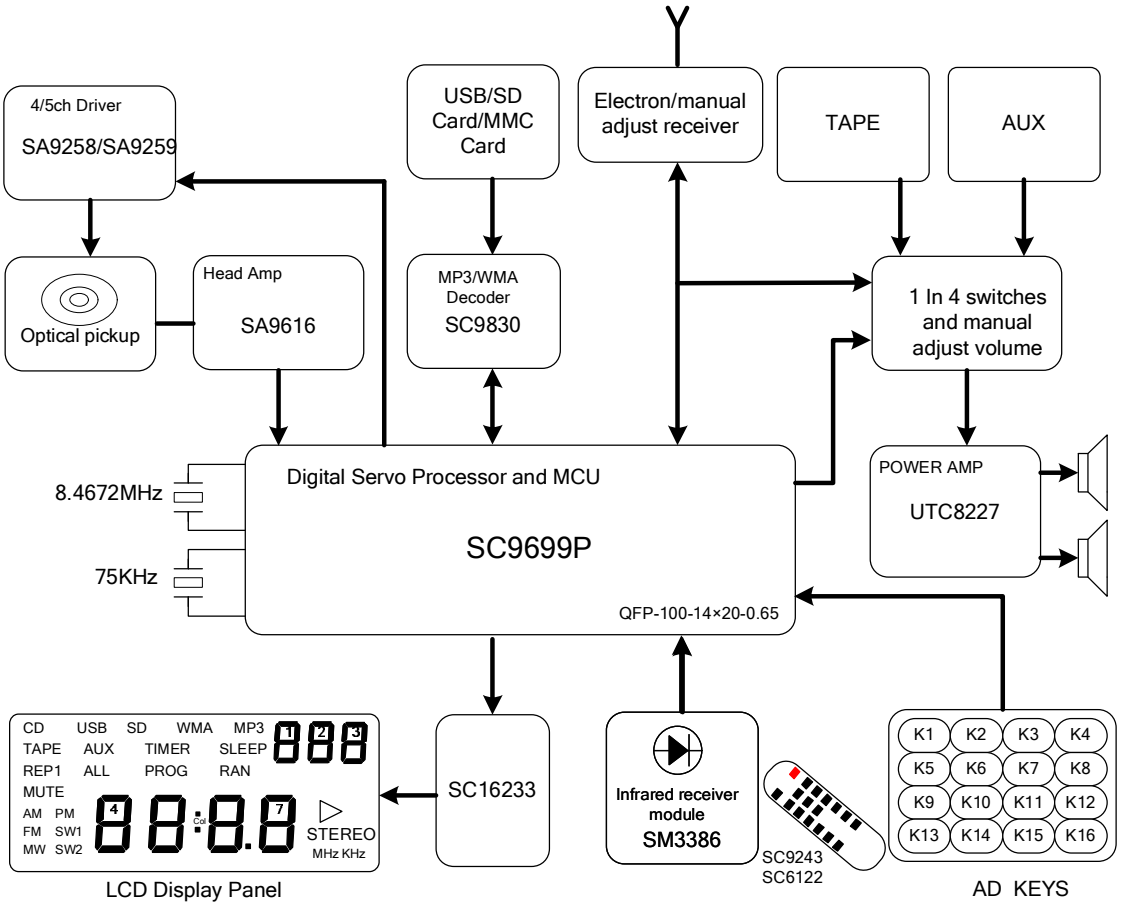
4. DTS module

DTS module is composed of phase locked loop (PLL) and IF counting (IFC) two sections. FM or AM local oscillator signal is amplified and input the program frequency divider, and then the output signal compares with the reference frequency signal to output the error signal. This error signal is switched to control voltage by the external low-pass filter to control the oscillator, and then adjust the frequency is consistent with the program setting value. IF counting circuit includes a 16-bit counter which will count the IF signal within the gating time set by the program.

5. Serial interface

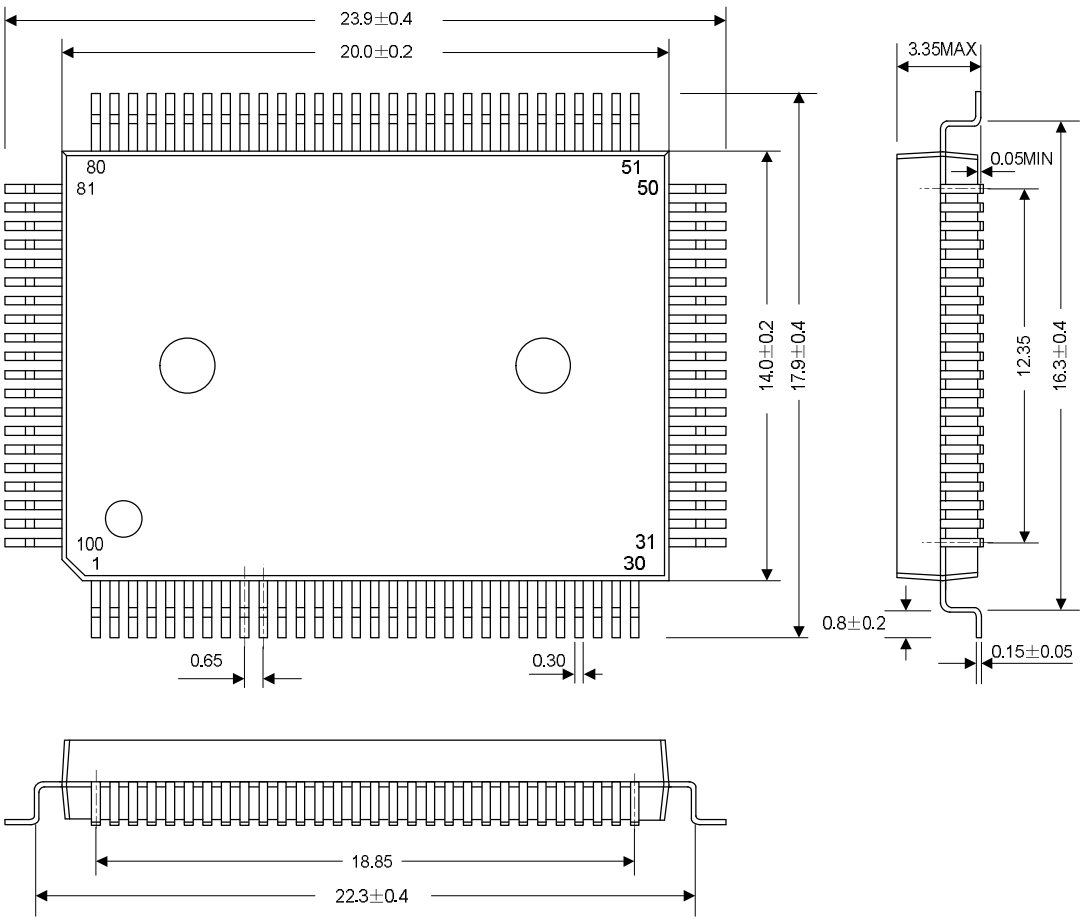
Control the other embedded serial interface system by the serial interface.

TYPICAL APPLICATION CIRCUIT



PACKAGE OUTLINE

QFP-100-14×20-0.65 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

Note: Silan reserves the right to make changes without notice in this specification for the improvement of the design and performance. Silan will supply the best possible product for customers.