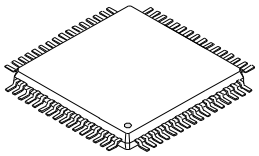
CD ELECTRONIC SHOCKPROOF CONTROLLER

DESCRIPTION

SC9821C is a kind of CD player with electronic anti-shock function.



LQPF-64-10x10-0.5

FEATURES

* Provide 4 compress modes: 16:4, 16:5, 16:6 and non-compress mode
* Provide 3 pairs data, 2 pairs data and direct comparison connect three comparison connect modes.
* Serial host interface
* Support CD-DA straight in mode
* Support SDRAM/DRAM interface
* Only need one external 16.9344MHz crystal oscillator
* Support various play functions: skip forward/backward in track, skip forward/backward between tracks, pause, and play and so on.
* Support 1M/4M/8M/16Mx16 SDRAM, 1M/4M x16 DRAM

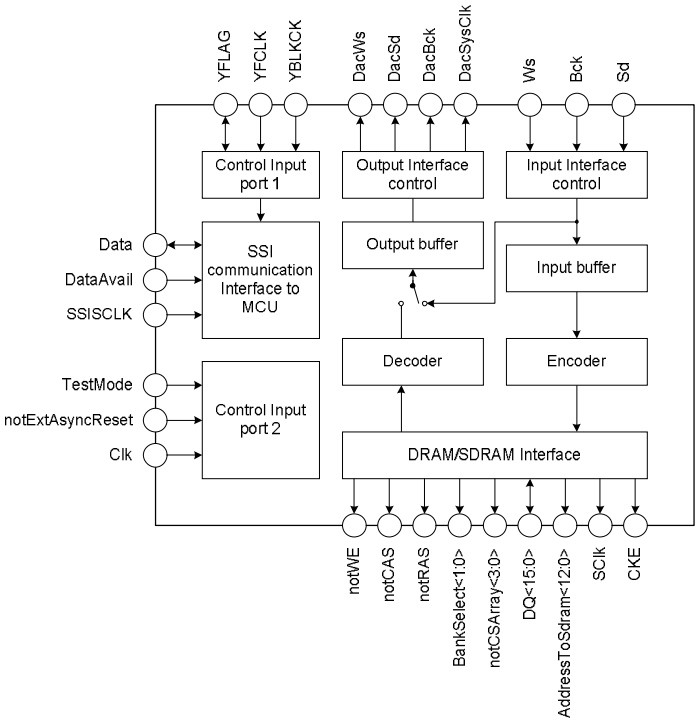
ORDERING INFORMATION

Device	Package
SC9821C	LQFP-64-10X10-0.5

APPLICATIONS

* CD

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

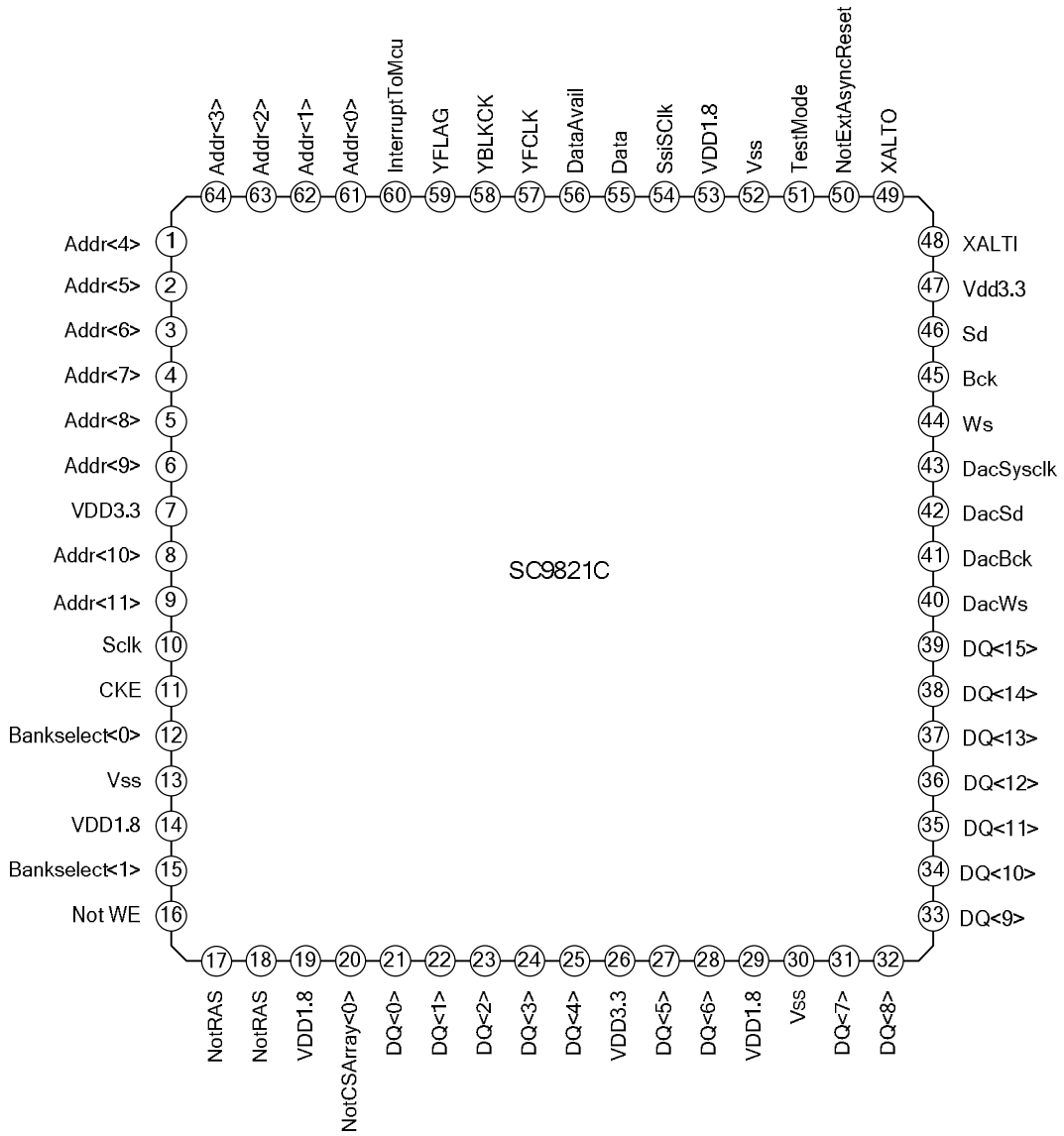
Characteristics	Symbol	Ratings	Unit
Kernel Voltage	V_{CCInt}	1.4 ~ +2.3	V
Port Voltage	V_{CCIO}	2.9~ 4.2	V
Input Voltage	V_{IN}	-0.3 ~V_{CCIO} + 0.3	V
Operating Temperature	T_{amb}	-40~90	°C
Storage Temperature	T_{stg}	-60~150	°C

ELECTRICAL CHARACTERISTICS (V_{CCINT}=1.8V, V_{CCIO}=3.3V, T_{amb}=25°C)

Characteristics	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Kernel Operating Voltage	V_{CCInt}	Normal working		1.6	1.8	2.0	V
Port Operating Voltage	V_{CCIO}	Normal working		3.1	3.3	3.9	V
Quiescent Current	I_{DDInt}	Kernel 's VDD1.8 supply current		--	5.3	--	μA
	I_{DDIO}	Port's VDD3.3 supply current		--	0	--	μA
Operating Current	I_{CCInt}	Kernel 's VDD1.8 supply current		10.1	--	11.9	mA
	I_{CCIO}	Port's VDD3.3 supply current		1.3	--	2.5	mA
Operating Frequency	M_{Clk}	--		--	16.9344	--	MHz
High Level Input Voltage	V_{IH}	--		2.1	--	--	V
Low Level Input Voltage	V_{IL}	--		--	--	0.6	V
High Level Input Current	I_{IH}	Type a[note]	$V_{IN}=V_{DD}$	0	--	--	μA
Low Level Input Current	I_{IL}	Type a[note]	$V_{IN}=V_{SS}$	0	--	--	μA
High Level Output Voltage	V_{OH}	I_{OH}=1mA		--	3.29	--	V
		I_{OH}=2mA		--	3.28	--	
Low Level Output Voltage	V_{OL}	I_{OL}=1mA		--	0.02	--	V
		I_{OL}=2mA		--	0.04	--	
Tri-state Output Leakage Current	I_{OZ}	$V_{OUT}=V_{SS}$ or V_{DD}		0	--	--	μA
Output Short current	I_{OS}	V_{DD}=3.3V, $V_O=V_{DD}$		--	47	--	mA
		V_{DD}=3.3V, $V_O=V_{SS}$		--	35	--	

Note: Type a: common input ports.

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin name	I/O	Pin descriptions
1	Addr<4>	O	SDRAM/DRAM address pin 4
2	Addr<5>	O	SDRAM/DRAM address pin 5
3	Addr<6>	O	SDRAM/DRAM address pin 6
4	Addr<7>	O	SDRAM/DRAM address pin 7
5	Addr<8>	O	SDRAM/DRAM address pin 8
6	Addr<9>	O	SDRAM/DRAM address pin 9
7	VDD3.3	I	Power supply for chip ports(3.3V)

(To be continued)

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Pin No.	Pin name	I/O	Pin descriptions
8	Addr<10>	O	SDRAM/DRAM address pin 10
9	Addr<11>	O	SDRAM/DRAM address pin 11
10	SClk	O	16.9344M SDRAM/DRAM clock output pin.
11	CKE	O	SDRAM/DRAM clock output enable pin.
12	BankSelect<0>	O	SDRAM/DRAM block selection output pin 0.
13	VSS	I	Ground of chip.
14	VDD1.8	I	Power supply for chip kernel. (1.8V)
15	BankSelect<1>	O	SDRAM/DRAM block selection output pin 1
16	NotWE	O	SDRAM/DRAM write signal output pin which is low active.
17	NotRAS	O	SDRAM/DRAM row address strobe pin which is low active.
18	NotCAS	O	SDRAM/DRAM Column address strobe pin which is low active.
19	VDD1.8	I	Power supply for chip kernel. (1.8V)
20	NotCSArray<0>	O	SDRAM/DRAM chip selection output pin 0 which is low active.
21	DQ<0>	I/O	SDRAM/DRAM data pin 0 with internal pull up resistor.
22	DQ<1>	I/O	SDRAM/DRAM data pin 1 with internal pull up resistor.
23	DQ<2>	I/O	SDRAM/DRAM data pin 2 with internal pull up resistor.
24	DQ<3>	I/O	SDRAM/DRAM data pin 3 with internal pull up resistor.
25	DQ<4>	I/O	SDRAM/DRAM data pin 4 with internal pull up resistor.
26	VDD3.3	I	Power supply for chip ports(3.3V).
27	DQ<5>	I/O	SDRAM/DRAM data pin 5 with internal pull up resistor.
28	DQ<6>	I/O	SDRAM/DRAM data pin 6 with internal pull up resistor.
29	VDD1.8	I	Power supply for chip kernel. (1.8V).
30	VSS	I	Ground of chip.
31	DQ<7>	I/O	SDRAM/DRAM data pin 7 with internal pull up resistor.
32	DQ<8>	I/O	SDRAM/DRAM data pin 8 with internal pull up resistor.
33	DQ<9>	I/O	SDRAM/DRAM data pin 9 with internal pull up resistor.
34	DQ<10>	I/O	SDRAM/DRAM data pin 10 with internal pull up resistor.
35	DQ<11>	I/O	SDRAM/DRAM data pin 11 with internal pull up resistor.
36	DQ<12>	I/O	SDRAM/DRAM data pin 12 with internal pull up resistor.
37	DQ<13>	I/O	SDRAM/DRAM data pin 13 with internal pull up resistor.
38	DQ<14>	I/O	SDRAM/DRAM data pin 14 with internal pull up resistor.
39	DQ<15>	I/O	SDRAM/DRAM data pin 15 with internal pull up resistor.
40	DacWs	O	Word select clock pin output to DAC interface.
41	DacBck	O	Bit clock pin output to DAC interface.
42	DacSd	O	Data pin output to DAC interface.
43	DacSysClk	O	System clock output to DAC interface.
44	Ws	I	Word select clock input pin for CD-DSP interface.
45	Bck	I	Bit clock input pin for CD-DSP interface.
46	Sd	I	Data input pin for CD-DSP interface.

(To be continued)

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Pin No.	Pin name	I/O	Pin descriptions
47	VDD3.3	I	Power supply for chip ports (3.3V)
48	XALTI	I	Crystal oscillator input pin
49	XALTO	O	Crystal oscillator output pin
50	NotExtAsyncReset	I	System reset pin which is low active
51	TestMode	I	Test mode configuration pin (high active, connect to the ground when the chip is not in test mode).
52	VSS	I	Ground.
53	VDD1.8	I	Power supply for chip kernel. (1.8V)
54	SsiSClk	I	Clock input pin of MCU interface
55	Data	I/O	Data pin of MCU interface
56	DataAvail	I	Communication control pin of MCU interface
57	YFCLK	I	Sub code frame sync signal
58	YBLKCK	I	Sub code block sync signal
59	YFLAG	I	CD servo error flag
60	InterruptToMcu	O	Interrupt signal output to MCU, and high active
61	Addr<0>	O	SDRAM/DRAM address pin 0
62	Addr<1>	O	SDRAM/DRAM address pin 1
63	Addr<2>	O	SDRAM/DRAM address pin 2
64	Addr<3>	O	SDRAM/DRAM address pin 3

FUNCTION DESCRIPTION

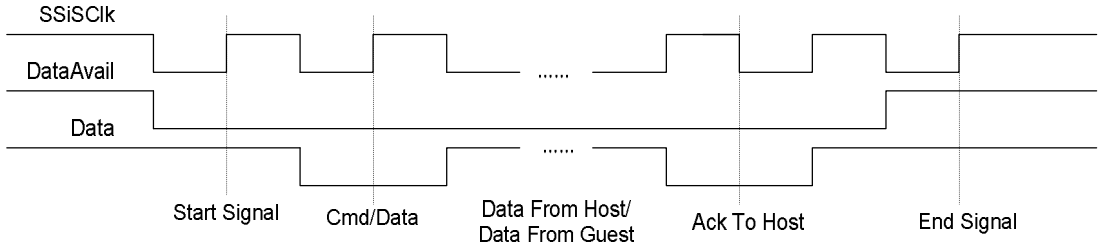
1. INTERFACE FUNCTION

1.1 Interface to main control MCU

SC9821C communicates with MCU through synchronism serial bus (SSI) data interface of SILAN Company.

1.1.1 Serial interface signal form

The serial interface communicating with MCU has 3 signal lines including control signal, data signal, and the signal sequence is as followed:



Where, SsiSClk is the clock generating from Host port, and the frequency can fluctuate in a wide range (as long as the wave is not distortion), and is independent of Guest port; DataAvail used for marking effective data time is also sent by host computer and it is a low active; Data is a bidirectional signal with pull-up resistor and used for specific data communication and feedback. As above picture, the data sent by the host port is all at the falling edge of SsiSClk and the feedback data or Ack signal of guest port are at the rising edge. We define one transmitting process as a frame, and the specification of the coherent signals are as follows:

Start Signal: Start of frame

We define the first checking low level of DataAvail at the rising edge of SsiSClk at Guest port as the start of frame. When check the start signal, the guest can receive the data at the next rising edge.

Data Signal: Data signal

Data signal bit width sent by host computer is one SsiSClk clock cycle.

Ack: Feedback signal

1. When Guest port receives the right addressing data, it feeds back to Host signal. And the width is an SsiSClk cycle. Used for data lead avoiding unmatched signal between two rising edges or corresponding to the data feedback to Host.

2. When Host sends to all Guest ports, signal before sending data is as lead signal, and between two falling edges of SsiSClk.

EndSignal: End of frame

When Guest detects the DataAvail at rising edge of SsiSClk, it means the transmission is end and waits for the next one.

1.1. 2 Serial communication protocol processing

Host and Guest realize the communication between each other by different explanation and processing for the data. The transmission process of one frame is as followed:

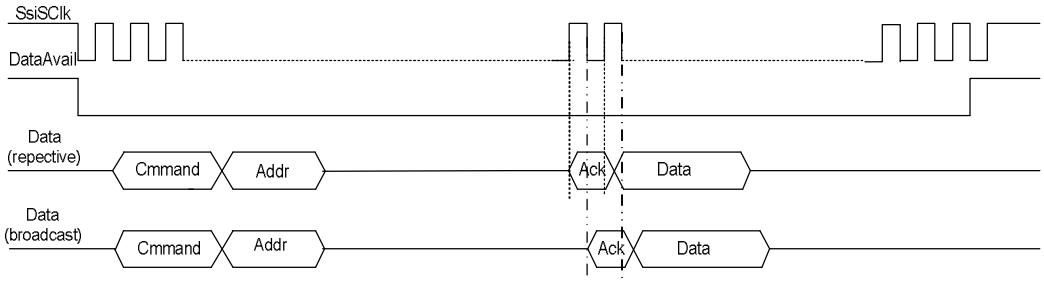


Figure 1 SSI frame signal format

In the above figure, Command pack explains the type of the frame; Addr is 8-bit address length. Data is the transmitting data; the leading Ack is may be given to Guest by Host(Customers address check all mode common), and may be fed back by Guest. That is all decided by the information of Command pack.

Command: In the process of the whole protocol processing, the Command pack byte is critical.

8 bits of Command byte are as followed:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	Burst	Reset	AddrExtend	Address[3]	Address[2]	Address[1]	Address[0]

Read/Write: Read-write flag bit; 1 denotes read data from Guest to Host, and 0 denotes the data flow is from Host to Guest.

Burst: Cooperate with Reset

Reset: When Burst is 0, reset is 1, denotes appointed Guest reset, at this time, have no next byte; When Burst and Reset are 1 at the same time, denotes short command form. The form of short command is introduced in “short command register”.

AddrExtend: 1 denotes this operation based on 16-bit address mode, and high 8-bit follows the low 8-bit; 0 is default 8-bit address operation mode.

Address[3:0]:	Assign the operation object. Note: When Address [3:0] = 4'b1111, all the Guests will be operation objects (common), but at this time, the Guest should close the feedback channel and only receive the data sending by Host. And when select the only Guest, it can be bidirectional communication (respective).
BurstLength:	Denote the operation length of Burst.
Addr:	8-bit addressing address of Host.
Ack:	It is an acknowledge signal. In the address check all modes; this signal is only used as leading data (low level) to denote the beginning of the data pack because the feedback channel of Guest is closed. In one-to-one mode, After the Guest receives a serial of pack leading with Command byte; it must feed back to Host an Ack signal in defined time which is decided by Host itself. When sending the data, if the transmission direction is from Host to Guest this time, Guest must feed back an Ack signal in defined time every time it receives a data; if overstep, Host will pull up DataAvail and end this transmission. When Host sends the data, if there is other data needed transmission after Host receives the Ack signal, it must transmit following the next cycle; When Host receives data, it must come into receiving state (otherwise end this transmission directly) after Host receives the Ack signal.
Data:	The transmitted data is following the leading Ack signal, and the latter limited a data when Burst is 0. When over the provision data, the receiver may not correspond to Ack signal.

According to above description, if complete the operations from Host to Guest, the read-write operation is as followed:

Adopt 8-bit effective address, and assume the addressing address of guest is 0H:

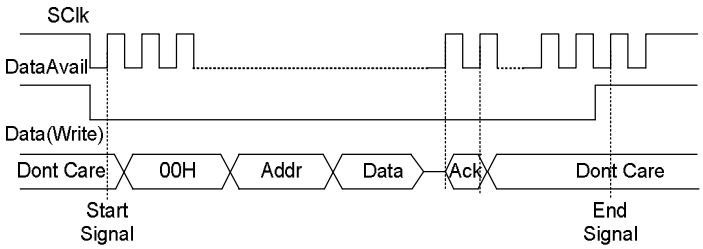


Figure 2 SSI write operation

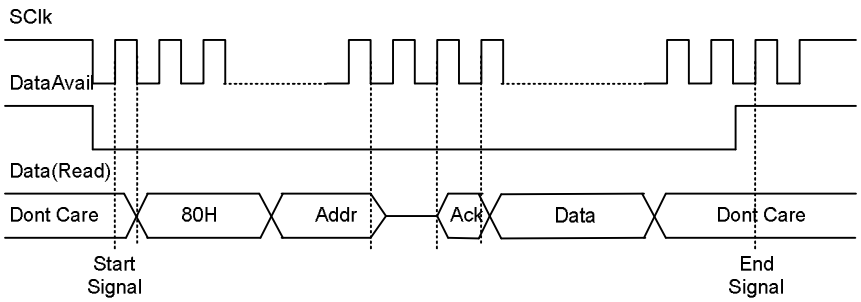


Figure 3 SSI read operation

1.1. 3 SC9821C registers read-write protocol

A single register read command:

S	DevReadCmd	RegAddr	Waiting	Ack	DataFromClient	P

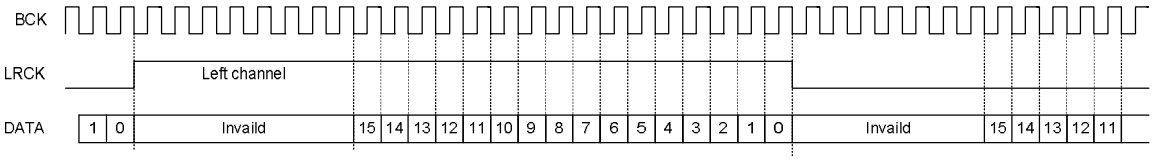
Where, S is Start Signal, P is Stop Signal, DevReadCmd is read command (suppose Guest's address is 1, and DveReadCmd is: 0x81), RegAddr is the address of the register, Waiting is the waiting time of Host, StartAddr is the address of start register when read constantly.

Register single write command:

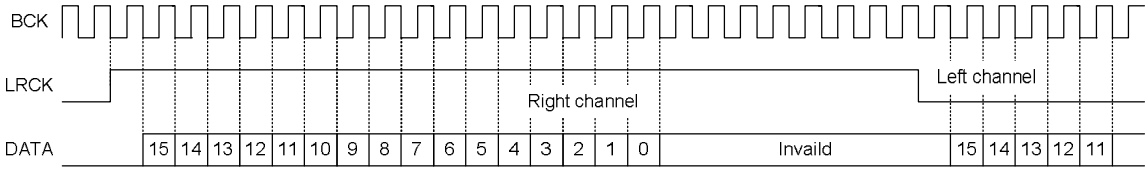
S	DevWriteCmd	RegAddr	Data	Waiting	Ack	p

1.2 Interfaces with CD-DSP

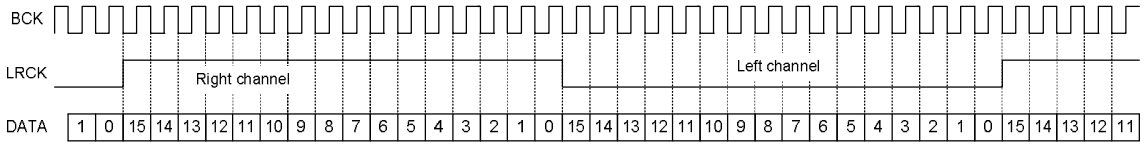
1) 24-bit Bck, the MSB send first, and the data is right flush, the word selection signal of right channel is low (EIAJ-24)



2) 24-bit Bck, the MSB send first, and the data is left flush, the word selection signal of right channel is high (IIS-24)



3) 16-bit Bck, the MSB send first, the word selection signal of right channel is low (EIAJ-16)/ the word selection signal of right channel is high (IIS-16)



2. SHORT COMMAND REGISTER

000:	PwrReset	Soft reset command. The chip is in the reset status after receives this command, until HOST send the UnPwrReset command.
111:	UnPwrReset	Soft release reset command.
001:	PowerOn	Soft power on command.
110:	PowerOff	Soft power off command.
100:	EspMode	Enter the Esp status command.
011:	UnEspMode	Exit the Esp status command.

3. REGISTER FUNCTION

Register description (The register address of SC9821C is 8 bits.)

Symbol	Address	R/W	Initialization	Description
Esp control register				
MSC80H [7:0]	0x50	W	0x00	Bit[0] :Control Esp operate mode 0-> straight in mode 1->electronic shockproof mode Bit[1] : 0-> Esp enable 1-> Esp disable Note: In the normal Esp operation, each time write to MSC80H, this bit should be set to 0. Bit[3:2]: Compare and connect command 00-> stop command 01-> execute command 10-> 2 pairs of commands 11-> 3 pairs of commands Note: During the compare and connect, if receive the new command, it will execute according the new command; and if receive the stop command, it will exit the compare and connect operation, and not output any result. Bit[4] : LocalReset command 0-> NOOP 1->reset the codec Bit[5] : Decode start command 0-> decode disable, 1-> decode enable. Bit[6]: LocalReset command 0-> NOOP 1-> reset the codec Bit[7] : Encode start command 0-> stop encode 1-> start encode Note: When the compare& connect command and encode command occur at the same time, the compare & connect command have the high PRI. If the encode command occurs in the compare & connect process, it will execute the compare and connect command.

(To be continued)

(Continued)

Symbol	Address	R/W	Initialization	Description
MSC83H [7:0]	0x51	W	0x00	Bit[3] : Mute control signal 0-> NOOP 1-> mute operation Bit[6:5] : Set compare & connect modes 00-> 16-bit precision 01-> 12-bit precision others-> 8-bit precision Bit[7] : WAQV signal, is the data valid signal send by MCU. 0-> NOOP 1-> data enable, execute the Valid operation
MSC85H [7:0]	0x52	W	0x00	Bit[3:0] : Encoder operate modes 1000-> non-compress mode, the audio data not compressed, and enter DRAM buffer 0100-> 6-bit compress mode 0010-> 5-bit compress mode 0001-> 4-bit compress mode others-> 6-bit compress mode, this is the default mode. Bit[5:4]: CD shock signal detect modes 00-> YFCKP falling edge, YFLAG＝0, judge it is shock 01-> YFCKP rising edge, YFLAG＝0, judge it is shock 10-> YFLAG＝0, judge it is shock 11-> YFLAG = 1, judge it is shock Bit[6]: SBSY sync modes 0-> SBSY falling edge sync, execute the Latch operation 1-> SBSY rising edge sync, execute the Latch operation Note: The default mode is 0.
Esp status register				
MSC90H [7:0]	0x53	W	0x00	Bit[1]: Decoder stop because the internal reason. 0-> decoder normal operation, (Encoder local reset, register execute the read/write operation, external reset). 1-> decoder stop because the internal reason, (detect the remain valid data is 0).

(To be continued)

(Continued)

Symbol	Address	R/W	Initialization	Description
MSC90H [7:0]	0x53	W	0x00	Bit[2] : Encoder stop because the internal reason: 0->encoder normal operation (compare & connect complete, encoder local reset, external reset). 1->Encoder stop because the internal reason,(FLAG6,,BOVF, MSOVF are set). Bit[3]:Compare and connect operation symbol : 0->not connect the coding (compare & connect complete, compare & connect stop, external reset), 1->execute the coding connect operation (compare & connect command). Note: During the compare & connect, send the encoder start command, it equal to send compare & connect command directly. So there can clear the compare & connect symbol. Bit[5] :Input buffer overflow symbol: 0-> input buffer normal, (this register read data, codec local reset, external reset) 1->input buffer overflow, (input buffer overflow). Bit[6]: External DRAM write overflow symbol: 0-> external DRAM normal write, (this register read data, codec local reset, external reset). 1-> external DRAM write overflow Bit[7]: Shock symbol: 0-> normal operation, no shock, (this register read data, ESP operate mode from straight in switch to shockproof mode, external reset). 1-> CD shock, (detect the CD vibrate)

(To be continued)

(Continued)

Symbol	Address	R/W	Initialization	Description
SC91H [7:0] Note: The flag of this register denotes the state signal; if the status is not satisfied, the corresponding bit will clear automatically.	0x54	R	0x00	Bit[2] : Restore operate status signal 0-> the current Restore operation not execute(have been complete) 1-> Restore is operating Note: In normal, Restore operate time is very short, so this signal should remain 0. Bit[3] : LocalReset status signal 0-> none LocalReset operation 1-> LocalReset operating Note: In normal, LocalReset operate time is very short, so the status signal remain 0. Bit[4]: Decoder operation status signal 0-> decoder stop 1-> decoder operate Bit[5]: Encoder operation status signal: 0-> encoder stop, 1-> encoder operate Bit[6]: Dram overflow symbol 0-> Dram in normal 1-> Dram overflow Bit[7]: Dram empty symbol 0-> Dram have valid data supply for decoder, 1-> Dram empty, no valid data supply for decoder.
MSC92H High[7:0]	0x55	R	0x00	Bit[7:0]: The remain valid data in DRAM take page as unit. The high 8 bit data, each page is 256×16bit.
MSC92HLow [7:0]	0x56	R	0x00	Bit[7:0]: The remain valid data in Dram take page as unit, there is the low 8 bits, each page is 256×16bits. Note: because the 16 bit pointer divide two parts for read operation, in the reading, the pointer also operating, so we should notice the carry bit in reading operation of main control processing.

(To be continued)

(Continued)

Symbol	Address	R/W	Initialization	Description
Esp configuration register				
BitStreamType[7:0]	0x76	W	0x00	bit[3:2] is CD-DA input interface, and bit[1:0] is DAC output interface. bit3: 1: the input is IIS interface 0: the input is EIAJ interface bit2: 0: the input word clock has 16 bitclk 1: the input word clock has 24 bitclk bit1: 1: the output is IIS interface 0: the output is EIAJ interface bit0: 0: the output word clock has 16 bitclk 1: the output word clock has 24 bitclk
BitPoolPageLimitHigh [7:0]	0x58	W	0x07	BitPoolPageLimitHigh and BitPoolPageLimitLow form the up limit of DRAM addressed by BitPool, and determined the DRAM space as ESP buffer; Note: the external DRAM space of BitPool address which can be accessed by BitPool is Page[0, BitPoolLimitHigh & BitPoolPageLimitLow]. In the current MCU, each page is 256×16bit
BitPoolPageLimitLow [7:0]	0x59	W	0xff	
ShockMsk[7:0]	0x5B	W	0x00	Shock signal shield register. It's unit is 128*59ns=7.552us, if the signal length is less than input time, it is not consider the shock. The max. shock shield time is 255x7.552us = 1,925.880 us.
Register in the Mmu module				
MmuHostCmd[7:0]	0x00	RW	0x08	Bit[2:0]: Control the Sdram operation: 0—>no operation 1—>control Sdram carry out Precharge 2—>control Sdram carry out CBR 3—> control Sdram set modes 4—>enable Sdram refresh

(To be continued)

(Continued)

Symbol	Address	R/W	Initialization	Description
MmuHostCmd[7:0]	0x00	RW	0x08	5 — >disable Sdram refresh, but enable Sdram auto refresh. When SDRAM not used in a period, but there should remain the data, it can adopt this mode, then reduce the power dissipation. 6—>DRAM SELF-REFRESH MODE, only for "s" version dram. When enter this mode for more than 100us, DRAM will be in SELF-REFRESH state. you can change mode only by set MmuHostCmd BIT[2:0] to 7(that's change to normal mode of dram) 7—> DRAM NORMAL MODE, before read or write operation of DRAM, you should enter NORMAL MODE for 200us for DRAM initiate (auto execute internal 8 cycles of refresh to initiate dram device) Bit[3] : Enable Sdram initialize 0—> enable Sdram initialize, and do it in the control of Bit[2:0] 1—> disable Sdram initialize, *—> FOR DRAM,THIS BIT IS DON'T CARE Bit[7:4] : When use sdram, Bit[7:4] select Sdram 0000: 1BANK*(4096*256 => 1M*16) 0001: 2BANK*(2048*256 => 512K) 0100: 2BANK*(4096*512 => 2M) 0101: 4BANK*(4096*256 => 1M) 0110: 2BANK*(4096*1024 => 4M) 0111: 4BANK*(4096*512 => 2M) 1000: 4BANK*(4096*1024 => 4M) 1001: 4BANK*(8192*512 => 4M) when use dram, Bit[7:4] select dram type: 0110: 4M * 16bit(4K*1K*16) (4k ref) 0101: 4M * 16bit(8K*512*16) (8k ref) 0100: 1M * 16bit(1k*1k*16) (1k ref) 0011: 1M * 16bit(2k*512*16) (4k ref) 0010: 1M * 16bit(4k*256*16) (4k ref) 0001: 256k*16(512*512*16) *note: for dram, access timing of 50ns and 60ns dram are supported!, 70ns haven't been test.

(To be continued)

(Continued)

Symbol	Address	R/W	Initialization	Description
CompareDataBaseAddressHigh [7:0]	0x02	RW	XX	Store the page base address (Bit15－Bit8) of compare & connect data.
CompareDataBaseAddressLow [7:0]	0x03	RW	XX	Store the page base address (Bit7－Bit0) of compare & connect data.
G722StatusBaseAddressHigh [7:0]	0x04	RW	XX	Store the page base address (Bit15－Bit8) of G722 status data.
G722StatusBaseAddressLow [7:0]	0x05	RW	XX	Store the page base address (Bit7－Bit0) of G722 status data.

4. Program Guide

4.1 Enter Esp mode

- First send short command 0x04, then enter Esp mode.

4.2 Configure external Sdram

- HOST need to initialize Sdram. Send the command 0x51 0x52 0x52 0x53 0x54 0x50 0x58 to register MmuHostCmd(8'h00) in turn.
- Host initialized Dram. Send the command 0x47 to register MmuHostCmd(8'h00)
- HOST need to configure the address of comparative data and decoding information. Send the command 0x0f to register CompareDataBaseAddressHigh(8'h02) , send the command 0xf4 to register CompareDataBaseAddressLow (8'h03), send the command 0x0f to register G722StatusBaseAddressHigh(8'h04) and send the command 0xf8 to register G722StatusBaseAddressLow (8'h05).
- HOST need to configure the size of Sdram. Now it can only support page as unit, BitPoolPageLimitHigh(8'h58) BitPoolPageLimitLow(8'h59) .

4.3 Configure audio input and output interface.

- HOST need to configure audio input interface. The input and output are 24 Bitclk of IIS interface. Send the command 0x0f to register BitStreamType (8'h76).

4.4 Configure compress mode, shake detecting mode, and shake signal shield time.

- HOST need to configure the compress mode. There are 4 compress modes to be selected (16: 4 compress, 16:5 compress, 16:6 compress and non-compress), which will send the command to register MSC85H(8'h52).
- HOST need to configure the shake detecting mode. There are 4 modes to be detected(rising edge of sub block sync signal, shake signal low level determinant; falling edge of sub block sync signal, shake signal high level determinant; shake signal low level determinant; shake signal high level determinant), Send the command to register MSC85H(8'h52).
- HOST can configure shake signal shield time. Because Cd servo only receives some very short level jam signal, but not the signal we need, we can solve this problem by setting the shake signal shield time.

Send the shielded time to register (8'h5b), the unit is 128*59ns=7.552us, the length of shake signal within the input value, it will not be considered as shake signal. The maximum shake shield time is 255x7.552us = 1,925.880 us.

4.5 Begin to encode and decode

- HOST sends encoding start command. Send 0xa1 to register MSC80H(8'h50).

4.6 Read Q sub code

- Read Q sub code of Cd every other time, and if the Q sub code is not continuous, do not enter Esp control flow, delay and read again. if the Q sub code is continuous, enter Esp main control flow.

4.7 Adopt query method to detect the state

- HOST will send query command every other time. Read register MSC90H(8'h53).

4.8 Send WAQV signal

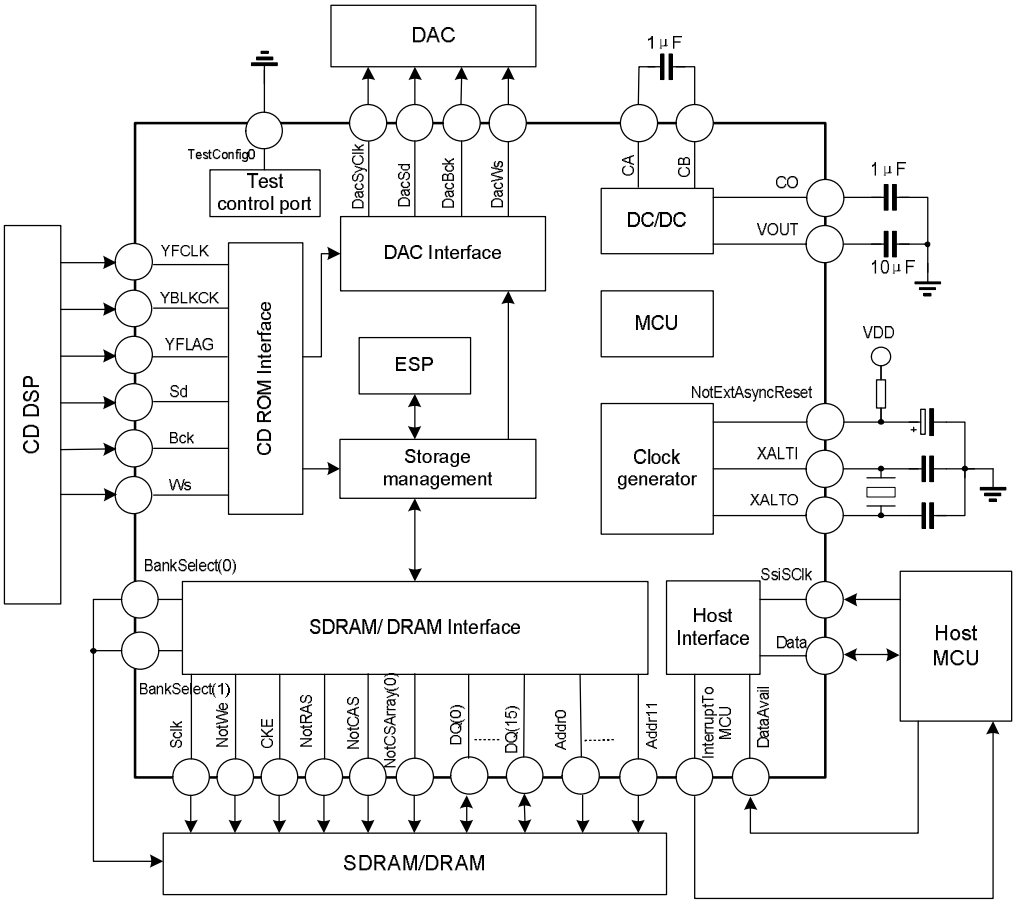
- HOST sends affirm command of effective signal. When the state is normal, send the command 0x80 to register MSC83H(8'h51), and record the current effective address of Q sub code.

4.9 Send the compare& connect command.

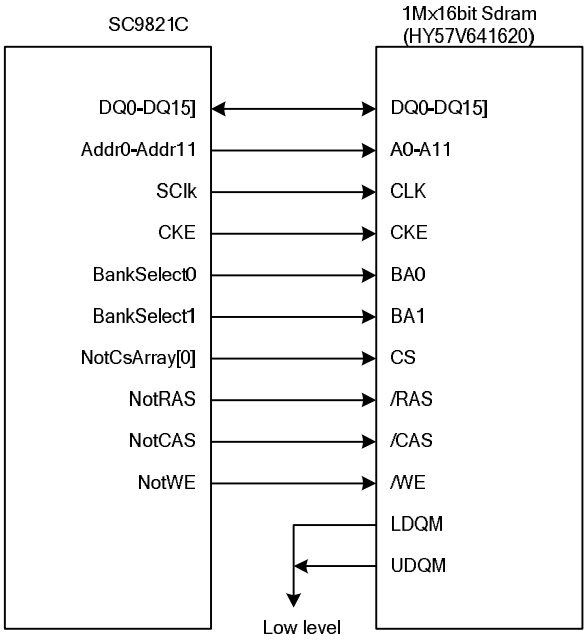
When read the three abnormal states of shake signal, input buffer over flow and Sdram data overflow, take CD back according to the effective address of Q sub code. Then begin to compare& connect to correct data.

- HOST configures the compare&connect command. There are 3 methods (16-bit , 12-bit, 8-bit precision). Send the command to register MSC83H(8'h51).
- HOST sends the compare & connect start command. There are two methods(3 pairs data comparative, direct compare & connect). Send the command to register MSC80H(8'h51).

TYPICAL APPLICATION CIRCUIT

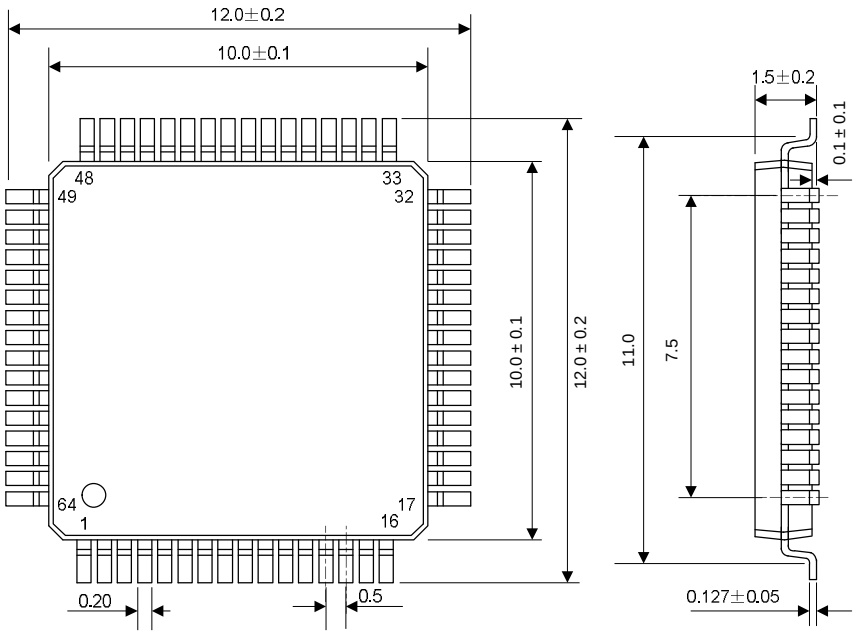


SC9821C CONNECT MEMORY SCHEMATIC



PACKAGEOUTLINE

LQFP-64-10x10-0.5 Unit : mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.