Sept. 2024

# SCB18X128XX0AF

## 128Mbit DDR OPI Xccela PSRAM
## EU RoHS Compliant Products

# Data Sheet

**Rev. H**

| Revision History | | |
|---|---|---|
| **Date** | **Revision** | **Subjects (major changes since last revision)** |
| 2022-12-08 | A | 1. P4 IDD spec done<br>2. Marketing want Ron 250ohm, based on Bailu, Ron max is 240ohm, need to discuss |
| 2023-02-02 | B | 1. Table 6, RL 400MHZ and 333MHZ changed<br>2. Table 8, Vendor ID update<br>3. Figure 16 & 18, A3 A0 A0 A0 change to A3 A2 A1 A0<br>4. P4 & P25 TC extend from 105℃to 125℃<br>5. Update 1.2 Table 1<br>6. Remove Table 20 Note |
| 2023-03-14 | C | 1. Table 1 update part number<br>2. P4 operation temperature using extended range 2 and extended range 1<br>3. Table 24 tCEM using extended temp2 and extended temp1 to satisfy retention<br>4. Table 20 operation condition add extended temp 2 and temp 1<br>5. Table 22 & Table 23 IDD items added based on temperature |
| 2023-03-28 | D | 1. Table 6, RL 400MHZ and 333MHZ changed back to v0.1 for same RL and WL |
| 2023-06-27 | E | 1. P4 update IDD;<br>2. P15 change Read variable description and Clock toggle suggestion;<br>3. Figure7 – Figure10, Figure13 correct read DQ preamble and tHZ;<br>4. Table21 – Table22 update IDD value;<br>5. Remove RBX description;<br>6. Add MR8[5] bit description;<br>7. Add MR0[6] bit description;<br>8. Update MR6 description;<br>9. Remove the clock stop recommend in Read/Write;<br>10. Add note of tCSP/tCHD for clock not stop during CE_n High;<br>11. Correct some spell mistakes. |
| 2023-09-6 | F | 1. Fill the blanks in IDD table with TBD;<br>2. Fill the TBD values in AC timing table;<br>3. Update table 1 part number<br>4. Change feature Tj to Tc, and change standard temperature range<br>5. Package ballout remove x8 and notes |
| 2024-07-31 | G | 1. Adding Figure 2 Package Outline Drawing<br>2. Adding part number for component |
| 2024-09-04 | H | 1. Update IDD value of Table 23<br>2. Update description and value of $ISB_{STDDPD}$ in Table 23<br>3. Update $ISB_{EXT1}$/ $ISB_{EXT2}$ / $ISB_{STDroom}$ value of Table 23<br>4. Update Note4/ Note5 of Table 23<br>5. Add Note6 of Table 23<br>6. Update typical value of Table21/Table 22<br>7. Update IDD values of 1.1 Features<br>8. Update tCPH & tDQSCK<br>9. Update tSP/tHD of Table 24<br>10. Update tDS/tDH of Table 25<br>11. Remove Standby and Half Sleep Current @125C of Table 22<br>12. Remove Half Sleep Current @105C of Table 22<br>13. Remove Standby Current @85C of Table 22<br>14. Update tKHKL @300Mhz/333Mhz/400Mhz of Table 24<br>15. Add tHP/tQHS/tQH in Table 25 |

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# Contents

# 1 Overview

This chapter gives an overview of the 128Mbit PSRAM component product and describes its main characteristics.

## 1.1 Features

### Specifications

- Single Supply Voltage
  - VDD=1.8V, VDDmin=1.62V, VDDmax= 1.98V
  - VDDQ=1.8V, VDDQmin=1.62V, VDDQmax= 1.98V
- Interface
  - two Bytes transfers per clock cycle in x8 mode
  - two Words transfer per clock cycle in x16 mode
  - Mode register configurable x8(default) / x16 mode
- Max. clock rate: 400MHz
- Max. data rate: 800MBps for DDR mode -- x8
  1600MBps for DDR mode -- x16
- Organization: 128Mb in x8 mode(default)
  - 16M x 8bits, 128Mb;
  - Column address: CA0~CA10;
  - Row address: RA0~RA12
  - Page size: 2048 Bytes
- Organization: 128Mb in x16 mode
  - 8M x 16bits, 128Mb;
  - Column address: CA0~CA9;
  - Row address: RA0~RA12
  - Page size: 1024 Words
- Refresh: auto-managed
- Operation Temperature
  - Tc = -25℃ ~ +85℃ (standard range)
  - Tc = -40℃ ~ +105℃ (extended range 2)
  - Tc = -40℃ ~ +125℃ (extended range 1)
- Typical mean Room Standby Current
  - 53uA @ 25℃
  - 22uA @ 25℃(Half Sleep Mode with data retained)
- Maximum Standby Current
  - 68uA @ 25℃

### Features

- Low Power Feature
  - Partial Array Self-Refresh (PASR)
  - Auto Temperature Compensated Self-Refresh
  - Configurable refresh rate
  - Half Sleep Mode with data retained
- Software Reset
- LVCMOS output deriver with programmable drive strength
- Support Write Data Mask
- High speed read operation with Data Strobe
- Register Configurable write and read initial latencies
- Burst length
  - max. 2048 Bytes(x8) / 1024 Word(x16)
  - min. 2 Bytes(x8) / 2 Words(x16)
- Wrap & Hybrid Burst
  - 16/32/64/2K Bytes length in x8 mode
  - 16/32/64/1K Words length in x16 mode
- Linear Burst Command
- Optional host control of refresh rate via MR0[7]
- x16 mode can be configured by setting MR8[6] = 1(default is x8 mode and MR8[6] = 0)

## 1.2 Product List

Table 1shows all possible products within the 128Mbit PSRAM generation. Availability depends on application needs.

**Table 1 - Ordering Information for 128Mbit PSRAM**

| Part Number | IO | Temperature Range | Max Frequency | Note |
|---|---|---|---|---|
| SCB18X128800AF-10E | x8 | Tc= -25℃ ~ +85℃ | 400MHz | miniBGA 24L |
| SCB18X128160AF-10E | x16 | Tc= -25℃ ~ +85℃ | 400MHz | miniBGA 24L |
| SCB18X128800AF-10E2 | x8 | Tc= -40℃ ~ +105℃ | 400MHz | miniBGA 24L |
| SCB18X128160AF-10E2 | x16 | Tc= -40℃ ~ +105℃ | 400MHz | miniBGA 24L |
| SCB18X128800AF-10E1 | x8 | Tc= -40℃ ~ +125℃ | 400MHz | miniBGA 24L |
| SCB18X128160AF-10E1 | x16 | Tc= -40℃ ~ +125℃ | 400MHz | miniBGA 24L |
| SCB18X128160AF-05E2 | x16 | Tc= -40℃ ~ +105℃ | 200MHz | miniBGA 24L |

## 1.3 PSRAM Addressing

**Table 2 - 128Mbit PSRAM Addressing**

| Configuration | 16M × 8bits | 8M x 16bits | Note |
|---|---|---|---|
| Internal Organization | 16M × 8bits | 8M × 16bits | |
| Row Address | A[12:0] | A[12:0] | |
| Number of addressable Rows | 8K | 8K | |
| Column Address | A[10:0] | A[9:0] | |
| Number of addressable Columns (page length) | 2048 | 1024 | 1) |
| Page Size | 2K Bytes | 1K Words | 2) |

Note:

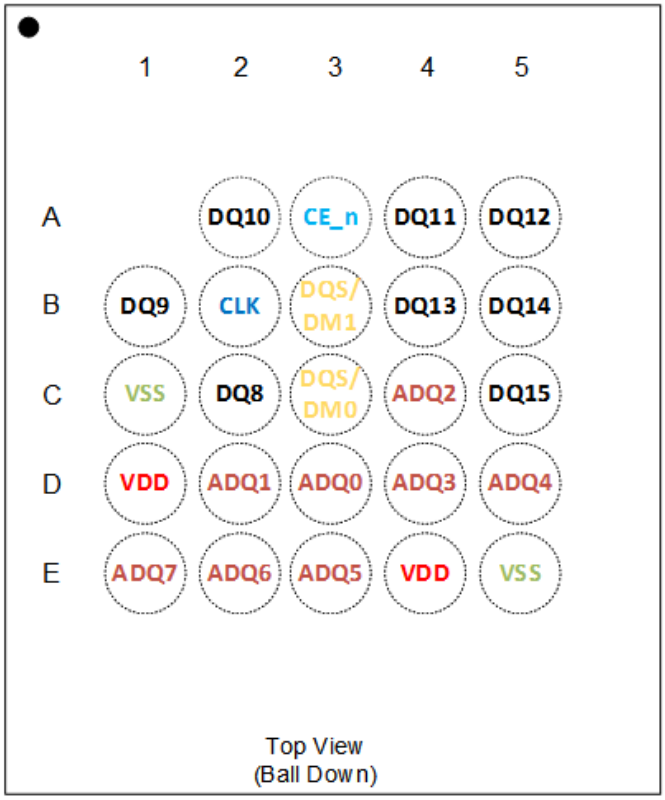
1) Page length is the number of addressable columns and is defined as $2^{COLBITS}$, where COLBITS is the number of column address bits.
2) Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered.

Octal DDR PSRAM device is byte-addressable(x8) / word-addressable(x16). PSRAM accesses are required to start on even addresses (A[0]=’0). Mode Register accesses allow both even and odd addresses.

## 1.4 Package Ballout

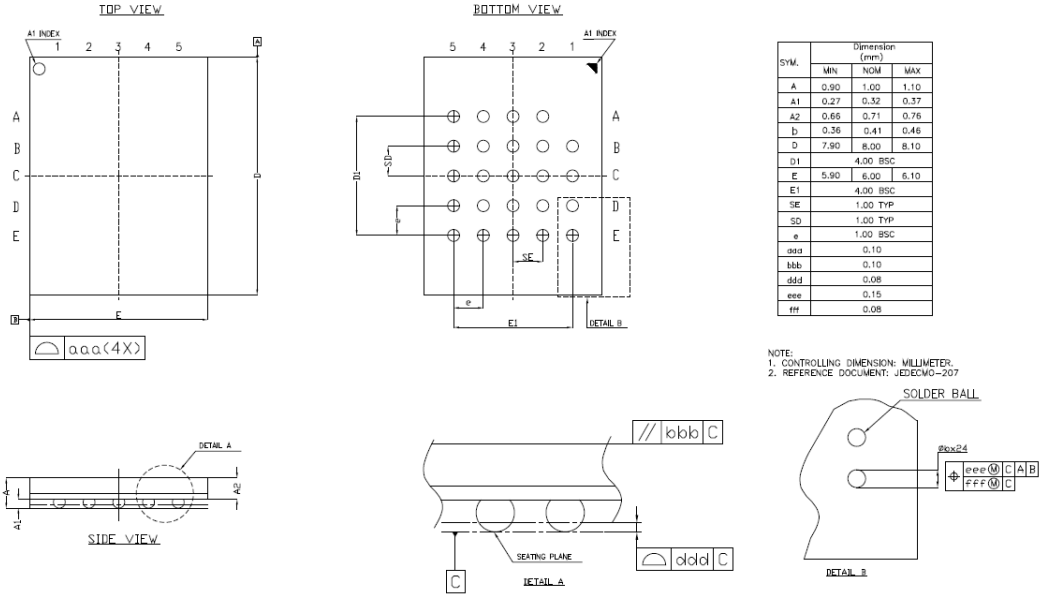
The PSRAM is available in miniBGA 24L package, the Figure 1 is PSRAM Ballout for 128Mb components

**Figure 1 - PSRAM Ballout for 128Mb components**




（6*8*1.0mm）（P1.0）（B0.41）

**Figure 2 - Package Outline Drawing**




| SYM. | Dimension (mm) | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.27 | 0.32 | 0.37 |
| A2 | 0.66 | 0.71 | 0.76 |
| b | 0.36 | 0.41 | 0.46 |
| D | 7.90 | 8.00 | 8.10 |
| D1 | 4.00 BSC | | |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 4.00 BSC | | |
| SE | 1.00 TYP | | |
| SD | 1.00 TYP | | |
| e | 1.00 BSC | | |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ddd | 0.08 | | |
| eee | 0.15 | | |
| fff | 0.08 | | |

## 1.5 Input / Output Signal Functional Description

**Table 3 - Input / Output Signal Functional Description**

| Symbol | Type | Function | Comments |
|---|---|---|---|
| VDD | Supply | Core & IO power supply 1.8V | VDDQ short to VDD internally |
| VSS | Supply | Core & IO supply ground | |
| A/DQ[7:0] | IO | Address and DQ bus[7:0] | used in x8 and x16 mode |
| DQ[15:8] | IO | DQ bus[15:8] | used in x16 mode only |
| DQS/DM[0] | IO | DQ strobe clock for DQ[7:0] during all reads, Data mask for DQ[7:0] during memory writes, DM is active, DM =1 means “do not write” | used in x8 and x16 mode |
| DQS/DM[1] | IO | DQ strobe clock for DQ[15:8] during all reads, Data mask for DQ[15:8] during memory writes, DM is active, DM =1 means “do not write” | used in x16 mode only |
| CE_n | Input | Chip select, active low. When CE_n=1, chip is in standby state. | |
| CLK | Input | Clock | |
| RESET_n | Input | Reset signal, active low, optional as the pad is internally tied to a weak Pull-up and can be left floating | May not be available for all package types |

# 2 Functional Description

## 2.1 Command Truth Tables

The truth tables list the input signal values at a given clock edge which represent a command or state transition expected to be executed by the PSRAM. Table 4 lists all valid commands to the PSRAM.

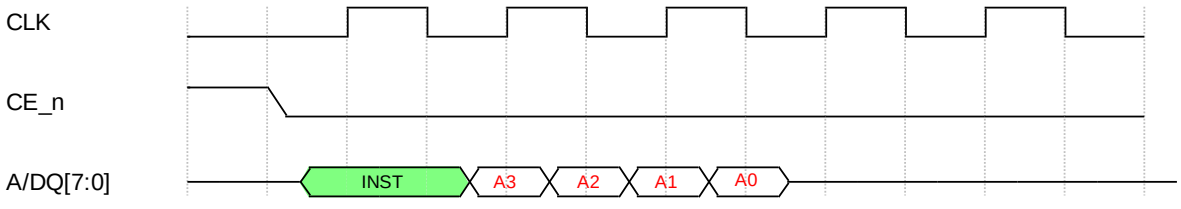
**Table 4- Command Truth Table**

| Function | 1st CLK | | 2nd CLK | | 3rd CLK | |
|---|---|---|---|---|---|---|
| | rising edge | falling edge | rising edge | falling edge | rising edge | falling edge |
| Sync Read | 00h | | A3 | A2 | A1 | A0 |
| Sync Write | 80h | | A3 | A2 | A1 | A0 |
| Sync Read (Linear Burst) | 20h | | A3 | A2 | A1 | A0 |
| Sync Write (Linear Burst) | A0h | | A3 | A2 | A1 | A0 |
| Mode Register Read | 40h | | V | | | MA |
| Mode Register Write | C0h | | V | | | MA |
| Global Reset | FFh | | V | | | |

NOTE1 "V" means "H or L (but a defined logic level)"
NOTE2 A3 = 8'bx unused address bits are reserved and should remain 0
NOTE3 A2 = RA[12:5]
NOTE4 A1 = RA[4:0], CA[10:8], CA[10] is used only in x8 mode
NOTE5 A0 = CA[7:0]
NOTE6 MA= Mode Register Address
NOTE7 The linear burst commands, 20h and A0h, ignore burst setting defined by MR8[2:0]
NOTE8 It is strongly recommended to disable clock(keep low) when CE_n is high

As shown in Figure 2, after CE_n goes LOW, instruction code is latched on 1st CLK rising edge. Access address is latched on the 3rd, 4th, 5th & 6th CLK edges (2nd CLK rising edge, 2nd CLK falling edge, 3rd CLK rising edge, 3rd CLK falling edge).

**Figure 3 - Command and Address latch**



## 2.2 Mode Register

Seven groups of Mode Registers are defined to control various operating modes of PSRAM. Shown in Table 5

**Table 5- Mode Register Table**

| MR num | MA[7:0] | READ/ WRITE | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | `h00 | R/W | TSO | Drive Str ext | LT | Read Latency Code | | | Drive Str. | |
| 1 | `h01 | R | ULP | RFU | | Vendor ID | | | | |
| 2 | `h02 | R | KGD | | | Dev ID | | Density | | |
| 3 | `h03 | R | 0 | 0 | SRF | | RFU | | | |
| 4 | `h04 | R/W | Write Latency Code | | | RF | | PASR | | |
| 6 | `h06 | W | Half Sleep & DPD | | | | | | | |
| 8 | `h08 | R/W | 0 | x8/x16 | High freq. enable | RFU | 0 | BT | BL | |

**Table 6- MR0 Mode register Definition**

| Field | Bits | Description |
|---|---|---|
| **Drive Str** | OP[1:0] | Output Drive Strength codes. Combined with MR0[6].<br>If MR0[6] = 0:<br>00B Full (25Ω default)<br>01B Half (50Ω)<br>10B 1/4 (100Ω)<br>11B 1/8 (200Ω)<br>**If MR0[6] = 1: Output Drive Strength resistor extended by about 1.2 times compare with MR0[6]=0 only when MR0[1:0] =11B. When MR0[1:0] is not 11B, the MR0[6] is unused.** |
| **Read Latency Code** | OP[4:2] | Read latency is related with Read Latency Type(OP[5]).<br>Read latency is pushed out up to LCx2 when internal Refresh is ongoing. |

| | | VL Codes (MR0[5]=0) | | FL Codes (MR0[5]=1) | Max. Input CLK Freq (MHz) | |
|---|---|---|---|---|---|---|
| MR8[5] | MR0[4:2] | Latency (LC) | Max push out (LCx2) | Latency (LCx2) | Standard | Extended |
| 0B | 000B | 3 | 6 | 6 | 66 | 66 |
| 0B | 001B | 4 | 8 | 8 | 109 | 109 |
| 0B | 010B | 5(default) | 10 | 10 | 133 | 133 |
| 0B | 011B | 6 | 12 | 12 | 166 | 166 |
| 0B | 100B | 7 | 14 | 14 | 200 | 200 |
| 0B | 101B | 8 | 16 | 16 | 225 | 225 |
| 0B | 110B | 9 | 18 | 18 | 250 | 250 |
| 0B | 111B | 11 | 22 | 22 | 300 | 300 |
| 1B | 000B | 12 | 24 | 24 | 333 | 333 |
| 1B | 001B | 16 | 32 | 32 | 400 | 400 |

| | | |
|---|---|---|
| **Read Latency Type** | OP[5] | 0B Variable (default)<br>1B Fixed |
| **Drive Strength extend** | OP[6] | Extend driver strength of 200Ohm;<br>Details in MR0[1:0]. |
| **Temperature Sensor Override** | OP[7] | 0B On-die thermal sensor controls refresh rate according to MR4[4:3](default).<br>1B Force refresh rate set by MR4[4:3].(Host takes on role of on-die built-in thermal sensor) |

**Table 7– Operation Latency Code**

| Type | Operation | VL (default) | | FL |
|---|---|---|---|---|
| | | No Refresh | Refresh | |
| Memory | Read | LC | Up to LCx2 | LCx2 |
| | Write | WLC | | WLC |
| Register | Read | LC | | LC |
| | Write | 1 | | 1 |

**Table 8– MR1 Mode register Definition**

| Field | Bits | Description |
|---|---|---|
| **Vendor ID** | OP[4:0] | 11010: UNIIC |
| **Ultra Low Power Device mapping** | OP[7] | 0B Non-ULP (no Half Sleep)<br>1B ULP (Half Sleep supported) |

**Table 9– MR2 Mode register Definition**

| Field | Bits | Description |
|---|---|---|
| **Device Density mapping** | OP[2:0] | 001B 32Mb<br>011B 64Mb<br>101B 128Mb(default)<br>111B 256Mb<br>others reserved |
| **Device ID** | OP[4:3] | 00B Version A(default)<br>01B Version B<br>10B Version C<br>11B Version D |
| **Good-Die Bit** | OP[7:5] | 110B PASS<br>others FAIL<br>Note: Default is FAIL die, and only mark PASS after all test passed. |

**Table 10– MR3 Mode register Definition**

| Field | Bits | Description |
|---|---|---|
| **Self Refresh Flag** | OP[5:4] | MR3[5:4] indicates current device refresh rate. Refresh rate depends on temperature and refresh frequency configuration. Set by MR4[4:3].<br>01B 0.5x Refresh<br>00B 1x Refresh<br>10B 4x Refresh<br>11B reserved |

**Table 11– MR4 Mode register Definition**

<table>
<tr><th>Field</th><th>Bits</th><th>Description</th></tr>
<tr><td>PASR</td><td>OP[2:0]</td><td>If PASR (Partial Array Self-Refresh) is enabled, only data located in the specified areas of the array will be refreshed. This feature can reduce standby current.<br><br>
<table>
<tr><td colspan="5">128Mb x8 (MR8[6] = 0B default) address space RA[12:0],CA[10:0]</td></tr>
<tr><th>Codes</th><th>Refresh Coverage</th><th>Address Space</th><th>Size</th><th>Density</th></tr>
<tr><td>000B</td><td>Full array (default)</td><td>000000h-FFFFFFh</td><td>16M x8</td><td>128Mb</td></tr>
<tr><td>001B</td><td>Bottom 1/2 array</td><td>000000h-7FFFFFh</td><td>8M x8</td><td>64Mb</td></tr>
<tr><td>010B</td><td>Bottom 1/4 array</td><td>000000h-3FFFFFh</td><td>4M x8</td><td>32Mb</td></tr>
<tr><td>011B</td><td>Bottom 1/8 array</td><td>000000h-1FFFFFh</td><td>2M x8</td><td>16Mb</td></tr>
<tr><td>100B</td><td>None</td><td>0</td><td>0M</td><td>0Mb</td></tr>
<tr><td>101B</td><td>Top 1/2 array</td><td>800000h-FFFFFFh</td><td>8M x8</td><td>64Mb</td></tr>
<tr><td>110B</td><td>Top 1/4 array</td><td>C00000h-FFFFFFh</td><td>4M x8</td><td>32Mb</td></tr>
<tr><td>111B</td><td>Top 1/8 array</td><td>E00000h-FFFFFFh</td><td>2M x8</td><td>16Mb</td></tr>
</table>
<br>
<table>
<tr><td colspan="5">128Mb x16 (MR8[6] = 1B) address space RA[12:0],CA[9:0]</td></tr>
<tr><th>Codes</th><th>Refresh Coverage</th><th>Address Space</th><th>Size</th><th>Density</th></tr>
<tr><td>000B</td><td>Full array (default)</td><td>000000h-7FFFFFh</td><td>8M x16</td><td>128Mb</td></tr>
<tr><td>001B</td><td>Bottom 1/2 array</td><td>000000h-3FFFFFh</td><td>4M x16</td><td>64Mb</td></tr>
<tr><td>010B</td><td>Bottom 1/4 array</td><td>000000h-1FFFFFh</td><td>2M x16</td><td>32Mb</td></tr>
<tr><td>011B</td><td>Bottom 1/8 array</td><td>000000h-0FFFFFh</td><td>1M x16</td><td>16Mb</td></tr>
<tr><td>100B</td><td>None</td><td>0</td><td>0M</td><td>0Mb</td></tr>
<tr><td>101B</td><td>Top 1/2 array</td><td>400000h-7FFFFFh</td><td>4M x16</td><td>64Mb</td></tr>
<tr><td>110B</td><td>Top 1/4 array</td><td>600000h-7FFFFFh</td><td>2M x16</td><td>32Mb</td></tr>
<tr><td>111B</td><td>Top 1/8 array</td><td>700000h-7FFFFFh</td><td>1M x16</td><td>16Mb</td></tr>
</table>
Note:<br>CA[10] is ignored in x16 mode.</td></tr>
<tr><td>Refresh Frequency</td><td>OP[4:3]</td><td>x0B Always 4x Refresh(default)<br>01B Enables 1x Refresh when temperature allows<br>11B Enable 0.5x Refresh when temperature allows<br>Note: x = don’t care</td></tr>
<tr><td>Write Latency</td><td>OP[7:5]</td><td>Write latency, WLC, default to 5 after power up<br>Write Latency Code contain MR4[7:5] and MR8[5]
<table>
<tr><th>MR8[5]</th><th>MR4[7:5]</th><th>Write Latency</th><th>Fmax (MHz)</th></tr>
<tr><td>0B</td><td>000B</td><td>3</td><td>66</td></tr>
<tr><td>0B</td><td>100B</td><td>4</td><td>109</td></tr>
<tr><td>0B</td><td>010B</td><td>5(default)</td><td>133</td></tr>
<tr><td>0B</td><td>110B</td><td>6</td><td>166</td></tr>
<tr><td>0B</td><td>001B</td><td>7</td><td>200</td></tr>
<tr><td>0B</td><td>101B</td><td>8</td><td>225</td></tr>
<tr><td>0B</td><td>011B</td><td>9</td><td>250</td></tr>
<tr><td>0B</td><td>111B</td><td>11</td><td>300</td></tr>
<tr><td>1B</td><td>000B</td><td>12</td><td>333</td></tr>
<tr><td>1B</td><td>100B</td><td>16</td><td>400</td></tr>
</table></td></tr>
</table>

**Table 12– MR6 Mode register Definition**

| Field | Bits | Description |
|---|---|---|
| **HSM &DPD** | OP[7:0] | 11110000B Half Sleep mode<br>11000000B Deep Power Down mode<br>others reserved |

**Table 13– MR8 Mode register Definition**

<table>
<tr><th>Field</th><th>Bits</th><th>Description</th></tr>
<tr><td>Burst Length</td><td>OP[1:0]</td><td>The device is power up in 32 Bytes(x8) / 32 Words(x16) Hybrid Wrap, however, non-hybrid burst and other burst length can be set by MR8[2:0]. Minimum write and read burst length is 2 bytes(x8) / words(x16). And no restriction on maximum burst length as long as tCEM is met.</td></tr>
<tr><td>Burst Type</td><td>OP[2]</td><td>
<table>
<tr><th rowspan="2">MR8[2]</th><th rowspan="2">MR8[1:0]</th><th rowspan="2">Burst Length</th><th colspan="2">Example of Sequence of Bytes During Wrap</th></tr>
<tr><th>Starting Address</th><th>Byte Sequence</th></tr>
<tr><td>0B</td><td>00B</td><td>16 Byte/Word Wrap</td><td>4</td><td>[4,5,6,…15,0,1,2,…]</td></tr>
<tr><td>0B</td><td>01B</td><td>32 Byte/Word Wrap</td><td>4</td><td>[4,5,6,…31,0,1,2,…]</td></tr>
<tr><td>0B</td><td>10B</td><td>64 Byte/Word Wrap</td><td>4</td><td>[4,5,6,…63,0,1,2,…]</td></tr>
<tr><td>0B</td><td>11B</td><td>2K Byte/ 1K Word Wrap</td><td>4</td><td>[4,5,6,…2047,0,1,2,…]</td></tr>
<tr><td>1B</td><td>00B</td><td>16 Byte/Word Hybrid Wrap</td><td>2</td><td>[2,3,…15,0,1],16,17,…2047,0,1,…</td></tr>
<tr><td>1B</td><td>01B</td><td>32 Byte/Word Hybrid Wrap (default)</td><td>2</td><td>[2,3,…31,0,1],32,33,…2047,0,1,…</td></tr>
<tr><td>1B</td><td>10B</td><td>64 Byte/Word Hybrid Wrap</td><td>2</td><td>[2,3,…63,0,1],64,65,…2047,0,1,…</td></tr>
<tr><td>1B</td><td>11B</td><td>2K Byte/1K word Wrap</td><td>2</td><td>[2,3,…2047,0,1,2,…]</td></tr>
</table>
</td></tr>
<tr><td>High Freq. Enable</td><td>OP[5]</td><td>High frequency latency enable for 333Mhz and 400Mhz.</td></tr>
<tr><td>x8/x16 mode selectable</td><td>OP[6]</td><td>0B device power up in x8 mode (default)<br>1B device power up in x16 mode<br>Device power up in x8 mode. After power up device can be configured to x16 mode by setting MR8[6]=1 via MRW. Host can switch in and out of x16 mode any time after power up.</td></tr>
</table>

The Linear Burst Write or Read Command (INST[7:0] = A0H or INST[7:0] = 20H) can forces the current array write / read command to do 2K Bytes in x8 mode or 1K Words in x16 mode Wrap (equivalent to having MR8[1:0] set to 2'b11). The burst command write / read linearly from the starting address and wrap back to the beginning of the page upon reaching the end of page. To access a different page, host must issue a new command.

## 2.3 Power-Up Initialization

There is an internal voltage detector to start the automatic initialization process. VDD and VDDQ must be applied simultaneously. When they reach a stable level at or above minimum VDD, the device is in Phase 1 and will require 150µs to complete its auto-initialization process. The user can then proceed to Phase 2 of the initialization described in this section.

During Phase 1 CE_n should remain HIGH (track VDD within 200mV); CLK should remain LOW.

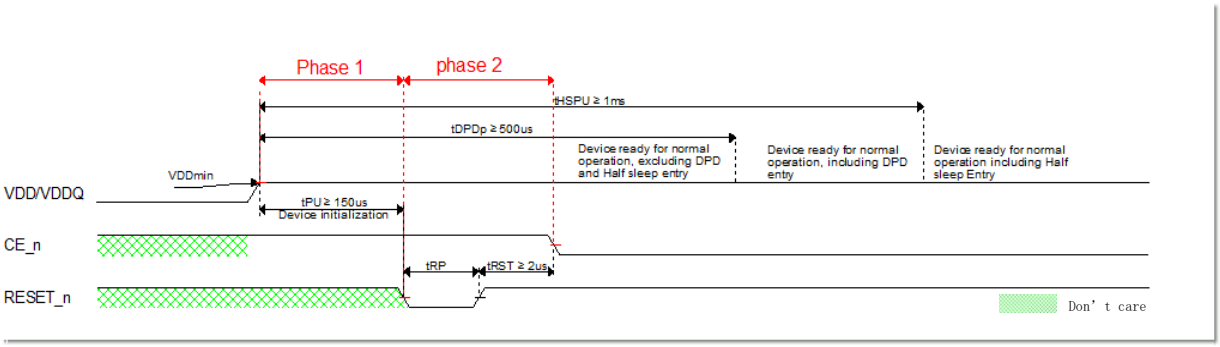
After Phase 2 is complete the device is ready for operation, however Half Sleep entry and Deep Power Down (DPD) entry are not available until Half Sleep Power Up (tHSPU) or DPD Power Up (tDPDp) duration is observed.

There are two method for Power-Up Initialization, By RESET_n pin or by the reset command.

- *Power-Up Initialization by RESET_n pin*

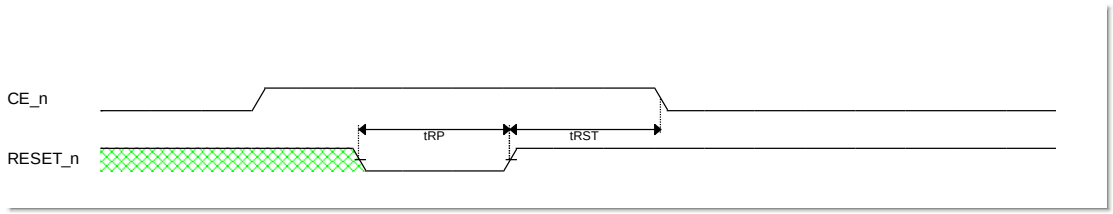
The RESET_n pin can be used to initialize the device during Phase 2 as follows Figure 3:

**Figure 4 - Power-up Initialization with RESET_n pin**




The RESET_n pin can also be used at any time after the device is initialized to reset all register contents. Memory content is not guaranteed after reset. Timing requirements for RESET_n usage are shown below Figure 4:

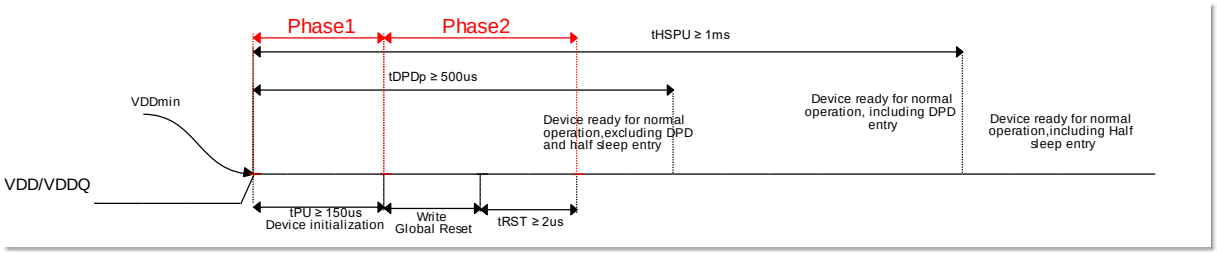
**Figure 5 - Reset_n pin Timing**




- *Power-Up Initialization by Global Reset command*

As an alternate power-up initialization method, After the Phase 1 150µs period the Global Reset command is used to reset the device in Phase 2 as follows Figure 5:

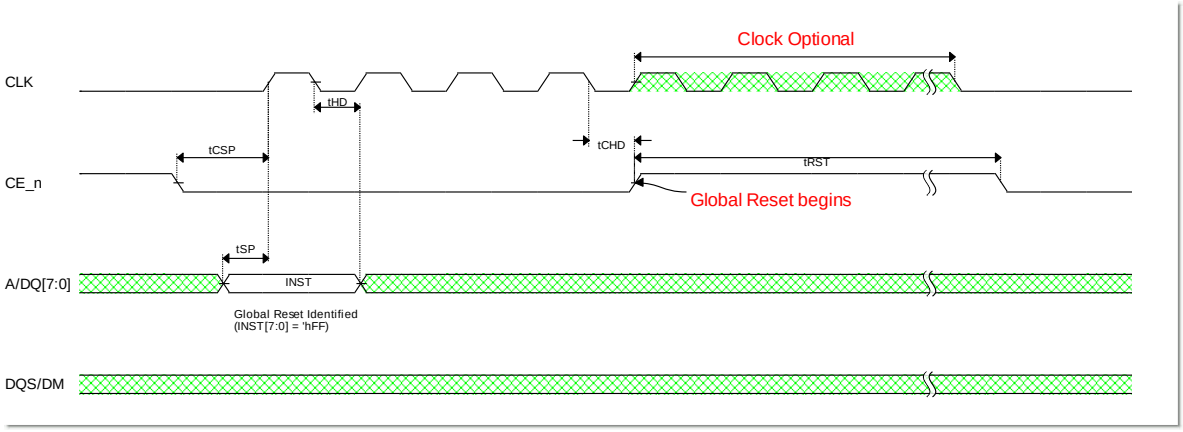
**Figure 6 - Power-Up Initialization with Global Reset command**




The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is

made of 4 clocked CE# lows. Clocking is optional during tRST. The Global Reset command sequence is shown below Figure 6.

**Figure 7 - Global Reset command**




## 2.4 Read

After address latching, the device drive DQS/DM to 0 from next CLK rising edge of the 3rd clock cycle (A1). See Figure 7 below.

Output data is available after Read Latency cycles, as shown in Figure8 & Figure9. Read Latency is defined in MR0[5:2] and MR8[5]. When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 10. Synchronous timing parameters are shown in Table 24 & Table 25.

In case of internal refresh insertion, variable latency output data may be delayed by **up to** (LCx2) latency cycles as shown in Figure 9. True variable refresh push out latency can be anywhere **between** LC to LCx2. The 1st DQS/DM rising edge after read pre-amble indicates the beginning of valid data.

In x16 mode DQ[15:8] will not receiver INST/ADD, instead they will remain Hi-Z until read latency and then start pumping out data, similar to DQ[7:0].

**Figure 8 - Synchronous Read**

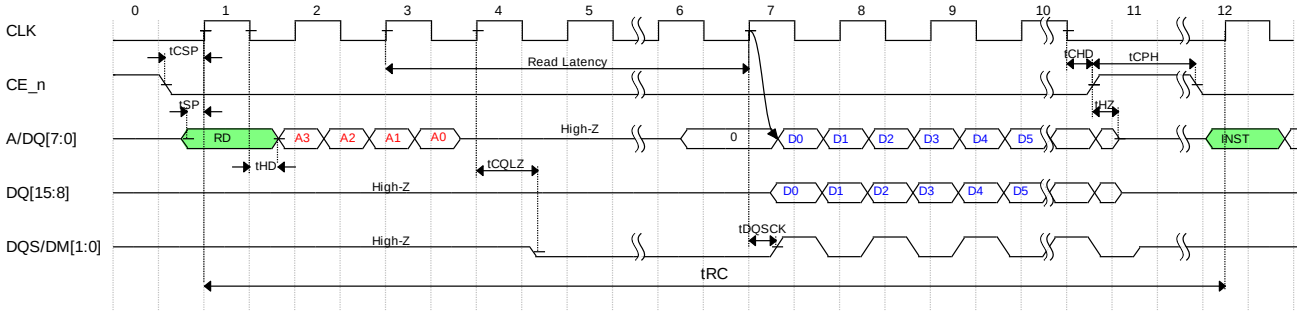


**Figure 9 - Synchronous Read without internal refresh**

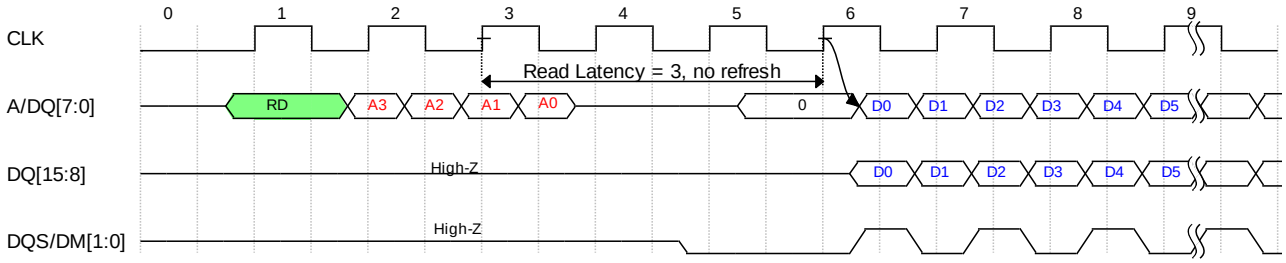



**Figure 10 - Synchronous Read with internal refresh**

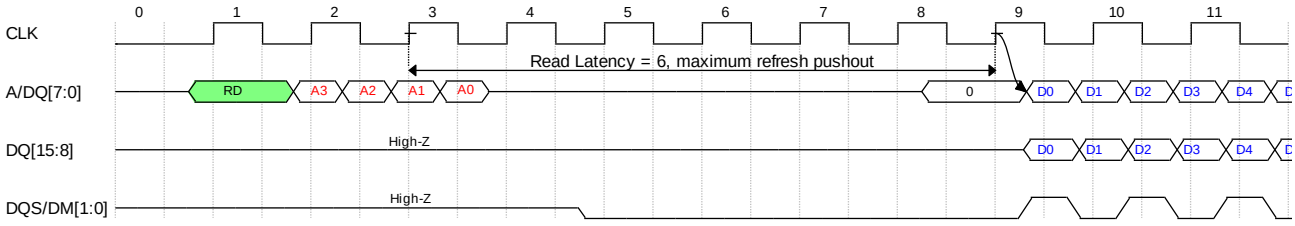
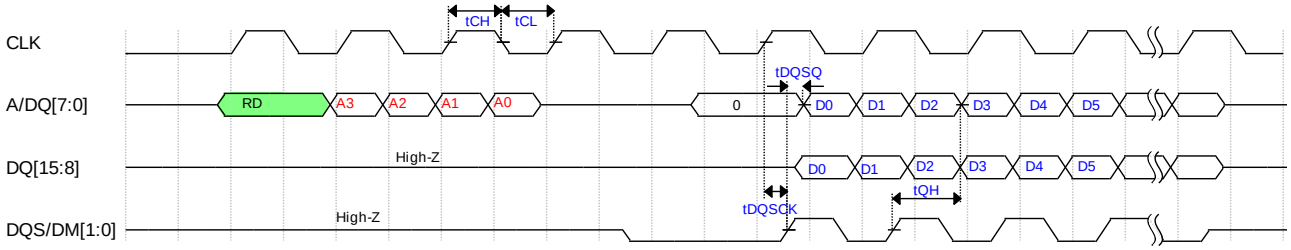



**Figure 11 - Read DQS/DM & DQ timing**




Note:

1) All DQ are valid tDQSQ after the DQS edge, regardless of tDQSCK
2) DQS/DM[1] is DQS/DM for DQ[15:8], DQS/DM[0] is DQS/DM for DQ[7:0]

## 2.5 Write

At least 2 bytes(in x8 mode) / 2 words(in x16 mode) of data must be input in a write operation. For short burst writes tRC must be met, and for long burst writes, tCEM must be met. During write data input DQS/DM is used to mask the corresponding write data, DQS/DM low means the write data is valid and will be written into array, DQS/DM high means the write data is mask as shown in figure 11.

In x16 mode, DQ[15:8] are ignored during INST/ADDR cycles, instead, DQ[15:8] are only used after write latency to receive the data, similar to DQ[7:0], During write data cycle the DQ[15:8] and DQ[7:0] can be independently masked via DM[1] and DM[0].

**Figure 12 - Synchronous Write**

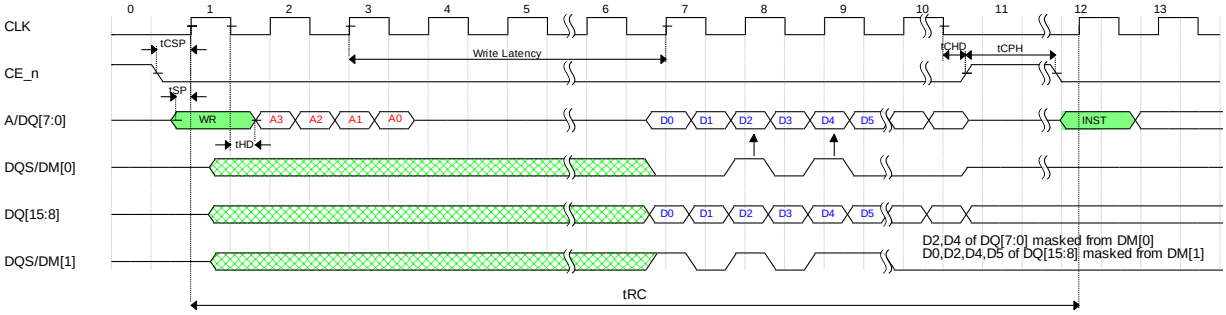
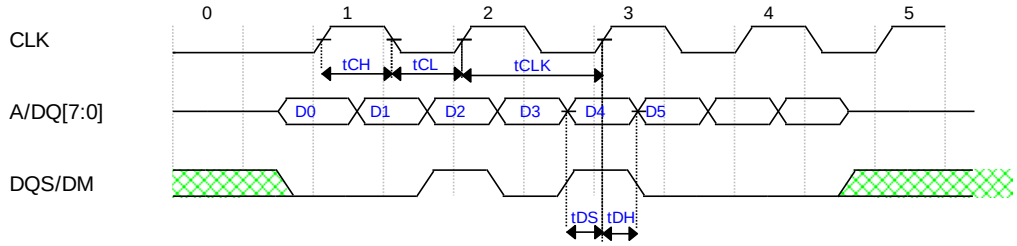



Figure 12 shows the write timing, tDS/tDH are the DQ and DM setup/hold time relates to CLK.

**Figure 13 - Write Timing**




Note: DQS/DM[1] is DQS/DM for DQ[15:8],DQS/DM[0] is DQS/DM for DQ[7:0]

## 2.6 Mode Register Read/Write

All mode registers are 8-bit wide, mode register read and write uses only A/DQ[7:0] and DQS/DM[0] even in x16 mode.

- *Mode Register Read*

Mode Register Read latency defines in 'Table 7 – Operation Latency Code', no push out by internal refresh, As shown in Figure 13, MA indicates which Mode Register content will be read out.

**Figure 14 - Mode Register Read**

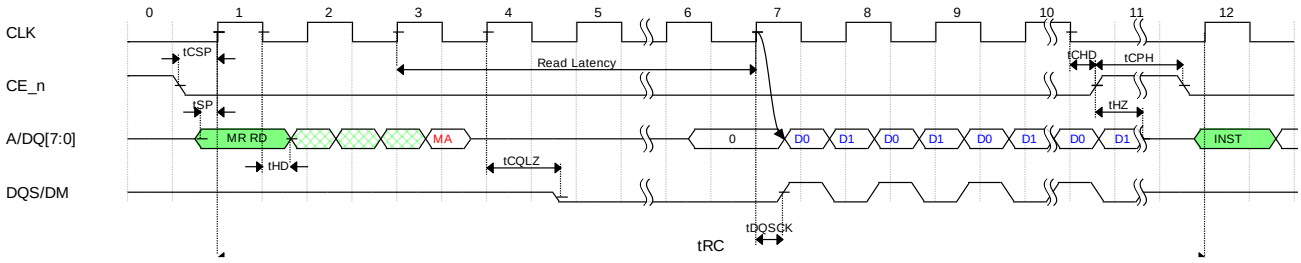



Table 14 shows the relationship of MA and the read out MR data.

**Table 14– MA decoder for MR read**

| MA | D0 | D1 |
|---|---|---|
| 0 | MR0 | MR1 |
| 1 | MR1 | MR2 |
| 2 | MR2 | MR3 |

| | | |
|---|---|---|
| 3 | MR3 | MR4 |
| 4 | MR4 | MR8 |
| 8 | MR8 | MR0 |

- *Mode Register Write*

Register Write latency is fixed to 1, Registers 0, 4 & 8 are read and writable, Registers 1, 2 and 3 are read-only, and Register 6 is write-only.

**Figure 15 - Mode Register Write**

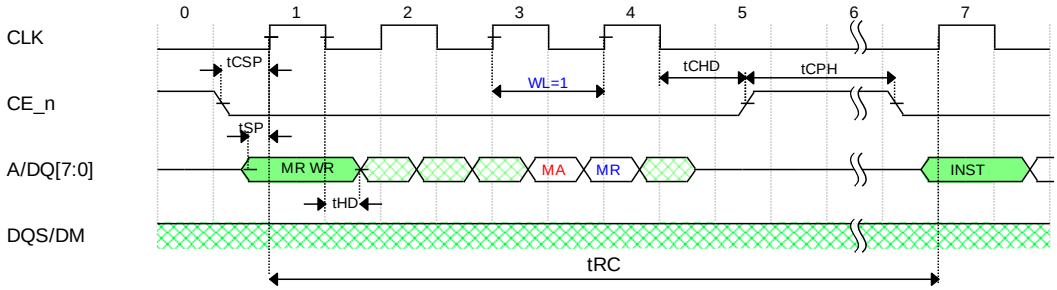



**Table 15– MA decoder for MR Write**

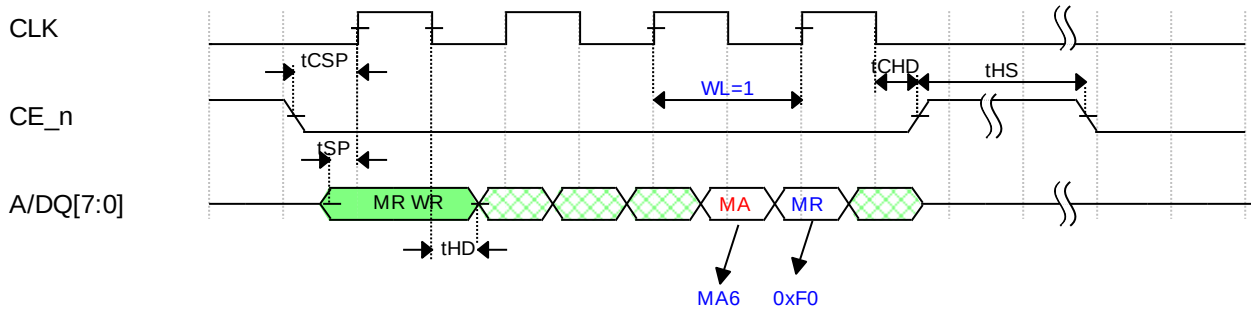
| MA | MR |
|---|---|
| 0 | MR0 |
| 4 | MR4 |
| 6 | MR6 |
| 8 | MR8 |

# 3 Low power features

## 3.1 Half Sleep Mode

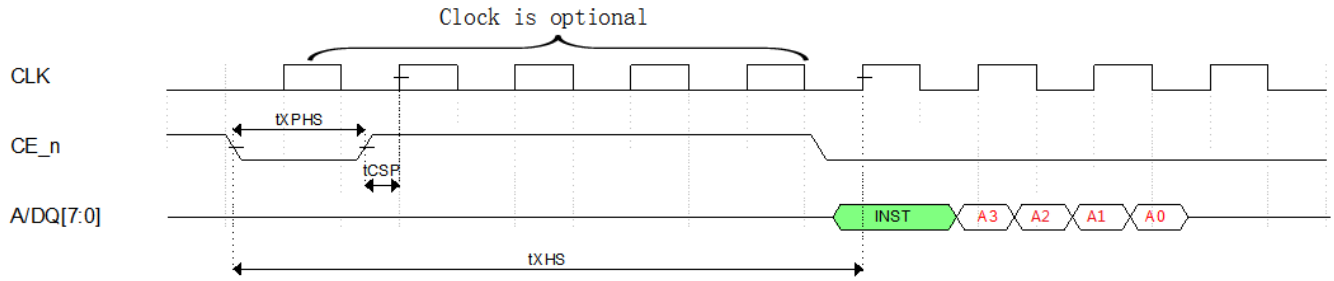
Half Sleep Mode puts the device in an ultra-low power mode with array data is retained. Half Sleep Mode is entered by writing 0xF0 into MR6. CE_n going high initiates the PSRAM into Half Sleep Mode and must be maintained for the minimum duration of tHS. As shown in Figure 15

**Figure 16 - Half Sleep Mode Entry**




Half Sleep Exit is initiated by a low pulsed CE_n. Afterwards, CE_n can be held high with or without clock toggling until the first operation begins (observing minimum tXHS).

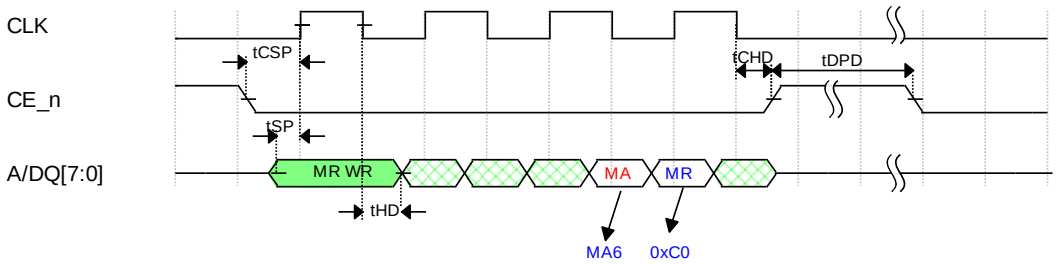
**Figure 17 - Half Sleep Mode Exit**




## 3.2 Deep Power Down Mode

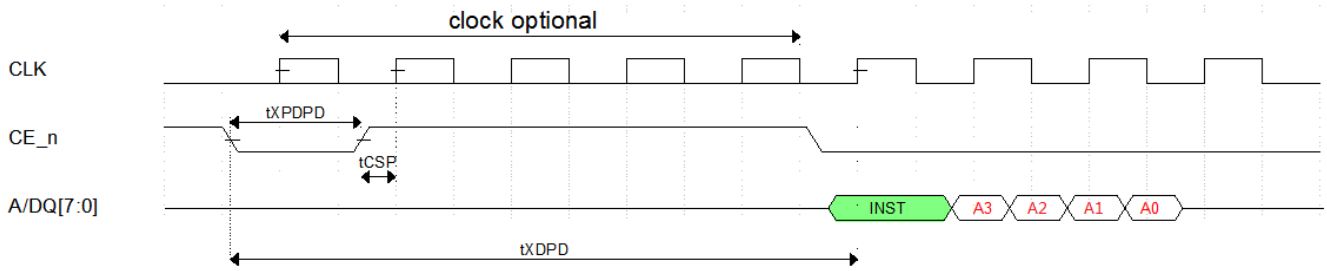
Deep Power Down Mode (DPD) puts the device into power down state without array data retained. DPD Mode Entry is entered by writing 0xC0 into MR6. CE_n going high initiates the DPD Mode and must be maintained for the minimum duration of tDPD. The Deep Power Down Entry command sequence is shown below.

**Figure 18- Deep Power Down Entry**




Deep Power Down Exit is initiated by a low pulsed CE_n. After a CE_n DPD Exit, CE_n must be held high with or without clock toggling until the first operation begins (observing minimum tXDPD).

**Figure 19 - Deep Power Down Exit**




Register values and memory content are not retained in DPD Mode. After DPD mode register values will reset to defaults. tDPDp is minimum period between two DPD Modes (measured from DPD exit to the next DPD entry) as well as from the initial power up to the first DPD entry.

# 4 Operating Conditions and Interface Specification

## 4.1 Absolute Maximum Ratings

**Table 16 - Absolute Maximum Ratings**

| Parameter | Symbol | Rating | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Voltage to any ball except VDD, VDDQ relative to VSS | VT | –0.4 | VDD/VDDQ+0.4 | V | |
| Voltage on VDD supply relative to VSS | VDD | –0.4 | + 2.45 | V | |
| Voltage on VDDQ supply relative to VSS | VDDQ | –0.4 | + 2.45 | V | |
| Storage Temperature | $T_{STG}$ | –55 | +150 | ℃ | 1) |

Notes:
Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## 4.2 Pin Capacitance

**Table 17- Bare Die Pin Capacitance**

| Parameter | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Input Pin Capacitance | $C_{IN}$ | | 1 | pF | $V_{IN}$=0V |
| Output Pin Capacitance | $C_{OUT}$ | | 2 | pF | $V_{OUT}$=0V |

Notes:
1) spec condition is 25℃.

**Table 18- Package Pin Capacitance**

| Parameter | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Input Pin Capacitance | $C_{IN}$ | | TBD | pF | $V_{IN}$=0V |
| Output Pin Capacitance | $C_{OUT}$ | | TBD | pF | $V_{OUT}$=0V |

Notes:
1) spec condition is 25℃.

**Table 19- Load Capacitance**

| Parameter | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Load Capacitance | $C_L$ | | 15 | pF | |

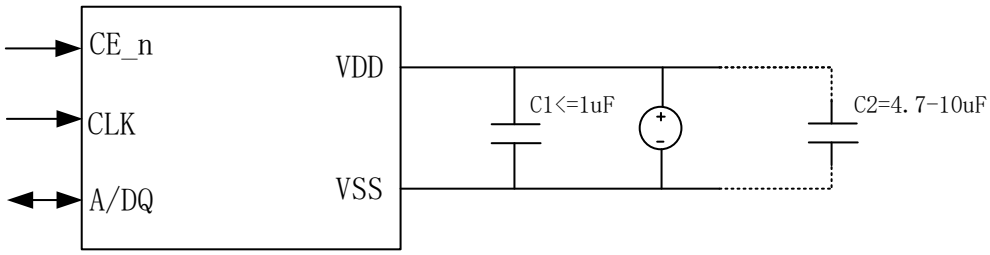
Notes:
1) System $C_L$ for the use package.

## 4.3 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak

currents/usage modes.

**Figure 20 - Decoupling Capacitor**




- Low ESR cap C1

It is recommended to place a low ESR decoupling capacitor of <=1μF close to the device to absorb transient peaks.

- Large cap C2

During Half-sleep modes even though half-sleep average currents are very small (less than 100μA), its peak current from internal periodical burst refresh can reach up to the level of 25mA. The peak current duration can last for few tens of microseconds. During this period if the system regulator cannot supply such large peaks, it is important to place a 4.7μF-10μF cap to cover the burst refresh current demand and replenish the cap before the next burst of refresh.

## 4.4 Operating Conditions

**Table 20– Operating Temperature**

| Parameter | Min. | Max. | Unit | Note |
|---|---|---|---|---|
| Operating Temperature (extended 1) | -40 | 125 | ℃ | |
| Operating Temperature (extended 2) | -40 | 105 | ℃ | |
| Operating Temperature (standard) | -40 | 85 | ℃ | |

## 4.5 ISB Partial Array Refresh Current

**Table 21- Typical PASR Current @ 25℃**

| Standby Current @ 25°C | | | |
|---|---|---|---|
| PASR | ISB –typical mean | Unit | Notes |
| Full | 53 | μA | 1),2) |
| 1/2 | 45 | μA | 1),2) |
| 1/4 | 41 | μA | 1),2) |
| 1/8 | 39 | μA | 1),2) |
| Half Sleep Current @ 25°C | | | |
| PASR | I Half Sleep-typical mean | Unit | Notes |
| Full | 22 | μA | 1),2),3) |
| 1/2 | 18 | μA | 1),2),3) |
| 1/4 | 16 | μA | 1),2),3) |
| 1/8 | 14 | μA | 1),2),3) |

**Table 22- Typical PASR Current @ 105℃/85℃**

| Standby Current @ 105°C | | | |
|---|---|---|---|
| PASR | PASR | PASR | PASR |
| Full | Full | Full | Full |
| 1/2 | 1/2 | 1/2 | 1/2 |
| 1/4 | 1/4 | 1/4 | 1/4 |
| 1/8 | 1/8 | 1/8 | 1/8 |
| Half Sleep Current @ 85°C | | | |
| PASR | PASR | PASR | PASR |
| Full | Full | Full | Full |
| 1/2 | 1/2 | 1/2 | 1/2 |
| 1/4 | 1/4 | 1/4 | 1/4 |
| 1/8 | 1/8 | 1/8 | 1/8 |

Note:
1) Slow Refresh current is only attainable by enabling 0.5x Refresh Frequency (see Table 17)
2) PASR Current is only characterized without CLK toggling.
3) Half Sleep current is only guaranteed after 150ms into Half Sleep mode.

## 4.6 DC Characteristics

**Table 23- DC Characteristics**

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| VDD | Supply Voltage | 1.62 | 1.98 | V | |
| VDDQ | I/O Supply Voltage | 1.62 | 1.98 | V | |
| $V_{IH}$ | Input high voltage | VDDQ-0.4 | VDDQ+0.3 | V | |
| $V_{IL}$ | Input low voltage | -0.3 | 0.4 | V | |
| $V_{OH}$ | Output high voltage (IOH=-0.2mA) | 0.8 VDDQ | | V | |
| $V_{OL}$ | Output low voltage (IOL=+0.2mA) | | 0.2 VDDQ | V | |
| $I_{LI}$ | Input leakage current | | 1 | μA | |
| $I_{LO}$ | Output leakage current | | 1 | μA | |
| ICC | Write @13MHz (x8/x16)( -40 ℃ to 125 ℃) | | 5/5 | mA | 1) |
| | Write @133MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 12/17 | mA | 1) |
| | Write @166MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 14/20 | mA | 1) |
| | Write @200MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 16/23 | mA | 1) |
| | Write @225MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 17/26 | mA | 1) |
| | Write @250MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 19/28 | mA | 1) |
| | Write @300MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 22/33 | mA | 1) |
| | Write @333MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 24/36 | mA | 1) |
| | Write @400MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 27/43 | mA | 1) |
| | Read @13MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 5/6 | mA | 1) |
| | Read @133MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 15/23 | mA | 1) |
| | Read @166MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 17/27 | mA | 1) |
| | Read @200MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 20/32 | mA | 1) |
| | Read @225MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 22/36 | mA | 1) |
| | Read @250MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 23/39 | mA | 1) |
| | Read @300MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 27/46 | mA | 1) |
| | Read @333MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 30/50 | mA | 1) |
| | Read @400MHz (x8/x16) ( -40 ℃ to 125 ℃) | | 35/59 | mA | 1) |
| $ISB_{EXT1}$ | Standby current (extended temp 1) | | 778 | μA | 2) |
| $ISB_{EXT2}$ | Standby current (extended temp 2) | | 409 | μA | 2) |
| $ISB_{STD}$ | Standby current (standard temp) | | 237 | μA | 2) |
| $ISB_{STDroom}$ | Standby current (room temp) | | 68 | μA | 2), 3), 4) |
| $ISB_{STDDPD}$ | Standby current (Deep Power Down -40 ℃ to 125 ℃) | | 11 | μA | 5) |

Note:

1) Current is only characterized.
2) Without CLK toggling. ISB will be higher if CLK is toggling.
3) 0.5x Refresh.
4) Typical mean $ISB_{STDROOM}$ 53uA.
5) Typical mean $ISB_{STDDPD}$ 3uA at 25℃.
6) Current is only guaranteed after 150ms into Half Sleep mode.

## 4.7 AC Characteristics

**Table 24- READ/WRITE Timing**

| | | BGA 1.8V Only | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 166MHz | | 200MHz | | 225MHz | | 250MHz | | 300MHz | | 333MHz | | 400MHz | | | |
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Unit | Notes |
| tCLK | CLK period | 6 | | 5 | | 4.4 | | 4 | | 3.3 | | 3 | | 2.5 | | ns | |
| tCH/tCL | Clock high/low width | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCLK | |
| tKHKL | CLK rise or fall time | | 1 | | 0.8 | | 0.7 | | 0.6 | | 0.5 | | 0.4 | | 0.3 | ns | |
| tCPH | CE# HIGH between subsequent burst operations | 22 | | 24 | | 26 | | 28 | | 30 | | 32 | | 35 | | ns | |
| tCEM | CE# low pulse width (excluding Half Sleep exit) | | 4 | | 4 | | 4 | | 4 | | 4 | | 4 | | 4 | µs | Standard temp |
| | | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | µs | Extended temp 2 |
| | | | 0.5 | | 0.5 | | 0.5 | | 0.5 | | 0.5 | | 0.5 | | 0.5 | µs | Extended temp 1 |
| tCEM | CE# low pulse width | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | tCLK | Min. 3 clocks |
| tCSP | CE# setup time to CLK rising edge | 2 | | 2 | | 2 | | 2 | | 1.5 | | 1.5 | | 1.5 | | ns | Note1 |
| tCHD | CE# hold time from CLK falling edge | 2 | | 2 | | 2 | | 2 | | 1.5 | | 1.5 | | 1.5 | | ns | Note1 |
| tSP | Setup time to active CLK edge | 0.6 | | 0.5 | | 0.45 | | 0.4 | | 0.3 | | 0.28 | | 0.26 | | ns | |
| tHD | Hold time from active CLK edge | 0.6 | | 0.5 | | 0.45 | | 0.4 | | 0.3 | | 0.28 | | 0.26 | | ns | Max. 0.75*tCLK |
| tHZ | Chip disable to DQ/DQS output high-Z | | 6.5 | | 6.5 | | 6.5 | | 6.5 | | 6.5 | | 6.5 | | 6.5 | ns | |
| tRC | Write Cycle | 60 | | 60 | | 60 | | 60 | | 60 | | 60 | | 60 | | ns | |
| tRC | Read Cycle | 60 | | 60 | | 60 | | 60 | | 60 | | 60 | | 60 | | ns | |
| tHS | Minimum Half Sleep duration | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | µs | |
| tXHS | Half Sleep Exit CE# low to CLK setup | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | µs | |
| tXPHS | Half Sleep Exit CE# low pulsewidth | 60 | | 60 | | 60 | | 60 | | 60 | | 60 | | 60 | | ns | |
| | | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | µs | Standard temp |
| | | | 0.5 | | 0.5 | | 0.5 | | 0.5 | | 0.5 | | 0.5 | | 0.5 | µs | Extended temp |
| tDPD | Minimum DPD duration | 500 | | 500 | | 500 | | 500 | | 500 | | 500 | | 500 | | µs | |
| tDPDp | Minimum period between DPD Modes | 500 | | 500 | | 500 | | 500 | | 500 | | 500 | | 500 | | µs | |
| tXDPD | DPD CE# low to CLK setup time | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | µs | |
| tXPDPD | DPD Exit CE# low pulsewidth | 60 | | 60 | | 60 | | 60 | | 60 | | 60 | | 60 | | ns | |
| tPU | Device Initialization | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | µs | |
| tRP | RESET# low pulse width | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | µs | |
| tRST | Reset to CMD valid | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | µs | |

Note1: It is strongly recommend to stop clock when CE_n is high;

If clock is togging when CE_n is high, the following conditions must be satisfied:

1). tCSP must be satisfied;

2). If tCHD could not be satisfied, the minimal value of tCHD=tCLK/2-tCSPmin should be guaranteed;

**Table 25– DDR Timing Parameters**

| | | BGA 1.8V Only | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 166MHz | | 200MHz | | 225MHz | | 250MHz | | 300MHz | | 333MHz | | 400MHz | | | |
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Unit | Notes |
| tCQLZ | Clock rising edge to DQS low | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | ns | |
| tDQSCK | DQS output access time from CLK | 2 | 5 | 2 | 5 | 2 | 5 | 2 | 5 | 2 | 5 | 2 | 5 | 2 | 5 | ns | |
| tDQSQ | DQS – DQ skew | | 0.5 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | ns | |
| tDS | DQ and DM input setup time | 0.6 | | 0.5 | | 0.45 | | 0.4 | | 0.3 | | 0.28 | | 0.26 | | ns | |
| tDH | DQ and DM input hold time | 0.6 | | 0.5 | | 0.45 | | 0.4 | | 0.3 | | 0.28 | | 0.26 | | ns | |
| tHP | Half Period | = min(tCH, tCL) | | | | | | | | | | | | | | ns | |
| tQHS | Datahold skew factor | | 0.6 | | 0.5 | | 0.45 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | ns | |
| tQH | DQ output hold time from DQS | = tHP - tQHS | | | | | | | | | | | | | | ns | |

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