Signetics

SCB68175
Bus Controller

Preliminary Specification

Microprocessor Products

DESCRIPTION

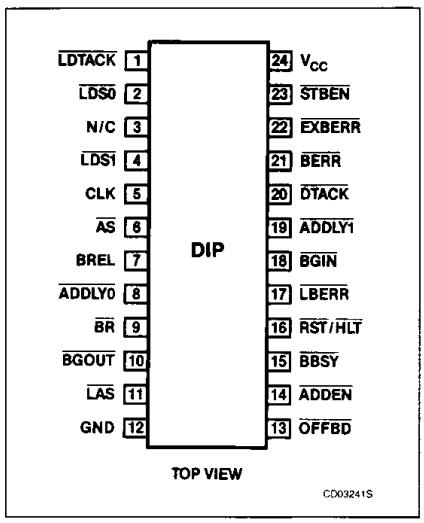
The Signetics SCB68175/8X821 Bus Controller is a high-speed bus requester and timing generator designed to interface a local master (typically, a microprocessor or DMA controller) to the VMEbus or VERSAbus™. The requester is fully asynchronous and controls all the sequencing required for acquisition and use of the bus, including both strobe and buffer timing. To permit fixed or variable length bus access, both release-when-done (RWD) and release-on-request (ROR) modes are supported by the SCB68175/8X821. In addition, an early bus-busy release increases system throughput by allowing bus arbitration to be performed concurrently with the final bus cycle of the local master. A bus error/retry circuit is also included in the SCB68175/8X821. This circuit allows the local master to rerun a cycle that was terminated by a bus error. Interface and control signals for a typical configuration are shown in Figure 1.

The SCB68175/8X821 Bus Controller is designed primarily for implementing a simple and efficient interface to the VMEbus. For more information regarding the protocol definitions, proper use, and application of this device, refer to the VMEbus Specification Manual.

FEATURES

- **Asynchronous bus controller for VMEbus and VERSAbus systems**
- **Provides transparent system interface to local master**
- **Supports both release-on-request (ROR) and release-when-done (RWD) operations**
- **Early bus-busy release for optimal bus usage**
- **Error/entry sequencing**
- **Dual port capability using 74LS764 DRAM controller**
- **High speed bipolar technology**
- **Single +5V supply**
- **24-pin slimline DIP package**

PIN CONFIGURATION



VERSAbus is a registered trademark of Motorola, Inc.

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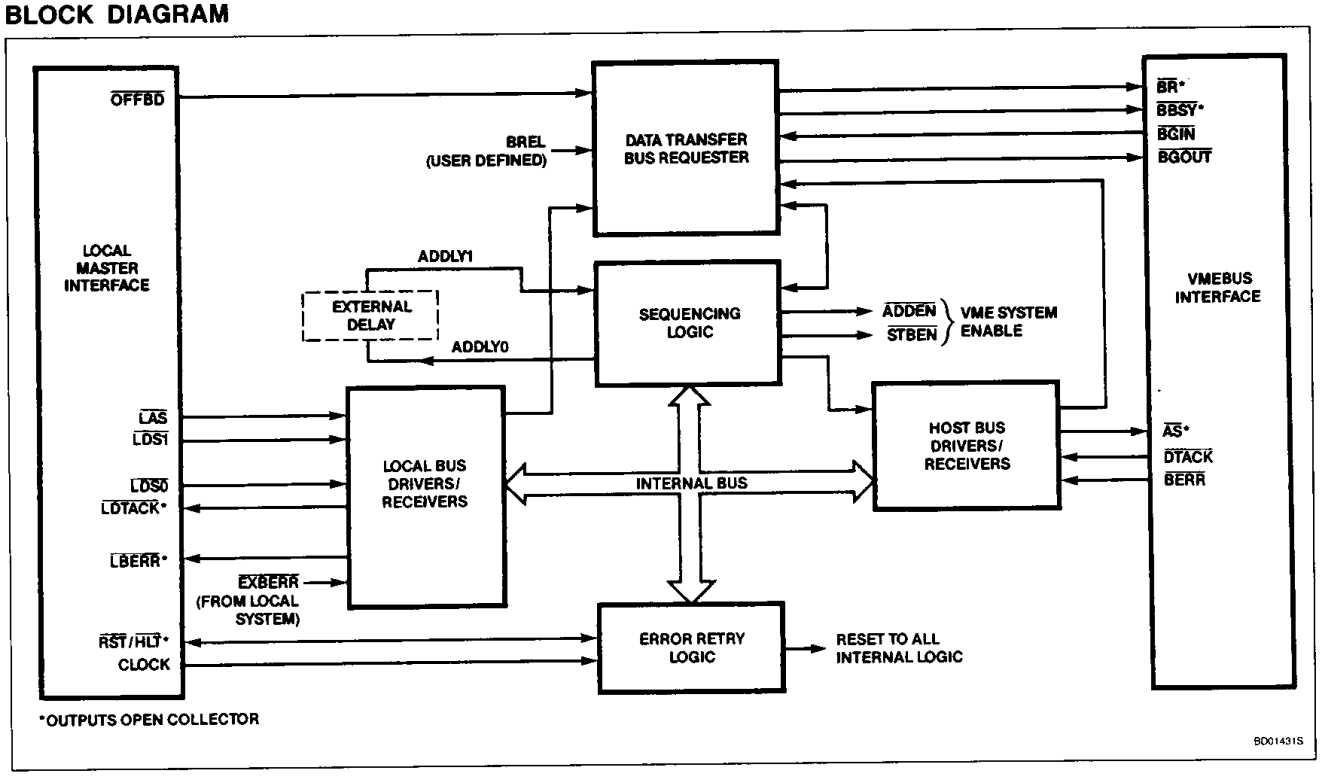
BLOCK DIAGRAM



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ORDERING CODE

PACKAGES	V_{CC} = 5V ± 5%, T_A = 0°C to 70°C
Ceramic DIP	SCB68175C2I24
Plastic DIP	SCB68175C2N24

PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
$\overline{LDTACK}$	1	O	**Local Data Transfer Acknowledge:** Active low, open collector. $\overline{LDTACK}$ is the acknowledge signal to the local master.
$\overline{LDS0}$	2	I	**Local Data Strobe 0:** Active low (hysteresis) input lower data strobe of the local master.
$\overline{LDS1}$	4	I	**Local Data Strobe 1:** Active low (hysteresis) input upper data strobe of the local master.
CLK	5	I	**Clock:** CLK is the clock input to the retry circuitry.
$\overline{AS}$	6	I/O	**Address Strobe:** Active low, open collector. $\overline{AS}$ is the address strobe of the system bus. As an output, $\overline{AS}$ is asserted to indicate a valid address on the system bus. As an input (hysteresis), $\overline{AS}$ is monitored during the bus acquisition phase to determine when the current master has relinquished control of the bus.
BREL	7	I	**Bus Release:** Active high input used to get the SCB68175/8X821 to release the system bus.
$\overline{ADDLYO}$	8	O	**Address Delay Out:** Active low, totem pole. $\overline{ADDLYO}$ is the output to an external delay line.
$\overline{BR}$	9	O	**Bus Request:** Active low, open collector. The bus request output to the system bus; asserted when the SCB68175/8X821 is not the current master and $\overline{LAS}$ and $\overline{OFFBD}$ are asserted.
$\overline{BGOUT}$	10	O	**Bus Grant Out:** Active low, totem pole. $\overline{BGOUT}$ is the daisy-chain output.
$\overline{LAS}$	11	I	**Local Address Strobe:** Active low $\overline{LAS}$ is the (hysteresis) input address strobe signal from the local master. If $\overline{OFFBD}$ and $\overline{LAS}$ are asserted low, the SCB68175/8X821 will initiate a bus cycle requesting the bus, if necessary.
GND	12	I	**Ground**
$\overline{OFFBD}$	13	I	**Off Board:** $\overline{OFFBD}$ is an active low select input driven by an address decoder to request access to the system bus. If $\overline{LAS}$ and $\overline{OFFBD}$ are asserted low, the SCB68175/8X821 will initiate a bus cycle requesting the bus, if necessary.
$\overline{ADDEN}$	14	O	**Address Enable:** Active low, totem pole. $\overline{ADDEN}$ is an enable signal to the address and data bus drivers/receivers.
$\overline{BBSY}$	15	O	**Bus Busy:** Active low, open collector. $\overline{BBSY}$ output is driven low when the local master has been granted the system bus.
$\overline{RST/HLT}$	16	I/O	**Reset/Halt:** Active low, open collector. (Hysteresis) input resets the SCB68175/8X821. As an output, it is asserted along with $\overline{LBERR}$ to initiate a rerun cycle upon receiving either $\overline{BERR}$ for a bus cycle, or $\overline{EXBERR}$ for a local cycle.
$\overline{LBERR}$	17	I/O	**Local Bus Error:** Active low, open collector. $\overline{LBERR}$ is the bus error signal to the local master.
$\overline{BGIN}$	18	I	**Bus Grant In:** Active low. $\overline{BGIN}$ is the daisy-chain input.
$\overline{ADDLYI}$	19	I	**Address Delay In:** Active low. Input from the external delay line.
$\overline{DTACK}$	20	I	**Data Transfer Acknowledge:** Active low. $\overline{DTACK}$ is the (hysteresis) input data transfer acknowledge signal of the system bus. During the bus acquisition phase, $\overline{DTACK}$ is monitored to determine when the current master has relinquished control of the bus.
$\overline{BERR}$	21	I	**Bus Error:** Active low. $\overline{BERR}$ is the (hysteresis) input bus error signal of the system bus. During the bus acquisition phase, $\overline{BERR}$ is monitored to determine when the current master has relinquished control of the bus.
$\overline{EXBERR}$	22	I	**External Bus Error:** Active low. $\overline{EXBERR}$ is a (hysteresis) input bus error signal from a local device.
$\overline{STBEN}$	23	O	**Strobe Enable:** Active low, totem pole. $\overline{STBEN}$ is an enable signal to the system bus data strobe drivers.
V_{CC}	24	I	**Supply Voltage:** +5V power supply.

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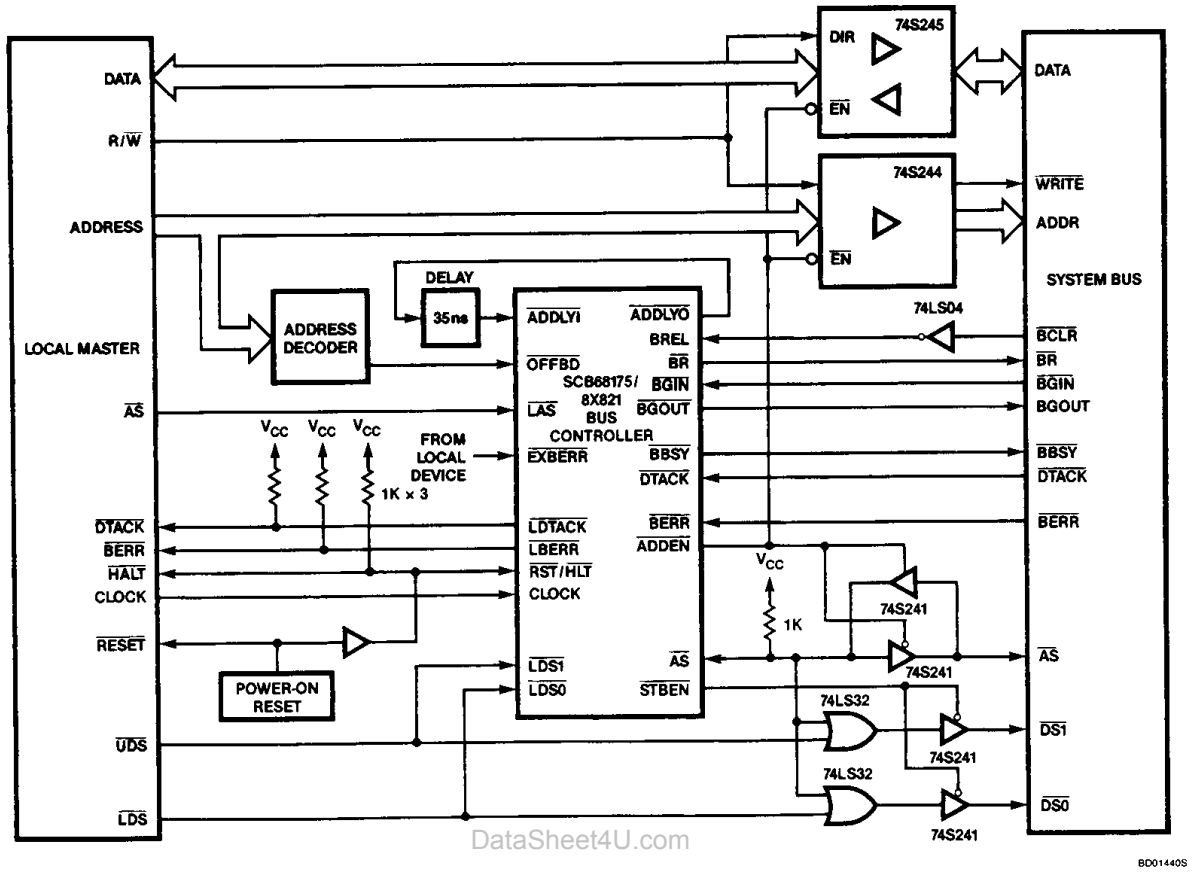

Figure 1. Typical System Configuration

FUNCTIONAL DESCRIPTION

Bus Acquisition

In a multimaster, bus oriented system, each master requires some method of gaining access to global resources such as, main memory, disk storage and I/O devices. A very precise access arbitration protocol is implemented (fully defined in the VMEbus Specification) and is basically:

1. Asserting a bus request.
2. Receiving a grant that the bus is available.
3. Acknowledging that mastership has been assumed.

Requesting the Bus

Local devices capable of becoming bus masters, for example, CPU and interrupt handler, request the system bus by asserting $\overline{OFFBD}$. This signal is typically the output from an address decoder indicating that the required resource (memory, I/O) is accessible only via the host bus. With both $\overline{OFFBD}$ and $\overline{LAS}$ low, the SCB68175/8X821 asserts the system bus request signal ($\overline{BR}$). In a VMEbus system, $\overline{BR}$ is tied to one of the four bus request signals ($\overline{BR0}$ – $\overline{BR3}$).

Receiving the Bus Grant

The BGIN/BGOUT signals comprise a daisy-chain network allowing multiple bus masters to share the same bus request level. The SCB68175/8X821 will assert $\overline{BGOUT}$ only if $\overline{BGIN}$ is received low prior to the assertion of a bus request ($\overline{BR}$). This allows the next master, in the daisy-chain, access to the bus. If $\overline{BR}$ precedes $\overline{BGIN}$, then the SCB68175/8X821 will assert $\overline{BBSY}$ and release $\overline{BR}$. This completes the bus request phase.

If $\overline{BGIN}$ precedes $\overline{BR}$, then $\overline{BR}$ remains asserted pending the next arbitration cycle. If a bus request and $\overline{BGIN}$ are asserted simultaneously, an onboard arbiter guarantees the outputs to remain stable until a random choice is made of either $\overline{BR}$ or $\overline{BGIN}$.

Bus Access

Actual bus access does not occur until the previous master has relinquished control of the bus. This is detected when the system signals $\overline{AS}$, $\overline{DTACK}$ and $\overline{BERR}$ are received high. The SCB68175/8X821 then controls the sequencing of the address, data and strobe signals required for each bus cycle.

Typical Bus Cycle

See Figure 2 for a typical bus access flowchart. For each bus access, the SCB68175/8X821 drives $\overline{ADDEN}$, $\overline{STBEN}$ and $\overline{AS}$ low. An external delay line (35ns minimum), when connected between $\overline{ADDLY0}$ and $\overline{ADDLY1}$, guarantees a minimum set-up time between the assertion of $\overline{ADDEN}$ and $\overline{AS}$.

In most cases, the local master will require multiple accesses to the host bus. To accommodate, the SCB68175/8X821 cycles $\overline{ADDEN}$, $\overline{STBEN}$ and $\overline{AS}$ for each bus access. For a local cycle (when the master asserts $\overline{LAS}$, but $\overline{OFFBD}$ is high), the SCB68175/8X821 holds $\overline{ADDEN}$, $\overline{STBEN}$ and $\overline{AS}$ high, and allows the master access to its local bus.

Read-Modify-Write Cycle

The SCB68175/8X821 also allows a read-modify-write access for system resources. A read-modify-write cycle is similar to a read cycle followed by a write cycle, except that $\overline{AS}$ is continuously driven low during both transfer cycles. However, unlike a read followed by a write, the read-modify-write cycle cannot be interrupted because $\overline{AS}$ is driven low continuously through both cycles, and

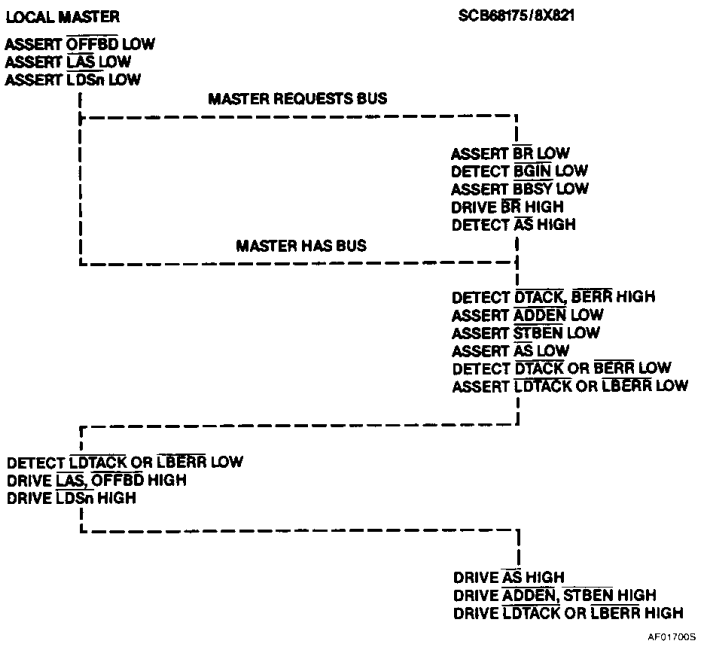

Figure 2. Typical Bus Cycle

control of the host bus may only be transferred while $\overline{AS}$ is high. The SCB68175/8X821 will cycle $\overline{STBEN}$ as required for a read-modify-write cycle.

Bus Release

Following initial bus acquisition, $\overline{BBSY}$ remains low for a minimum of 90ns, providing a 35ns delay line is connected between $\overline{ADDLY0}$ and $\overline{ADDLY1}$. If BREL is asserted high any time before the end of the current bus cycle, the SCB68175/8X821 will release $\overline{BBSY}$ allowing bus arbitration to take place. At the conclusion of the current bus cycle, the SCB68175/8X821 will release the bus by negating $\overline{ADDEN}$, $\overline{AS}$ and $\overline{STBEN}$. A subsequent offboard request will result in the start of a new bus acquisition cycle.

The bus release signal can be used to control the duration, that is the number of cycles the master will control the bus. For most simple masters, BREL can be tied high resulting in a single-cycle RWD configuration. In this case, the SCB68175/8X821 must request the bus for each and every bus cycle. A DMA controller might use the RWD mode, but would assert BREL only after performing a fixed number of cycles.

An ROR mode can be achieved by asserting BREL only when some other master is requesting bus access. Typically, this may be achieved by NANDing the appropriate $\overline{BR}$ lines together to assert BREL. BREL is not monitored by the SCB68175/8X821 until the last leading edge of either $\overline{BGIN}$ or $\overline{ADDLY1}$. This prevents the SCB68175/8X821 from relinquishing control due to its own bus request.

For improved system performance, BREL should be asserted early in the current cycle (that is, as soon as possible after $\overline{LAS}$ is asserted), to allow bus arbitration to be performed concurrently with the existing bus cycle.

Bus Error/Entry

The SCB68175/8X821 provides a bus error/entry facility which allows the local master to rerun its last cycle once, if the cycle was terminated by a bus error.

The bus error/entry sequence is initiated when a bus error is received instead of a (normal) data transfer acknowledge signal. Upon receipt of a bus error (either $\overline{BERR}$ for a bus cycle, or $\overline{EXBERR}$ for a local cycle), the SCB68175/8X821 asserts both $\overline{LBERR}$ AND $\overline{RST}/\overline{HLT}$. This will allow the local master to rerun the cycle.

The local master can then rerun the bus cycle using the same address, and the same data for a write. If this cycle is also terminated by a bus error, the SCB68175/8X821 will assert $\overline{LBERR}$ but not $\overline{RST}/\overline{HLT}$.

The $\overline{EXBERR}$ input is provided for local resources to initiate a retry sequence. Local devices may drive $\overline{LBERR}$ (an open collector output) directly to bypass the retry function.

Reset

The SCB68175/8X821 must be reset as specified in the reset timing in order to ensure proper operation. When $\overline{RST}/\overline{HLT}$ is asserted, the SCB68175/8X821 will drive all outputs high to release the bus. If the SCB68175/8X821 has control of the system bus and the local master fails, $\overline{RST}/\overline{HLT}$ should be asserted. This will ensure that the system bus is relinquished by the SCB68175/8X821 Bus Controller.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
Supply voltage	−0.5 to +7.0	V
Input voltage	−0.5 to +5.5	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5]

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Max	UNIT
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
V_{IC}	Input clamp diode voltage	$V_{CC} = 4.75V$, $I_{IN} = -18mA$		−1.5	V
I_{IL}	Input low current	$V_{CC} = 5.25V$, $V_{IN} = 0.4V$		−410	μA
I_{IH}	Input high current	$V_{CC} = 5.25V$, $V_{IN} = 2.7V$		20	μA
I_I	Input high current	$V_{CC} = 5.25V$, $V_{IN} = 5.5V$		100	μA
V_{OL}	Output low voltage	$V_{CC} = 4.75V$			
	$\overline{LDTACK}$, $\overline{ADDLYO}$, $\overline{BGOUT}$, $\overline{ADDEN}$, $\overline{RST}/\overline{HLT}$, $\overline{LBERR}$, $\overline{DTACK}$	$I_{OL} = 8mA$		0.5	V
	$\overline{AS}$	$I_{OL} = 20mA$		0.5	V
	$\overline{BR}$, $\overline{BBSY}$	$I_{OL} = 64mA$		0.5	V
V_{OH}	Output high voltage				
	$\overline{ADDLYO}$, $\overline{BGOUT}$, $\overline{ADDEN}$, $\overline{STBEN}$	$V_{CC} = 4.75V$, $I_{OH} = -400\mu A$	2.5		V
I_{CEX}	Open collector leakage current				
	$\overline{LDTACK}$, $\overline{AS}$, $\overline{RST}/\overline{HLT}$, $\overline{LBERR}$	$V_{CC} = 4.75V$, $V_{OUT} = 5.25V$		100	μA
I_{OS}	Short circuit output current				
	$\overline{ADDLYO}$, $\overline{BGOUT}$, $\overline{ADDEN}$, $\overline{STBEN}$	$V_{CC} = 5.25V$, $V_{OUT} = 0V$[6]	−15	−100	mA
I_{CC}	Supply current	$V_{CC} = 5.25V$		140	mA

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient for ceramic package (116°C/W for plastic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 3ns maximum and output voltages are checked at 0.8V and 2.0V.
6. At any time, no more than one output should be connected to ground.
7. If the asynchronous input requirement (t_{BG}) is not satisfied, then $\overline{BGOUT}$ will be asserted low for the duration of $\overline{BGIN}$ low.
8. Requires minumum 35ns delay line connected between $\overline{ADDLYO}$ and $\overline{ADDLYI}$.
9. If the asynchronous input requirement (t_{BRLS}) is not satisfied, then $\overline{BBSY}$ will be negated (driven high) on the following assertion of $\overline{LAS}$.
10. Valid only for system bus cycles not involving bus acquisition.
11. BREL is a don't care until the leading edge of either $\overline{ADDLYI}$ or $\overline{BGIN}$, whichever occurs last. If $\overline{ADDLYI}$ occurs last, then t_{DIS} is valid. If $\overline{BGIN}$ occurs last, then t_{BGS} is valid. If they occur simultaneously, then t_{DIS} is valid.
12. Valid only with 35ns external delay line and if t_{BBY} (minimum) has been met.
13. Valid from last leading edge of either $\overline{DTACK}/\overline{BERR}$ or $\overline{AS}$.
14. Only one of t_{REQ1}, t_{REQ2} is valid at once. If the falling edge of $\overline{OFFBD}$ occurs after the falling edge of $\overline{LAS}$, then t_{REQ1} is valid. If the falling edge of $\overline{LAS}$ occurs after the falling edge of $\overline{OFFBD}$, then t_{REQ2} is valid. If both $\overline{LAS}$ and $\overline{OFFBD}$ occur simultaneously, then t_{REQ2} is valid.
15. Only one of t_{ADN1}, t_{ADN2} is valid at once. If the falling edge of $\overline{OFFBD}$ occurs after the falling edge of $\overline{LAS}$, then t_{ADN1} is valid. If the falling edge of $\overline{LAS}$ occurs after the falling edge of $\overline{OFFBD}$, then t_{ADN2} is valid. If both $\overline{LAS}$ and $\overline{OFFBD}$ occur simultaneously, then t_{ADN2} is valid.
16. The SCB68175/8X821 must see two falling edges of the clock after the rising edge of $\overline{BERR}/\overline{EXBERR}$ before t_{GO} is valid.
17. Valid only if no bus request is pending.
18. The SCB68175/8X821 will only assert $\overline{LDTACK}/\overline{LBERR}$ with the high-to-low transition of $\overline{DTACK}/\overline{BERR}$. When running consecutive bus cycles, the SCB68175/8X821 will then ensure that any slow or lazy $\overline{DTACK}/\overline{BERR}$ terminating the first cycle is not transmitted through to the local master interface.
19. These parameters are guaranteed at the values listed; these values were determined either by system bench testing or by Signetics' characterization procedures. All other tabular entries are taken directly from simulation results run at a range of operational frequencies; these values are not tested or guaranteed.

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5]

PARAMETER		LIMITS		UNIT
		Min	Max	
Read/write (see figure 3)				
t_{REQ1}[14]	$\overline{OFFBD}$ low to $\overline{BR}$ low		56	ns
t_{REQ2}[14]	$\overline{LAS}$ low to $\overline{BR}$ low		56	ns
t_{BG}[7]	$\overline{BR}$ low to $\overline{BGIN}$ low set-up	0		ns
t_{BGAK}	$\overline{BGIN}$ low to $\overline{BBSY}$ low		32	ns
t_{BBY}[8]	$\overline{BBSY}$ asserted width	90		ns
t_{ASEN}[13]	$\overline{AS}$, $\overline{DTACK}$, $\overline{BERR}$ high to $\overline{ADDEN}$ low		39	ns
t_{DIST}	$\overline{ADDLYI}$ low to $\overline{STBEN}$ Low		23	ns
t_{STAS}	$\overline{STBEN}$ low to $\overline{AS}$ low		14	ns
t_{BRLS}[9]	BREL high to $\overline{LAS}$ high set-up time	0		ns
t_{ADN1}[10, 15, 19]	$\overline{OFFBD}$ low to $\overline{ADDEN}$ low		37	ns
t_{ADN2}[10, 15]	$\overline{LAS}$ low to $\overline{ADDEN}$ low		35	ns
t_{OBDH}	$\overline{LAS}$ high to $\overline{OFFBD}$ high hold time	0		ns
t_{BLBY}[12]	BREL high to $\overline{BBSY}$ high		65	ns
t_{DYEN}	$\overline{ADDLYO}$ low to $\overline{ADDEN}$ low		10	ns
t_{DIDO}	$\overline{ADDLYI}$ to $\overline{ADDLYO}$		29	ns
t_{DLY}	$\overline{ADDLYO}$ high/low to $\overline{ADDLYI}$ high/low (minimum delay line)	35		ns
t_{LAS}[19]	$\overline{LAS}$ high to $\overline{AS}$ high		11	ns
t_{LSEN}	$\overline{LAS}$ high to $\overline{ADDEN}$ high		25	ns
t_{LSST}	$\overline{LAS}$ high to $\overline{STBEN}$ high		25	ns
t_{BGS}[11]	BREL high to $\overline{BGIN}$ high set-up	0		ns
t_{DIS}[11]	BREL high to $\overline{ADDLYI}$ high set-up	0		ns
t_{DIAS}	$\overline{ADDLYI}$ low to $\overline{AS}$ low		37	ns
t_{ASST}[19]	$\overline{AS}$ high to $\overline{STBEN}$ high		14	ns
t_{ASD}[19]	$\overline{AS}$ high to $\overline{ADDEN}$ high		14	ns
t_{ASDT}	$\overline{AS}$ high to $\overline{DTACK}$ high	0		ns
t_{CYED}	$\overline{LAS}$ high to $\overline{LDTACK}$/$\overline{LBERR}$ high		45	ns
t_{LSLD}	$\overline{LAS}$ high to $\overline{LDSn}$ high	0		ns
t_{BGL}[17]	$\overline{BGIN}$ low to $\overline{BGOUT}$ low		57	ns
t_{BGH}[17]	$\overline{BGIN}$ high to $\overline{BGOUT}$ high		57	ns
t_{LDS}	$\overline{LAS}$ low to $\overline{LDSn}$ low	0		ns
t_{LDSO}[10]	$\overline{LAS}$ low to $\overline{ADDLYO}$ low		26	ns
t_{OFDO}[10]	$\overline{OFFBD}$ low to $\overline{ADDLYO}$ low		26	ns
t_{ASDO}[13]	$\overline{AS}$, $\overline{DTACK}$, $\overline{BERR}$ high to $\overline{ADDLYO}$ low		38	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		LIMITS		UNIT
		Min	Max	
Read-modify-write (see figure 4)				
t_{PDL}[18]	$\overline{DTACK}/\overline{BERR}$ low time, $\overline{LDTACK}/\overline{LBERR}$ low propagation delay		28	ns
t_{CYEN}	Local data strobe 0 and 1 high to $\overline{LDTACK}/\overline{LBERR}$ high		45	ns
t_{LDAS}	$\overline{LDTACK}/\overline{LBERR}$ low to $\overline{LAS}$ high	0		ns
t_{LDST}	Local data strobe 0 and 1 high to $\overline{STBEN}$ high		32	ns
t_{DTST}	$\overline{DTACK}/\overline{BERR}$ high to $\overline{STBEN}$		38	ns
t_{LDLN}	$\overline{LDTACK}/\overline{LBERR}$ low to local data strobe 0 or 1 high	0		ns
Bus error/retry and reset (see figures 5, 6 and 7)				
t_{RST}	$\overline{RST}$ low time		$3t_{CKPD}$	ns
t_{CKH}	Clock high time	20		ns
t_{CKPD}	Clock period	40		ns
t_{PDL2}	$\overline{BERR}/\overline{EXBERR}$ low to $\overline{LBERR}$ low propagation delay		28	ns
t_{PDH2}	$\overline{BERR}/\overline{EXBERR}$ high/to $\overline{LBERR}$ propagation delay		12	ns
t_{ERR}	$\overline{LBERR}$ low to $\overline{RST}/\overline{HLT}$ low		16	ns
t_{GO}[16]	Clock to $\overline{RST}/\overline{HLT}$ high		38	ns

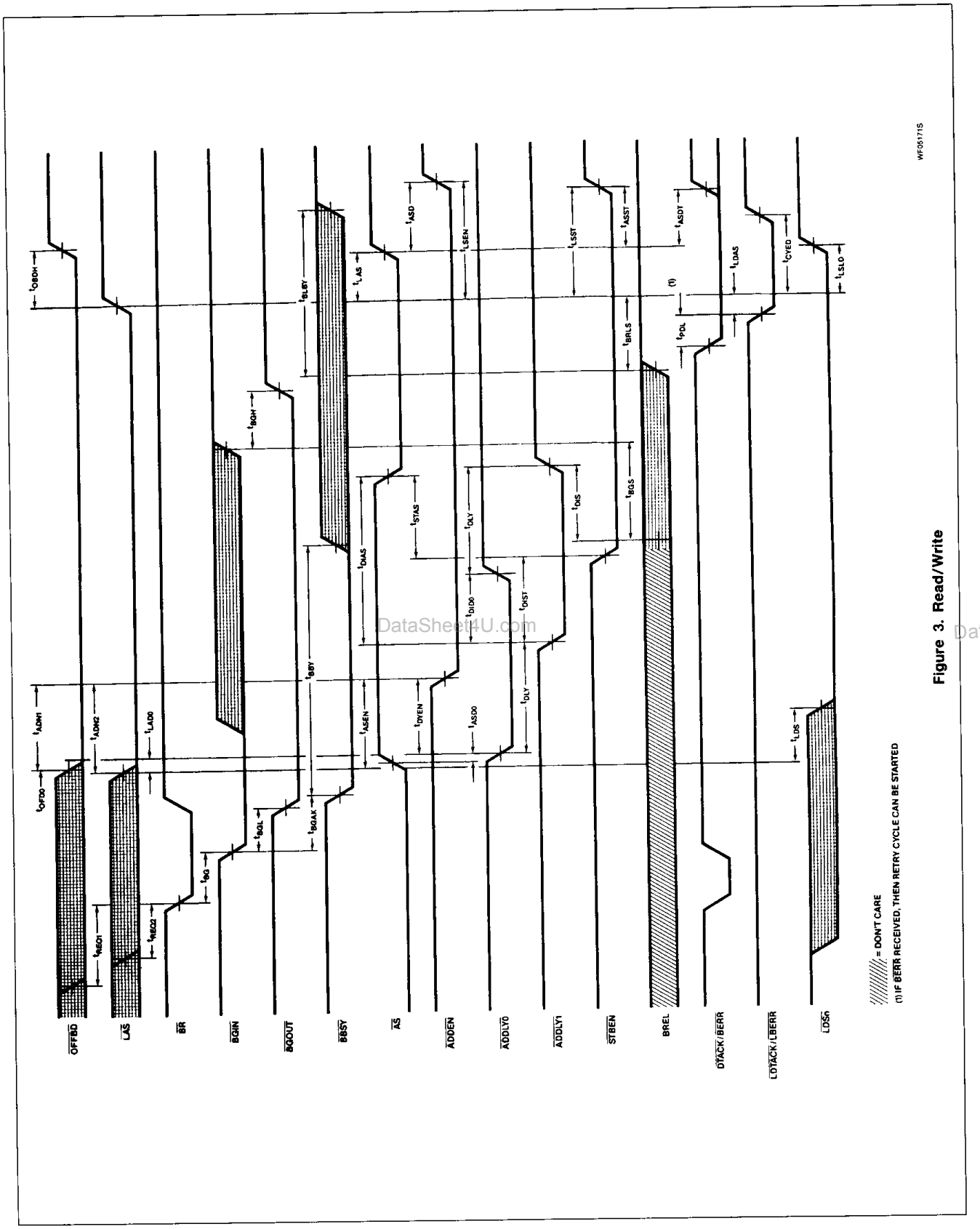

Figure 3. Read/Write

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Figure 4. Read/Modify/Write

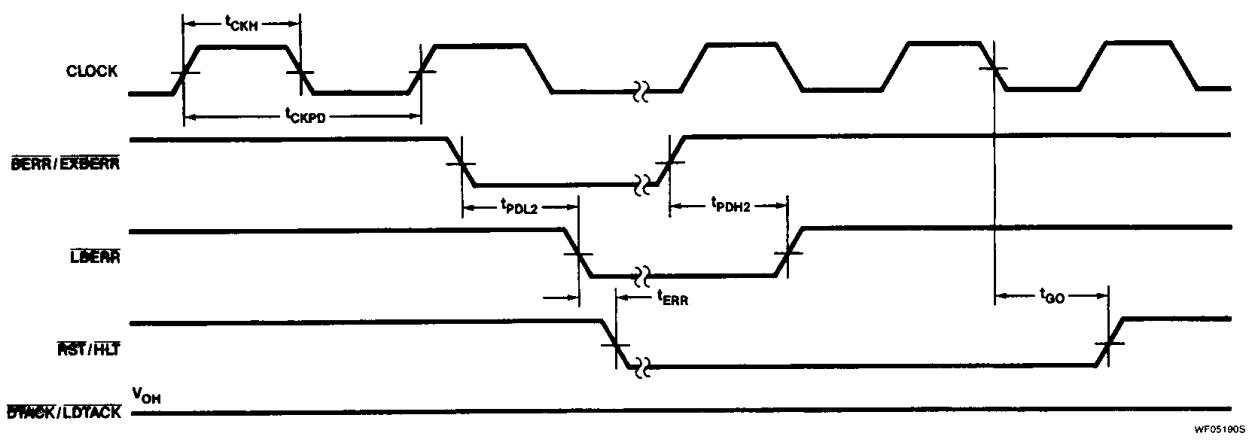

Figure 5. Bus Error/Retry (Last Cycle not Terminated by Error)

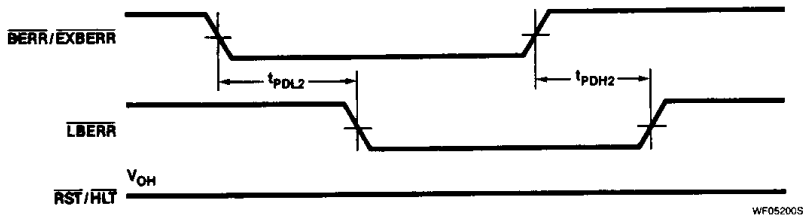

Figure 6. Bus Error/Retry (Last Cycle Terminated by Error)

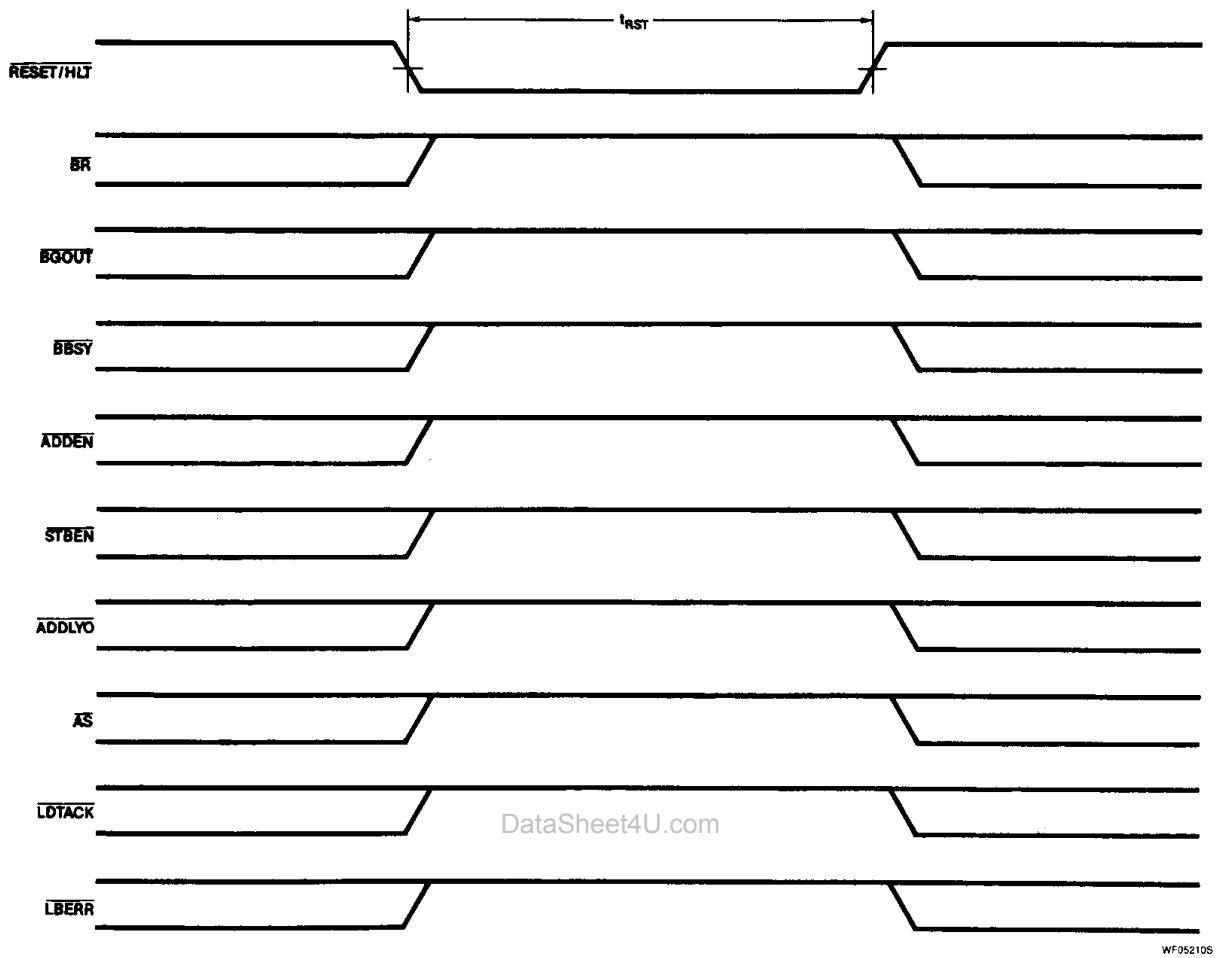

Figure 7. Reset