SCG2540 Synchronous Clock Generators

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

General Description

The SCG2540 is a mixed-signal phase lock loop generating CMOS outputs from an intrinsically low jitter voltage controlled crystal oscillator.

The SCG2540 can lock to one of two possible input reference frequencies at 10 kHz which is selectable using one input select pin.

Further features include an alarm output to indicate Loss of Reference, LOR, or Loss of Lock, LOL. If only one of the references is lost, the unit will disable its phase detector and will signal an alarm, but will not switch reference automatically. If both references are lost, the SCG2540 will enter a Free Run state which will guarantee a 20 ppm accurate output. Additionally, the Free Run mode may be entered manually by applying a high signal to the Force Free Run pin. If the unit is in Free Run mode, the Free Run status pin will be high.

All outputs, except the Oscillator Output, may be put into the tri-state high impedance condition for external testing purposes by applying a high signal to the Reset/ Tri-State pin.

The filtered 10 kHz is derived from the oscillator output. The offset between the filtered output and the reference input will change with each reference rearrangement.

The package maximum dimensions are .780” x .830” x .35” on a six layer FR4 board with surface mount pins. Parts are assembled using high temperature solder to withstand surface mount reflow process.

Features

- Phase Locked Output Frequency Control
- Intrinsically Low Jitter, Crystal Oscillator Derived Output
- Two Selectable References @ 10 kHz
- Alarm Output
- Tri-State Alarm Outputs and Reference Output
- Force Free Run Function
- Automatic Free Run Operation upon loss of both references
- Input Duty Cycle Tolerant
- 3.3 Volt Power Supply
- Small Size: 0.78” x 0.83” x 0.35” maximum
- Surface Mount, DIL Package

US Headquarters:
630-851-4722
European Headquarters:
+353-61-472221

Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{CC}	Power Supply Voltage	-0.5	-	+4.0	Volts	
V_I	Input Voltage	-0.5	-	+5.5	Volts	
T_S	Storage Temperature	-65.0	-	+150.0	°C	

Operating Specifications

Table 2

Parameter	Specifications	Notes
Voltage	3.3V ±5%	1.0
Current	100 mA Typical	
Oscillator Output Frequencies	20.48 MHz	
Temperature Range	0 to 70°C	
Input Frequency Ref 1 and Ref 2	10 kHz	2.0
Input Jitter Tolerance *(Jitter Frequencies ≥ 10 Hz)*	≥ 1µs Typical	
Jitter Bandwidth	< 10 Hz	
Typical Acquisition Time Data		
Acquisition from a cold power-up: Phase lock settled: Alarm time: Acquisition from Free Run: Phase lock settled: Alarm time: Frequency lock with a 20PPM reference frequency step: Typically 0.5s. Phase lock during a switch between equal frequency references: Typically 0.5s, no alarm should be issued	 30 - 60s <1.0s Typical 30 - 60s <1.0s Typical	
Capture/Pull-In Range	± 25 ppm Minimum	
Output Duty Cycle	40/60 % Min/Max @ 50% Level	
Output Rise and Fall Time	3 nS @ 20% to 80% output level	
Output Load	30 pF	
Alarm	LOR/LOL Status Signal Output	
Free Run Accuracy	±20 ppm	
Package	Fr4 SM 0.78” x 0.83” x 0.350” (Maximum)	
MTIE @ Synchronization Rearrangement	GR-253-CORE, 1999 R5-136	3.0, 4.0

Input and Output Characteristics

Table 3

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{IH}	High level input voltage	2.0	-	5.5	V	
V_{IL}	Low level input voltage	0	-	0.8	V	
T_{IO}	I/O to output valid	-	-	10	nS	
C_{OUT}	Output capacitance	-	-	10	pF	
V_{HO}	High level output voltage Ioh = -4mA	2.40	-	-	-	Vcc Min
V_{IO}	Low Level output voltage Io1 = 8mA	-	-	0.4	-	Vcc Max
T_{IR}	Input reference signal pulse width	30	-	-	nS	

Output Jitter Specifications

Table 4

Frequency (MHz)	Jitter BW 10 Hz - 1 MHz pS (RMS)	m UI	SONET Jitter BW 12 kHz - 20 MHz pS (RMS)	m UI
20.48	10 Typ.	0.205 Typ.	1 Max., 0.5 Typ.	0.020 Max.

Input Selection / Output Response

Table 5

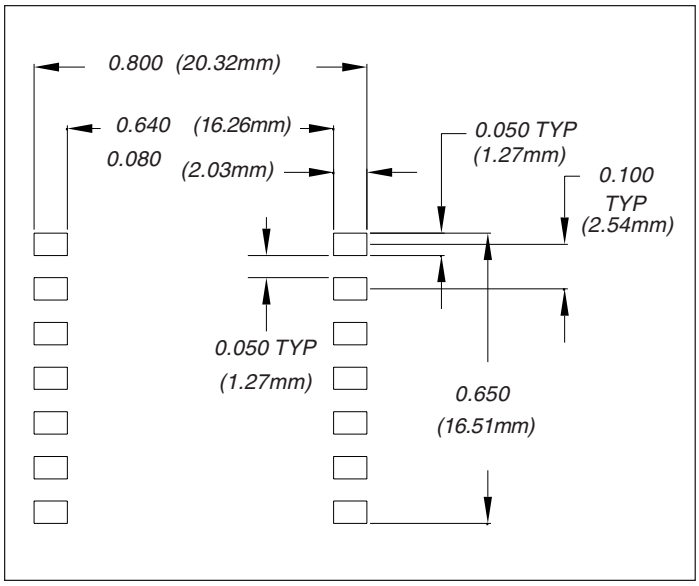
INPUTS					OUPUTS				
Reset/ Tri-State	SEL_{AB}	REF_A	REF_B	FR	FR_{status}	Alarm	Oscillator Output	10 kHz Output	Notes
1	X	X	X	X	TS	TS	FR	TS	
0	X	X	X	1	1	1	FR	FR	
0	0	A	A	0	0	0	LRA	LRAD	
0	1	NA	A	0	0	0	LRB	LRBD	
0	0	NA	A	0	0	1	U	U	5.0
0	1	A	NA	0	0	1	U	U	5.0
0	0	A	NA	0	0	0	LRA	LRAD	
0	X	NA	NA	0	1	1	FR	FR	

A = Active
TS = Tri-State
FR = Free Run
LRA = Locked to Ref A
LRB = Locked to Reb B
NA = Not Active or Not Present
U = Unstable
LRAD = Locked to Ref A and divided down
LRAB = Locked to ref B and divided down
X = Don't care

NOTES:
1.0 Requires external regulation
2.0 Externally selectable via Input Select AB
3.0 Entry into Free Run doesn't meet requirement for initial 2.33 seconds of self-timing
4.0 If the selected reference is removed, system response to the ALARM must be less than 100ns
5.0 On alarm assertion, switch references. If alarm is still active, force Free Run

Circuit Board Footprint

Figure 1



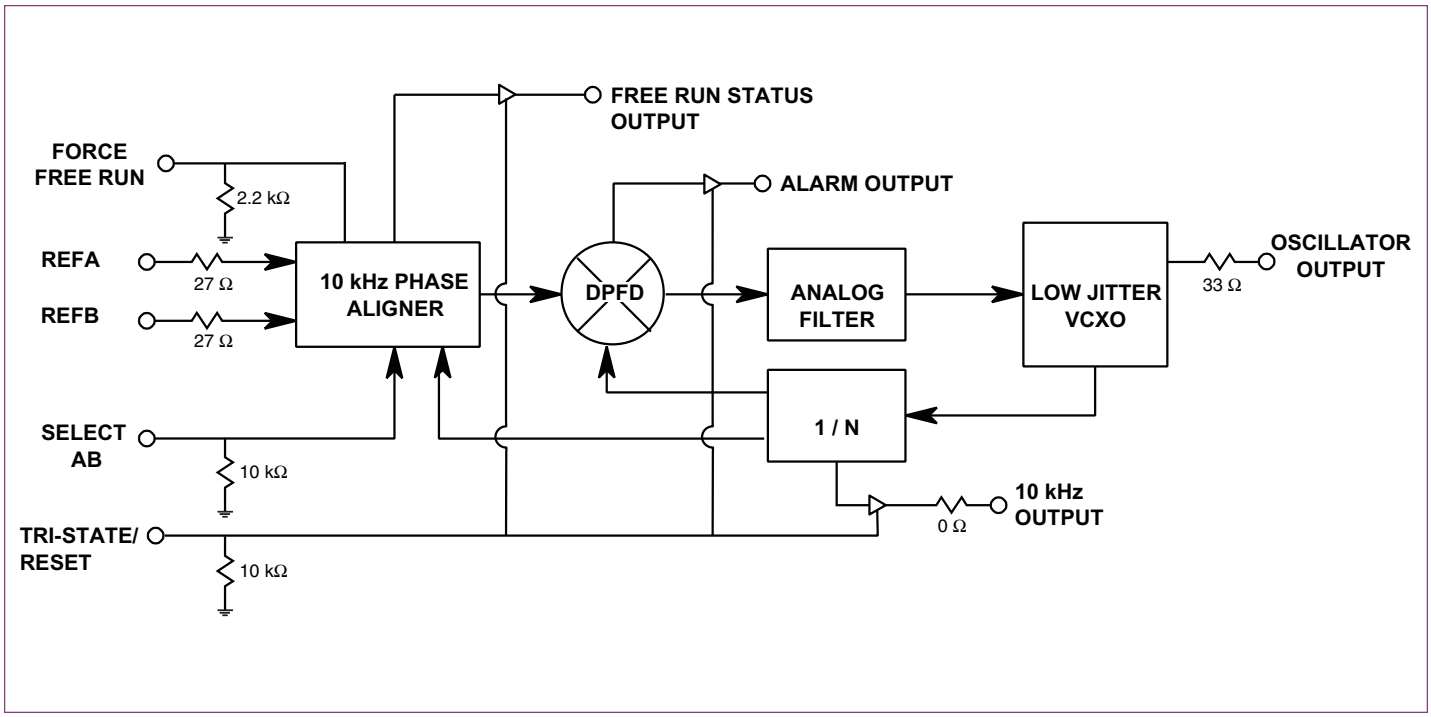
Pin Connections

Table 6

Pin	Connection
1	Filtered 10 kHz Output
2	TCK
3	TMS
4	Ground
5	Force Free Run / TDI (1 = Free Run)
6	Alarm Output (1 = Alarm)
7	REF B
8	REF A
9	Oscillator Output
10	Free Run Status Output (FR = 1)
11	Vcc
12	TDO
13	Reset / Tri-State
14	Input Reference Select AB (A = 0, B = 1)

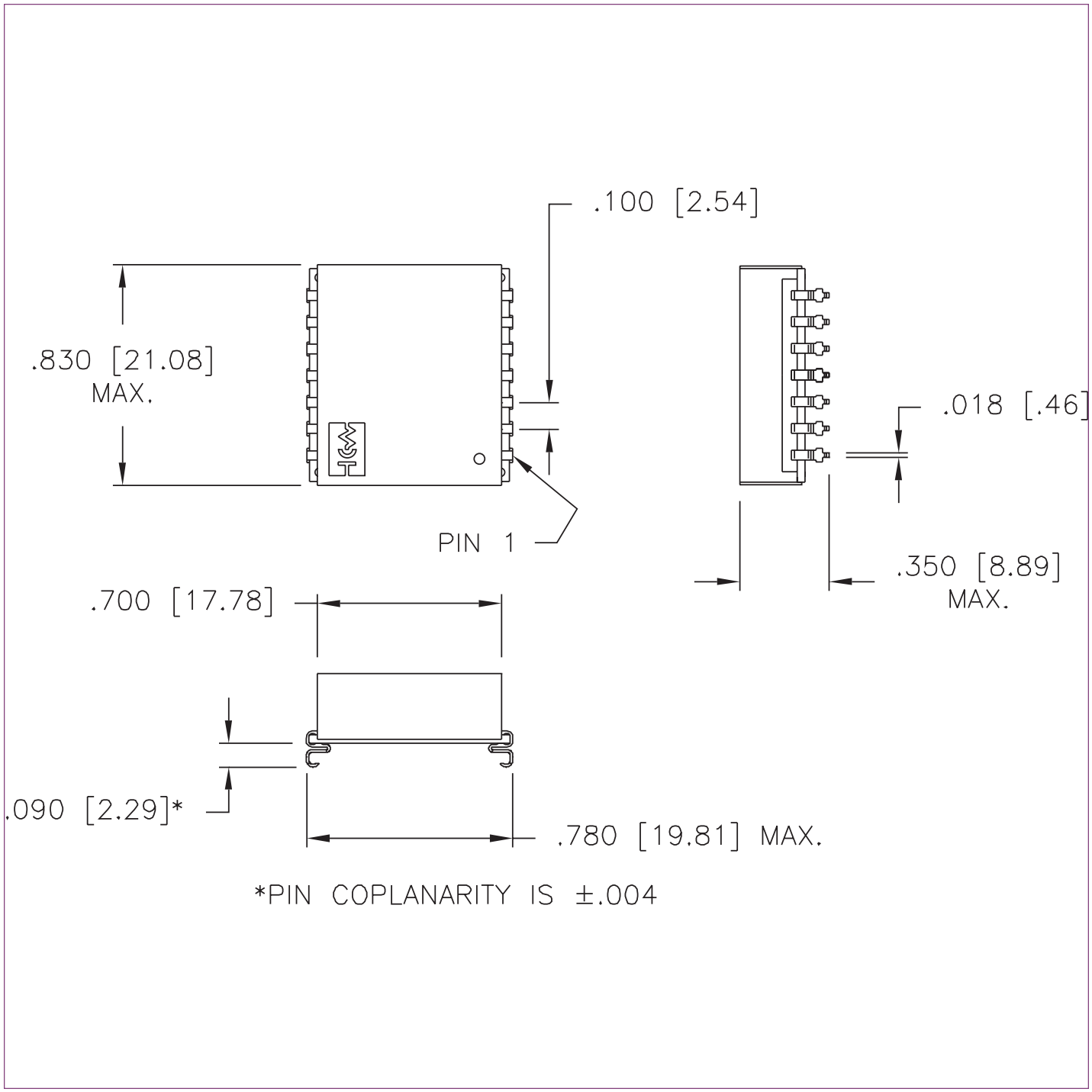
Block Diagram

Figure 2



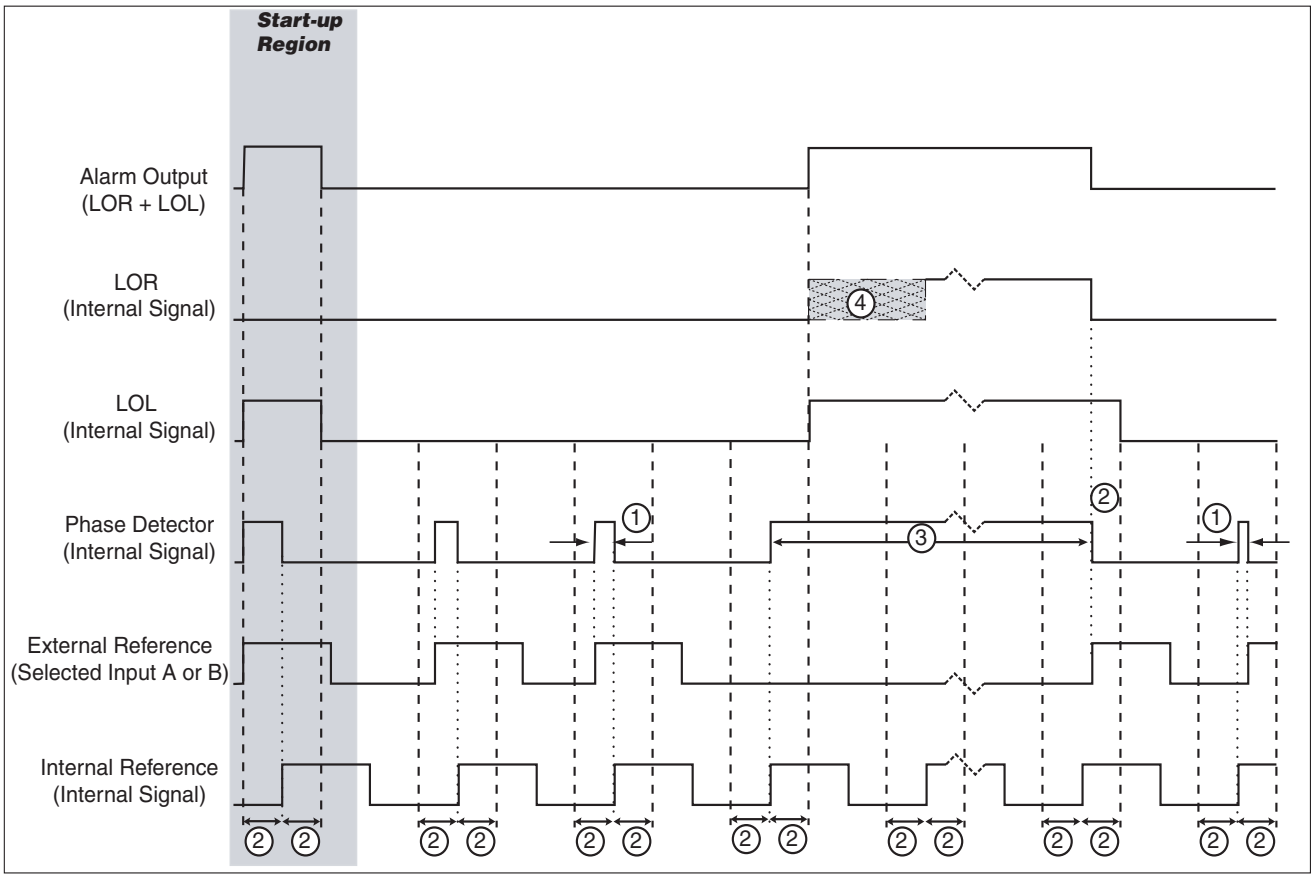
Package Maximum Dimensions

Figure 3



Loss of Reference Condition Alarm Timing

Figure 4



AlarmTiming Legend

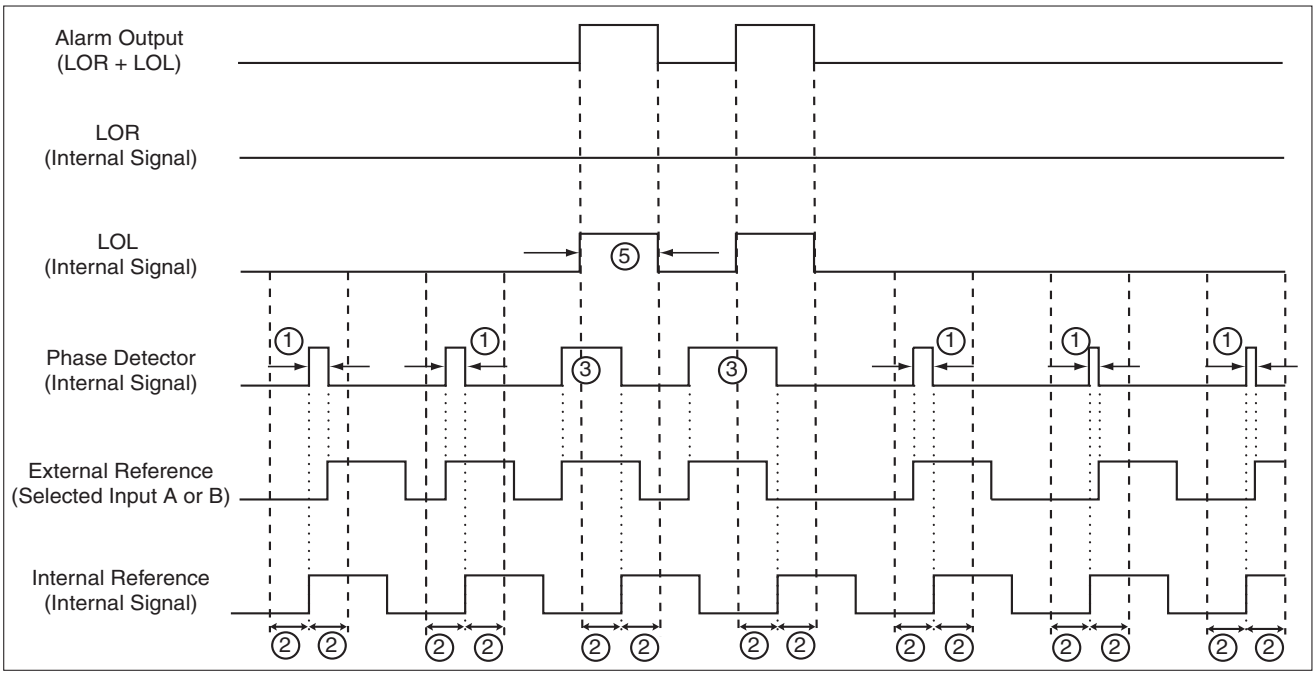
Use for all alarm timing diagrams

Table 7

	10 kHz Input Reference
1	< 1.0 µsec
2	1.0 µsec
3	> 1.0 µsec
4	100 Min to 300 Max µsec wide range
5	Minimum pulse width = 2 µsec
Start-up Region	During Start-up, The LOL Alarm will pulse during the first few seconds of operation.

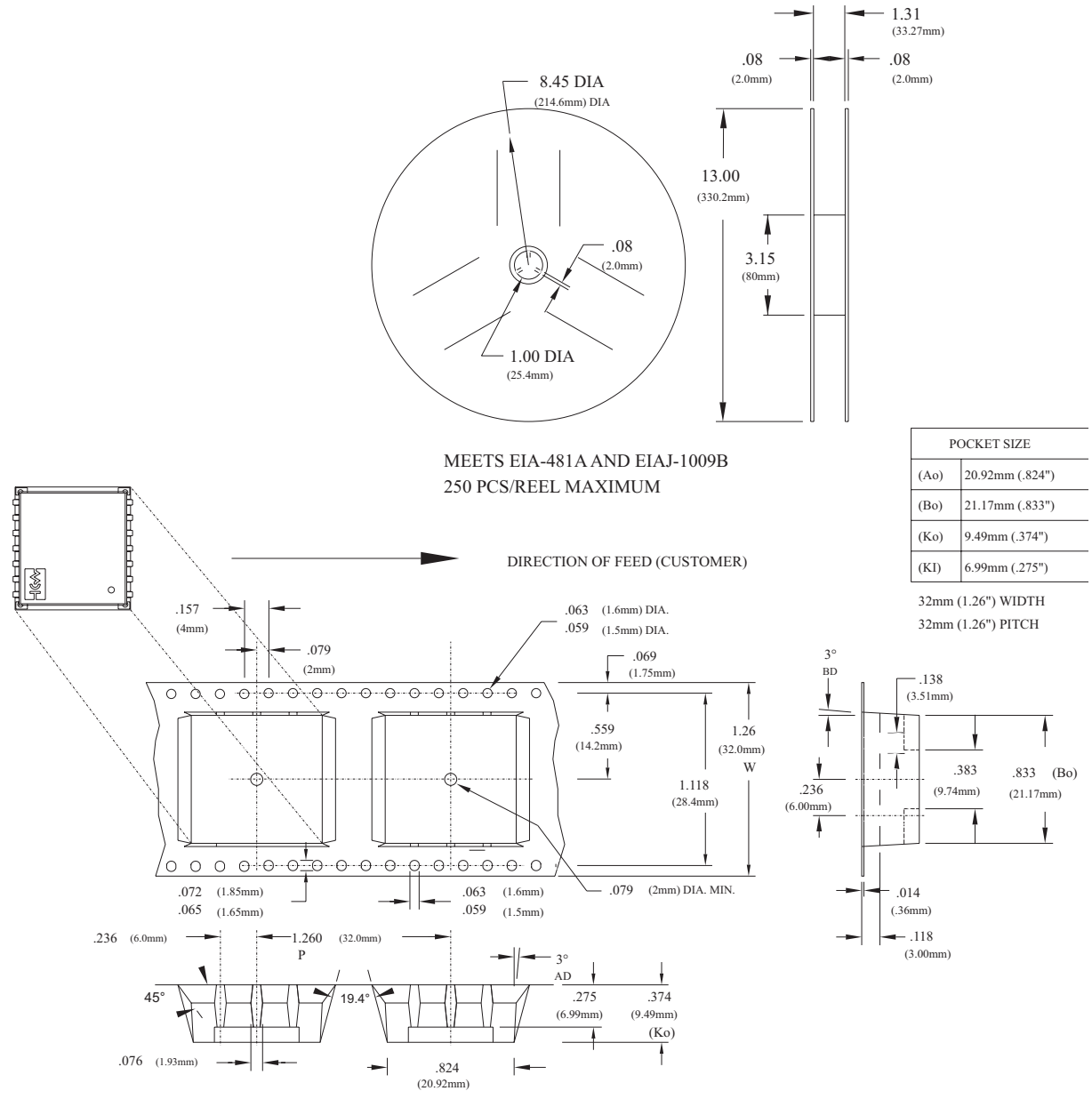
Loss of Lock Condition Alarm Timing

Figure 5



Tape and Reel Packaging

Figure 6

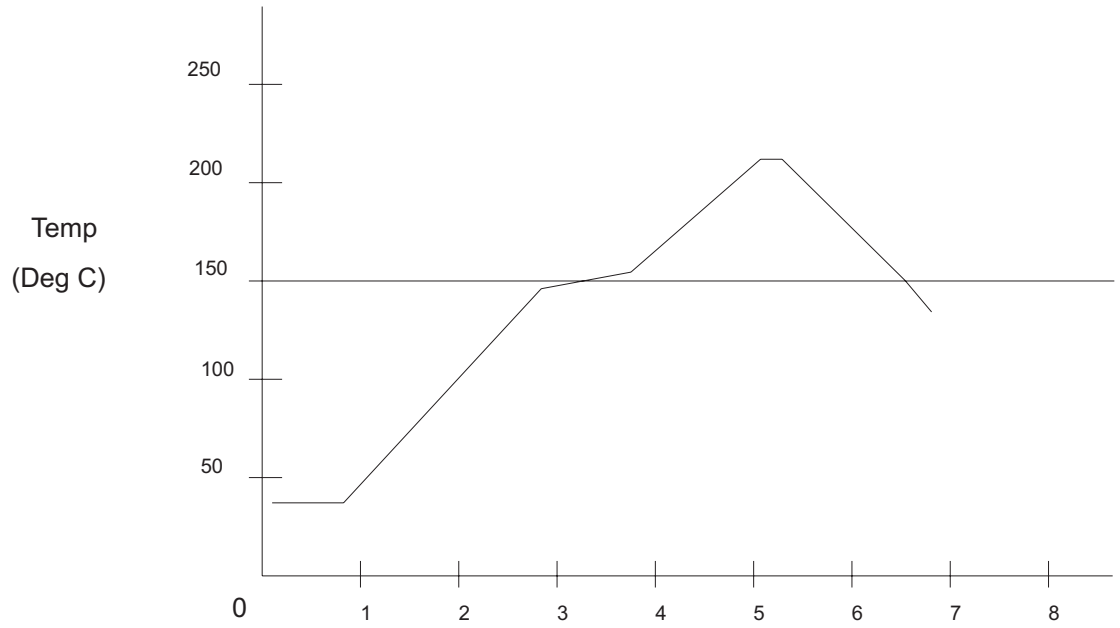


POCKET SIZE	
(Ao)	20.92mm (.824")
(Bo)	21.17mm (.833")
(Ko)	9.49mm (.374")
(KI)	6.99mm (.275")

32mm (1.26") WIDTH
32mm (1.26") PITCH

Solder Profile

Figure 7



Recommended Reflow Profile

Peak Temp:	217 Deg C
Max Rise Slope:	1.5 Deg C/Sec
Time Above 150 C:	100 Sec

Ordering Information

SCG{XXXX}-{FFF.FFF}{M}

XXXX equals a specific model (2540)
FFF.FFF equals the Oscillator Output frequency (020.48)
M equals MHZ and is added to all part numbers

Example: To order an SCG2540 with an Oscillator Output of 20.48 MHz,
Order part number SCG2540-020.48M

Please contact Connor-Winfield for other frequencies that may be available.

Model Comparison Table

Table 1

Model	Input Ref Freq	Max Duty Cycle	Reference Output	Oscillator Output (Synchronized Output)	Notes
SCG2500	2@8kHz	40/60	8 kHz	1.544 MHz - 77.76 MHz	
SCG2520	2@19.44 MHz	40/60	19.44 MHz	19.44 MHz	
SCG2540	2@10 kHz	40/60	10 kHz	20.48 MHz	
SCG2550	2@8 kHz	40/60	19.44 MHz	19.44 - 77.76 MHz	
SCG2560	2@25 MHz	45/55	25 MHz	125 MHz	

Other low jitter line card solutions from Connor-Winfield

SCG51 Series	Single input, jitter filtered with Free Run, 1 CMOS and 3 LVPECL outputs up to 622.08 MHz.
SCG102A/104A	Single input, frequency selectable, LVPECL clock smoothers from 77.76 to 777.76 MHz.
SCG2000 Series	Single input, jitter filtered with 20ppm Free Run, CMOS outputs from 8 kHz to 125.0 MHz.
SCG3000 Series	Single input, jitter filtered with Dual LVPECL outputs.
SCG4000 Series	Single input, jitter filtered with 20ppm Free Run, LVPECL outputs from 77.76 MHz to 180 MHz.
SCG4500 Series	Dual input, jitter filtered with Free Run, 1 LVPECL differential pair output up to 622.08 MHz.
SCG4600 Series	Dual input, jitter filtered with Free Run, 1 CML differential pair output up to 622.08 MHz.

Revision	Revision Date	Note
P00	5/16/02	Preliminary Product Release
P01	11/11/03	Revised Typ. Acquisition Time in Tbl. 2