Ordering number : ENN7532

P-Channel Silicon MOSFET

SCH1302

Ultrahigh-Speed Switching Applications

Features

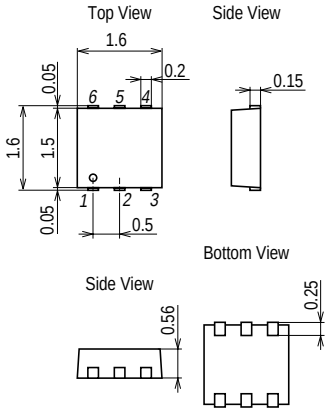
- Low ON-resistance.
- Ultrahigh-speed switching.
- 1.8V drive.

Package Dimensions

unit : mm

2221

[SCH1302]



1 : Drain
2 : Drain
3 : Gate
4 : Source
5 : Drain
6 : Drain

SANYO : SCH6

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		−20	V
Gate-to-Source Voltage	V_{GSS}		±10	V
Drain Current (DC)	I_D		−2	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	−8	A
Allowable Power Dissipation	P_D	Mounted on a ceramic board (900mm²×0.8mm)	0.8	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=-1mA, V_{GS}=0	−20			V
Zero-Gate Voltage Drain Current	$I_{DSS}1$	V_{DS}=-20V, V_{GS}=0			−10	μA
	$I_{DSS}2$	V_{DS}=-4V, V_{GS}=0			−1	μA
Gate-to-Source Leakage Current	$I_{GSS}1$	V_{GS}=±8V, V_{DS}=0			±10	μA
	$I_{GSS}2$	V_{GS}=±4V, V_{DS}=0			±1	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=-10V, I_D=-1mA	-0.3		-1.0	V
Forward Transfer Admittance	|yfs|	V_{DS}=-10V, I_D=-1A	1.8	3.0		S

Marking : JB

Continued on next page.

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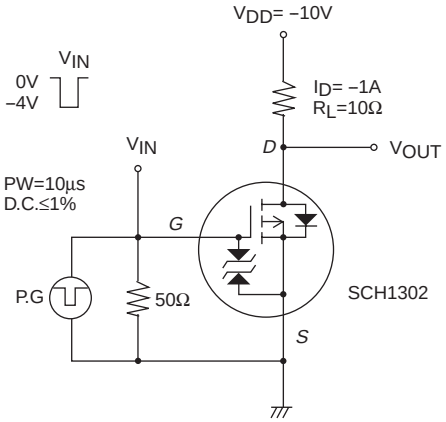
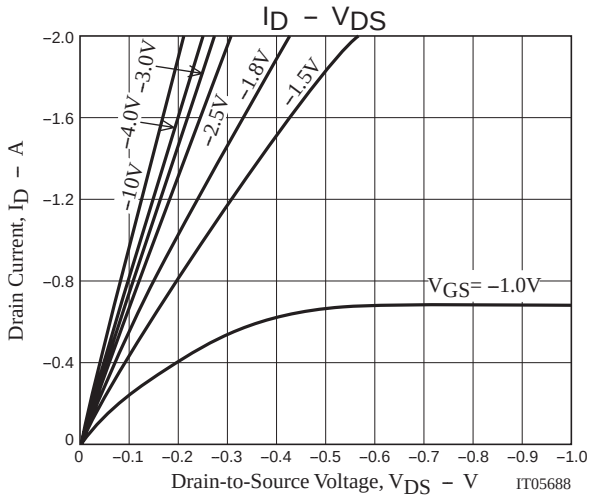
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

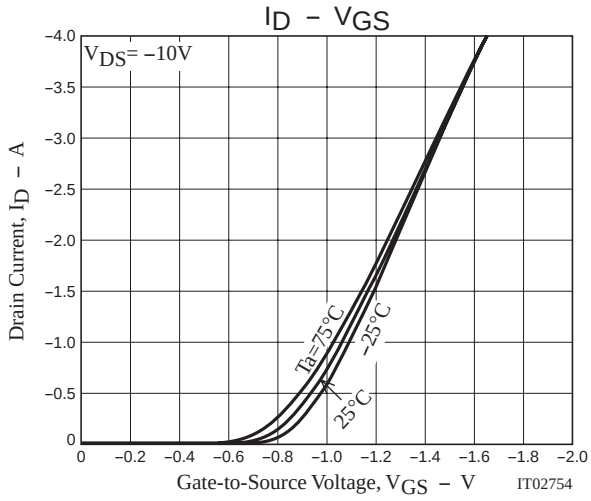
Continued from preceding page.

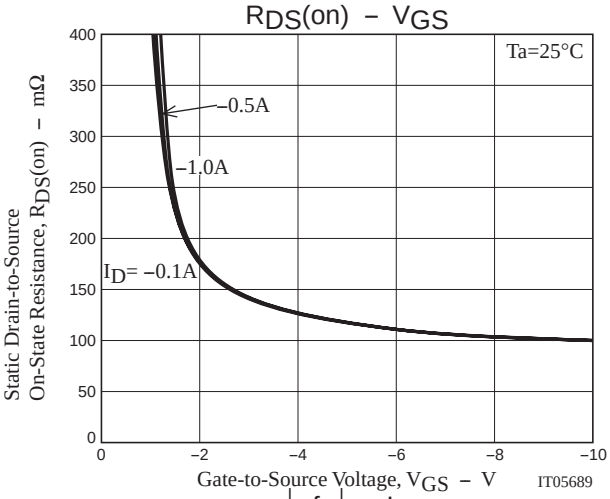
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Static Drain-to-Source On-State Resistance	$R_{DS}(on)1$	I_D=-1A, V_{GS}=-4V		125	165	mΩ
	$R_{DS}(on)2$	I_D=-0.5A, V_{GS}=-2.5V		155	220	mΩ
	$R_{DS}(on)3$	I_D=-0.1A, V_{GS}=-1.8V		195	280	mΩ
Input Capacitance	Ciss	V_{DS}=-10V, f=1MHz		410		pF
Output Capacitance	Coss	V_{DS}=-10V, f=1MHz		60		pF
Reverse Transfer Capacitance	Crss	V_{DS}=-10V, f=1MHz		40		pF
Turn-ON Delay Time	$t_d(on)$	See specified Test Circuit.		9		ns
Rise Time	t_r	See specified Test Circuit.		27		ns
Turn-OFF Delay Time	$t_d(off)$	See specified Test Circuit.		42		ns
Fall Time	t_f	See specified Test Circuit.		38		ns
Total Gate Charge	Qg	V_{DS}=-10V, V_{GS}=-10V, I_D=-2A		10		nC
Gate-to-Source Charge	Qgs	V_{DS}=-10V, V_{GS}=-10V, I_D=-2A		0.6		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=-10V, V_{GS}=-10V, I_D=-2A		1.2		nC
Diode Forward Voltage	V_{SD}	I_S=-2A, V_{GS}=0		-0.88	-1.2	V

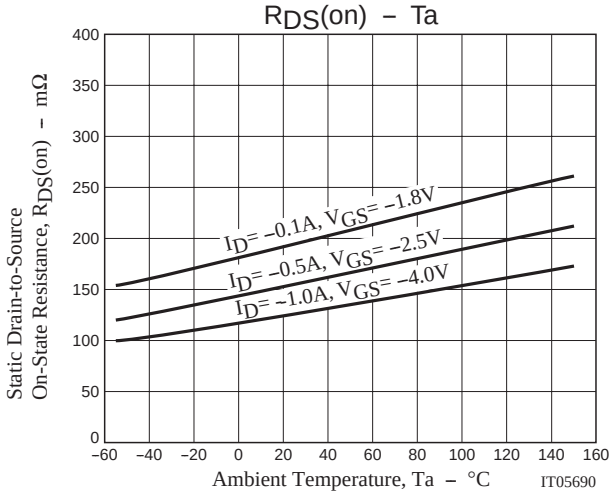
Switching Time Test Circuit

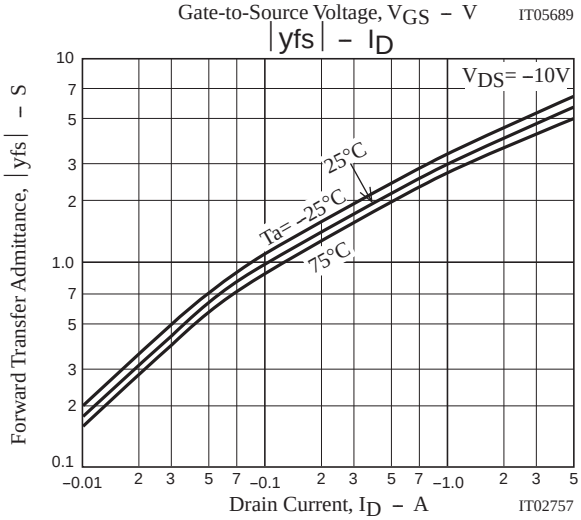


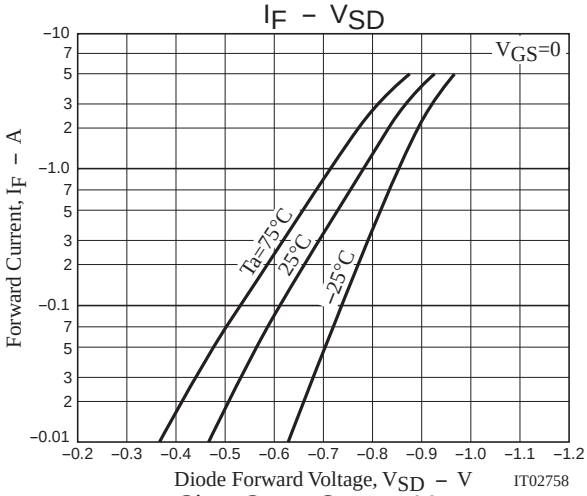


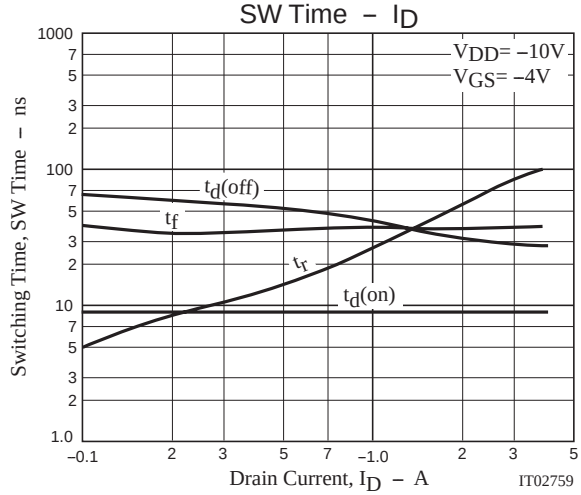


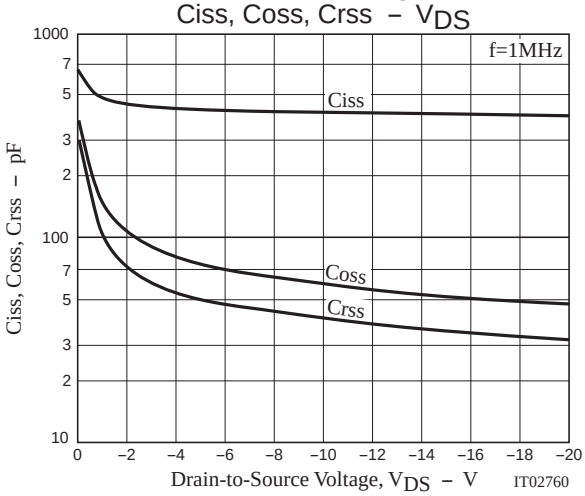

RDS(on) – VGS
Ta=25°C
–0.5A
–1.0A
ID= –0.1A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT05689

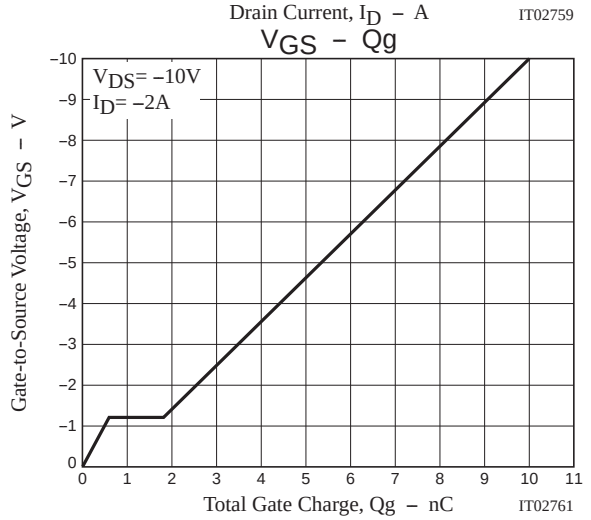

RDS(on) – Ta
ID= –0.1A, VGS= –1.8V
ID= –0.5A, VGS= –2.5V
ID= –1.0A, VGS= –4.0V
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Ambient Temperature, Ta – °C
IT05690

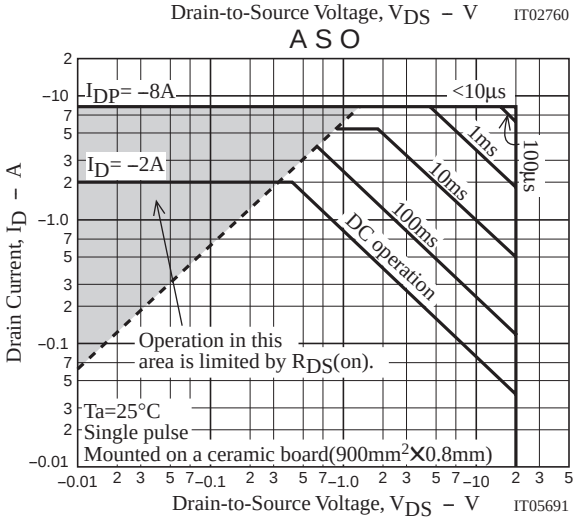

|yfs| – ID
VDS= –10V
25°C
Ta= –25°C
75°C
Forward Transfer Admittance, |yfs| – S
Drain Current, ID – A
IT02757


IF – VSD
VGS=0
Ta=75°C
25°C
–25°C
Forward Current, IF – A
Diode Forward Voltage, VSD – V
IT02758


SW Time – ID
VDD= –10V
VGS= –4V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Drain Current, ID – A
IT02759


Ciss, Coss, Crss – VDS
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT02760


VGS – Qg
VDS= –10V
ID= –2A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT02761


A S O
IDP= –8A
ID= –2A
<10μs
1ms
10ms
100ms
DC operation
100μs
Operation in this area is limited by RDS(on).
Ta=25°C
Single pulse
Mounted on a ceramic board(900mm²×0.8mm)
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT05691