SCH5127

Super I/O with Temperature Sensing, Auto Fan Control and Glue Logic

Product Features

- General Features
  - 3.3 Volt Operation (Most I/O Pins are 5 Volt Tolerant)
  - LPC Interface
  - PC99, PC2001 Compliant
  - ACPI 2.0 Compliant
  - Multiplexed Command, Address and Data Bus
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PME Interface
  - ISA Plug-and-Play Compatible Register Set
  - Programmable Wake-up Event (PME) Interface
  - System Management Interrupt (SMI)
  - 30 General Purpose Input/Output Pins
- AC Power Failure Recovery
- Watchdog Timer Capable to Pulse PWRGD Low and Change GPO Polarity
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with Microchip's Proprietary 82077AA Compatible Core
  - Supports One Floppy Drive
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM® Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - 480 Address, Up to Eight IRQ and Four DMA Options
  - Support 3 Mode FDD
- Enhanced Digital Data Separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Serial Port
  - Two Full Function Serial Ports
  - High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs

- Supports 230k and 460k Baud
- Programmable Baud Rate Generator
- Modem Control Circuitry
- 480 Address and 15 IRQ Options
- Multi-Mode™ Parallel Port with ChiProtect™
  - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bi-directional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection
  - 960 Address, Up to 15 IRQ and Four DMA Options
- Keyboard Controller
  - 8042 Software Compatible
  - 8 Bit Microcomputer
  - 2k Bytes of Program ROM
  - 256 Bytes of Data RAM
  - Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 8 Bit Counter Timer
  - Port 92 Support
  - Fast Gate A20 and KRESET Outputs
  - Phoenix Keyboard BIOS ROM
- Motherboard GLUE Logic
  - Resume Reset Signal Generation
  - IDE Reset Output
  - (4) Buffered PCI Reset Outputs with software controlled reset capability
  - Two 3VSB Gate signal generation for Suspend to RAM or S3/S5 Wake up dual power plane control
  - Front Panel Reset Debouncing and Main 3.3V Power Good Signal Generation
  - Power Supply Turn On Circuitry with Support for power button on PS/2 Keyboard
  - Switches for SMBus Isolation or Voltage Translation for DDC to VGA Monitor Circuitry
  - LED Control (2)
  - Speaker Input & Output Control

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- Fan Control
  - LPC compliant interface for Hardware Monitoring
  - 3 PWM (Pulse width Modulation) Outputs with High Frequency PWM Support
  - 3 Fan Tachometer Inputs
  - Two Programmable automatic fan control thermal zones based on Selectable Temperature Reading
  - Fan Tachometer Event can generate PME, SMI and/or Speaker Warning
- Temperature Monitor
  - Monitoring of Two Remote Thermal Diodes with $\pm 3°C$ TYP, $\pm 5°C$ MAX Accuracy
  - Internal Ambient Temperature Measurement
  - Beta Compensation for Accurate Temperature Sensing on Intel 65nm CPUs
  - Limit Comparison of all Monitored Values
  - Thermal Event can generate PME, SMI and/or Speaker Warning
- Processor Hot and Thermal Trip Support
- Voltage Monitor
  - Monitor Power supplies (V1_IN for +12V, V2_IN for +5V, +2.5V, VCCP, VBAT, +3.3VTR, +3.3VCC, +1.5VTRIP)
  - Limit Comparison of all Monitored Values
  - Voltage Event can generate PME, SMI and/or Speaker Warning
- Intruder Detection Support
- 8 VID (Voltage Identification) Input/Output Pins
- VRD revision 10 or 11 Detection
- 128-Pin QFP (3.2mm footprint) RoHS Compliant Package

Description

The SCH5127 is a 3.3V (Super I/O Block is 5V tolerant) PC99/PC2001 compliant Super I/O controller with an LPC interface. SCH5127 also includes Hardware Monitoring capabilities, enhanced Security features, Power Control logic and Motherboard Glue logic.

The SCH5127's hardware monitoring capability includes temperature, voltage and fan speed monitoring. It has the ability to alert the system to out-of-limit conditions and automatically control the speeds of multiple fans. There are five analog inputs for monitoring external voltages of +V1_IN (for scaled +12V), V2_IN (for scaled +5V), VTRIP (1.5V), +2.5V and VCCP (core processor voltage), as well as internal monitoring of the SIO's VCC, VTR, and VBAT power supplies. The SCH5127 includes support for monitoring two external temperatures via thermal diode inputs and an internal sensor for measuring ambient temperature. The hardware monitoring block of the SCH5127 is accessible via the LPC Bus. The out-of -limit temperature, voltage of fan tachometer events can be reported on the PME and/or SMI output pin and speaker alarm annunciation.

The Motherboard Glue logic includes various power management and system logic including generation of nRSMRST, SMBus isolation buffers, and buffered PCI reset outputs.

The SCH5127 incorporates complete legacy Super I/O functionality including an 8042 based keyboard and mouse controller, an IEEE 1284, EPP, and ECP compatible parallel port, one serial port that is 16C550A UART compatible, one IrDA 1.0 infrared ports, and a floppy disk controller with Microchip's true CMOS 765B core and enhanced digital data separator, The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures and is software and register compatible with Microchip's proprietary 82077AA core. System related functionality, which offers flexibility to the system designer, is available via General Purpose I/O control functions, control of two LED's, and fan control using fan tachometer inputs and pulse width modulator (PWM) outputs.

The SCH5127 is ACPI 1.0/2.0 compatible and therefore supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes support for keyboard and mouse wake-up events.

The SCH5127 supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, DMA Channel and hardware IRQ of each logical device in the SCH5127 may be reprogrammed through the internal configuration registers. There are up to 480 (960 - Parallel Port) I/O address location options, a Serialized IRQ interface, and Three DMA channels.

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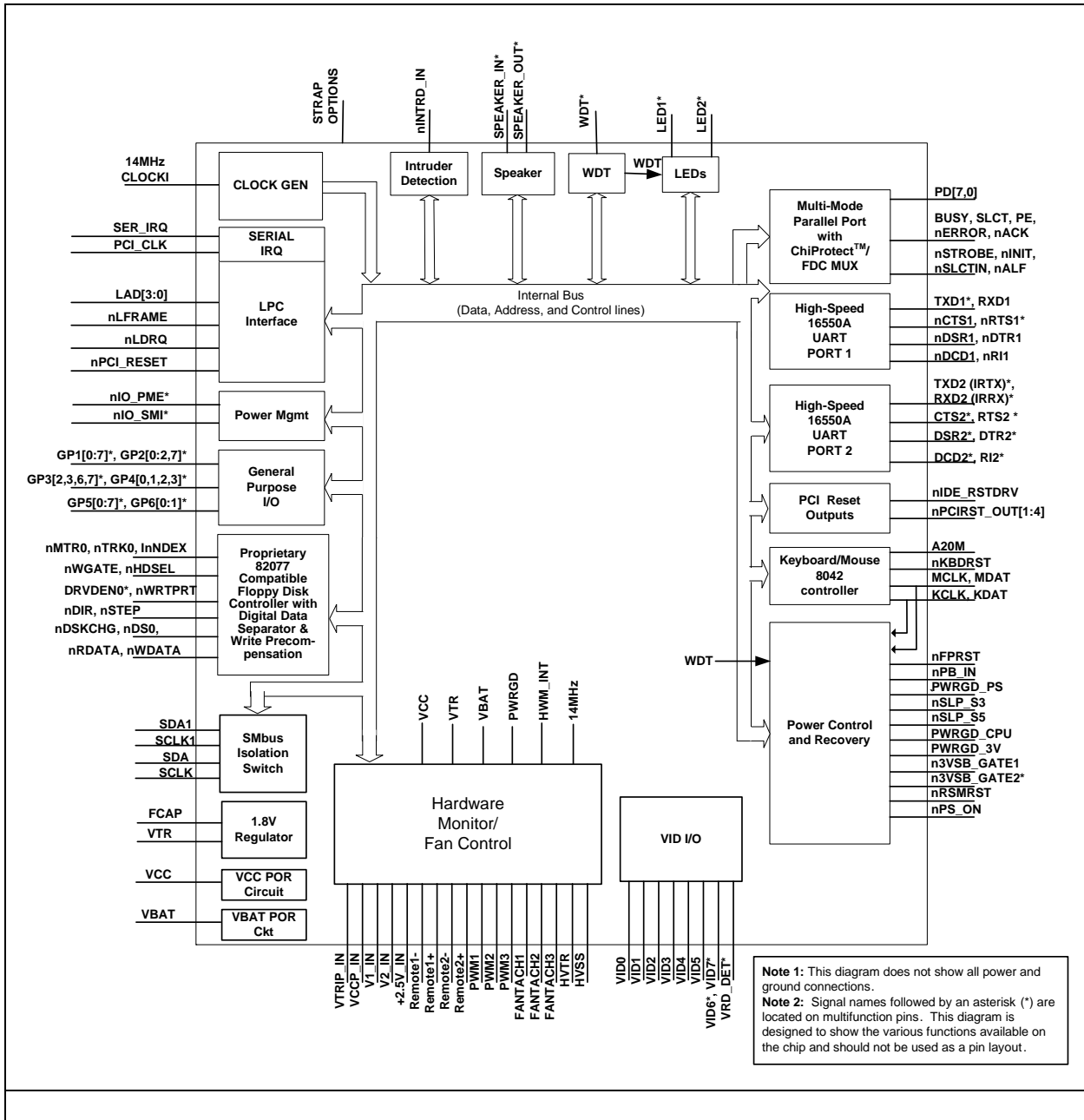
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BLOCK DIAGRAM

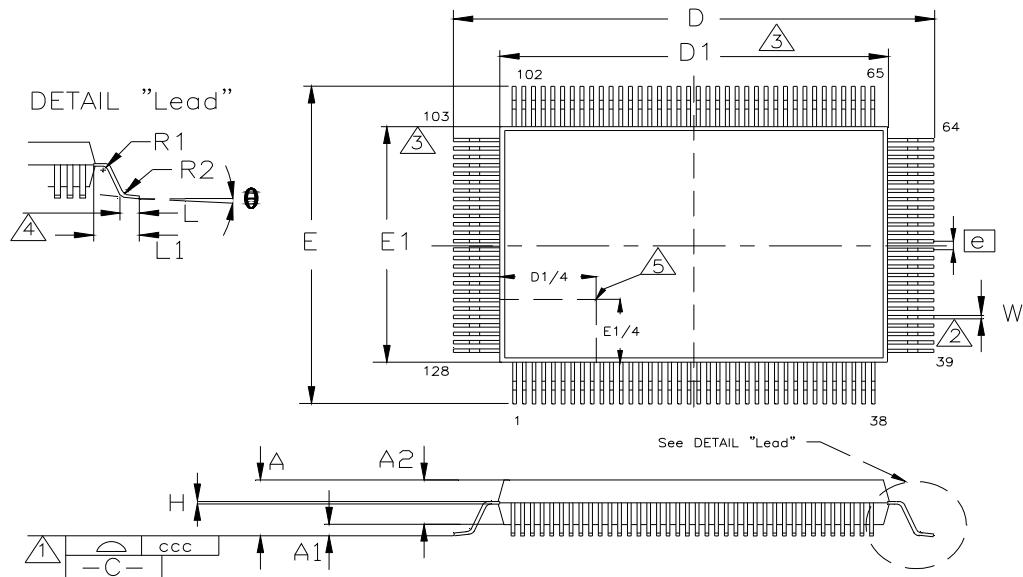**FIGURE 1:   SCH5127 BLOCK DIAGRAM**

Note 1: This diagram does not show all power and ground connections.

Note 2: Signal names followed by an asterisk (*) are located on multifunction pins. This diagram is designed to show the various functions available on the chip and should not be used as a pin layout.

PACKAGE OUTLINE

128 Pin QFP Package Outline, 14x20x2.7 Body, 3.2 mm Footprint

	Min	Nominal	Max	Remarks
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.55	~	3.05	Body Thickness
D	23.00	23.20	23.40	X Span
D1	19.90	20.00	20.10	X body Size
E	17.00	17.20	17.40	Y Span
E1	13.90	14.00	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.60	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0°	~	7°	Lead Foot Angle
W	0.10	~	0.30	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.30	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Note 1: Controlling Unit: millimeter.

2: Tolerance on the position of the leads is ± 0.04 mm maximum.

3: Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm.

4: Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.

5: Details of pin 1 identifier are optional but must be located within the zone indicated.

APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: **REVISION HISTORY**

Revision	Section/Figure/Entry	Correction
DS00001786A (07-11-14)	Replaces previous SMSC version Rev. 0.43 (11-17-06)	

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<u>PART NO.</u>[1]   -   <u>XXX</u>[2]   -   <u>[X]</u>[3]

Device   Package   Tape and Reel
                                  Option

Device:	SCH5127 [1]	
Package:	NW =	128-pin QFP [2] RoHS Compliant package
Tape and Reel Option:	Blank =	Tray packaging
	TR =	Tape and Reel [3]

Example:

SCH5127-NW = 128-pin QFP

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

Note 2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.micro-chip.com/pagehandler/en-us/aboutus/ehs.html .

Note 3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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