CMOS 7-STAGE BINARY COUNTER

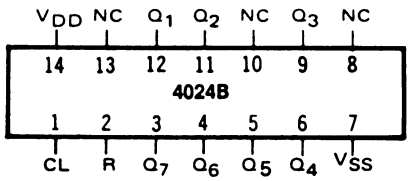
FEATURES

- 7 Fully Static Stages
- Buffered Outputs Available from All Stages
- Common Reset Line
- 8 MHz Counting Rate @ 10Vdc
- All Inputs Buffered

DESCRIPTION

The 4024B is a single chip monolithic medium scale integrated circuit containing N-Channel and P-Channel enhancement-mode MOS transistors. Seven single-phase clocked counting stages are provided with the Q output of each stage accessible. The Counter is reset to "zero" by a high level on the Reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse.

CONNECTION DIAGRAM
(all packages)



TRUTH TABLE

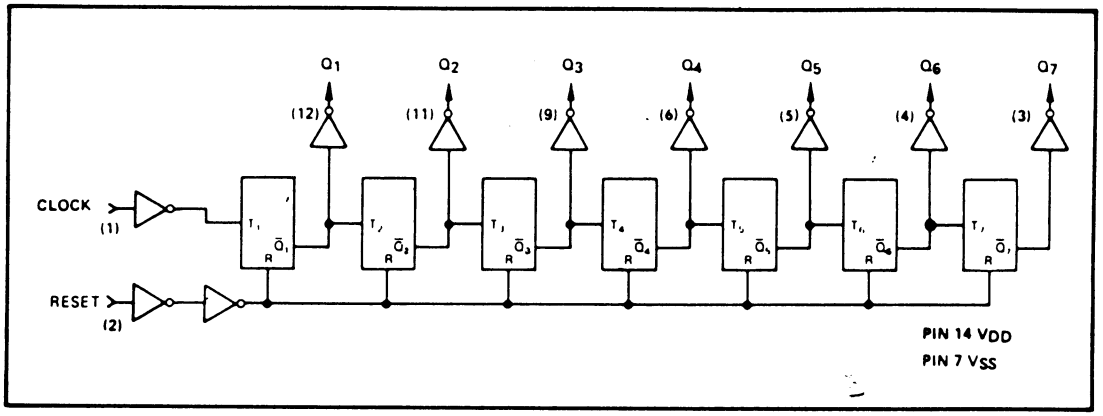
Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
⌐	0	No Change
⌐	1	All Outputs Low
¬	0	Advance One Count
¬	1	All Outputs Low

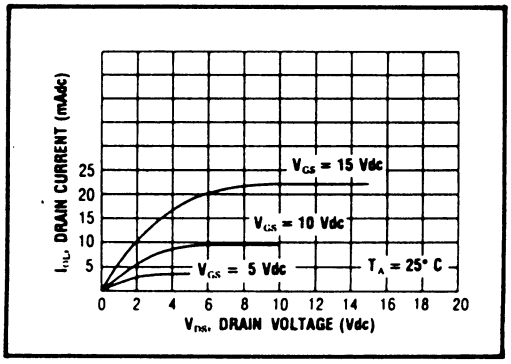
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

LOGIC DIAGRAM





Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications"

[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q_1	t_{PLH}, t_{PHL}	5	–	180	360	ns
		10	–	80	160	
		15	–	65	130	
Q_i to Q_{i+1}	t_{PLH}, t_{PHL}	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	120	240	ns
		10	–	60	120	
		15	–	45	90	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	2	4	—	MHz
		10	5	10	—	
		15	6	12	—	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{tCL}	5	15	–	—	μs
		10	10	–	—	
		15	5	–	—	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
RESET REMOVAL TIME	t_{rem}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	

TYPICAL COUNTER STAGE