CMOS 12-STAGE BINARY COUNTER

FEATURES

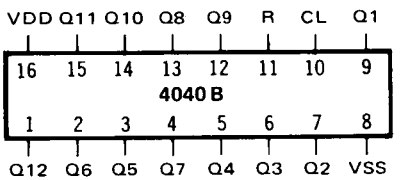
- 12 Fully Static Stages
- All 12 Buffered Outputs Available
- Common Reset Line
- 8MHz Counting Rate @ 10Vdc
- All Inputs Buffered

DESCRIPTION

The 4040 B consists of 12-ripple-carry binary counter stages with appropriate input buffers and reset circuitry. The counter is reset to its "all 0's" state by a high level on the Reset input. The counter is advanced one count on the negative-going transition of each input pulse. Isolation from external noise and the effects of loads is provided by output buffering.

Applications include time delay circuits, counter controls, and frequency dividers.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

TRUTH TABLE

Clock	Reset	Output State
⌐‾	0	No Change
‾⌐	0	Advance to next state
x	1	All Outputs are low

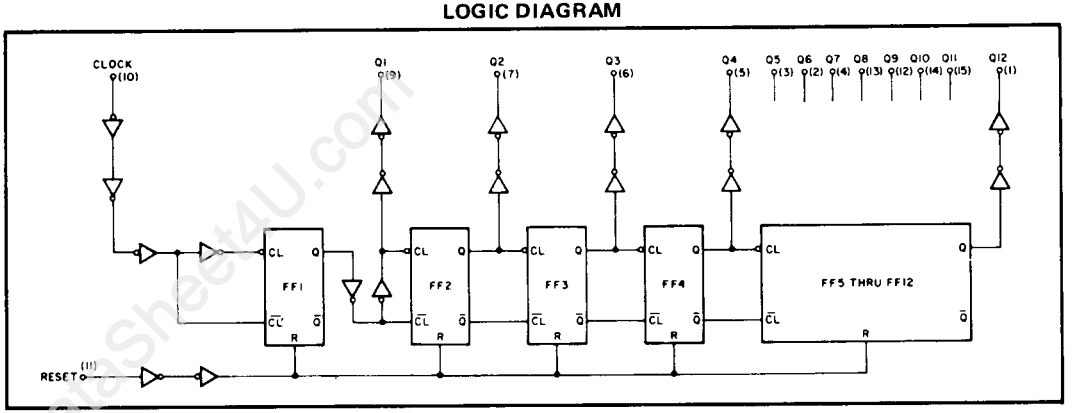
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

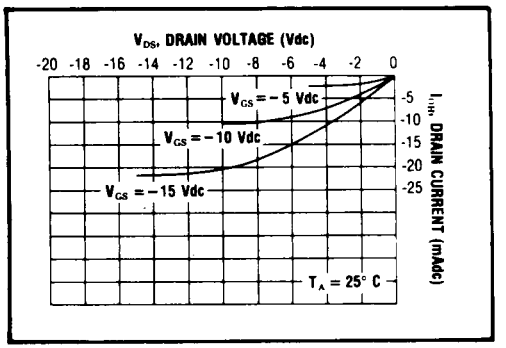
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	15	–	0.2	20	–	600	

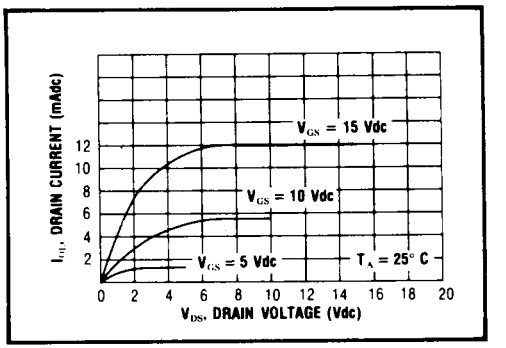
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q1	t_{PLH}, t_{PHL}	5	–	180	320	ns
		10	–	80	160	
		15	–	65	130	
Q_i to Q_{i+1}	t_{PLH}, t_{PHL}	5	–	100	200	ns
		10	–	40	60	
		15	–	30	30	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	3.0	4.5	–	MHz
		10	6.0	9.0	–	
		15	7.5	11.0	–	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	50	100	–	μs
		10	50	100	–	
		15	50	100	–	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	75	150	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
RESET REMOVAL TIME	t_{rem}	5	–	150	300	ns
		10	–	65	125	
		15	–	40	75	

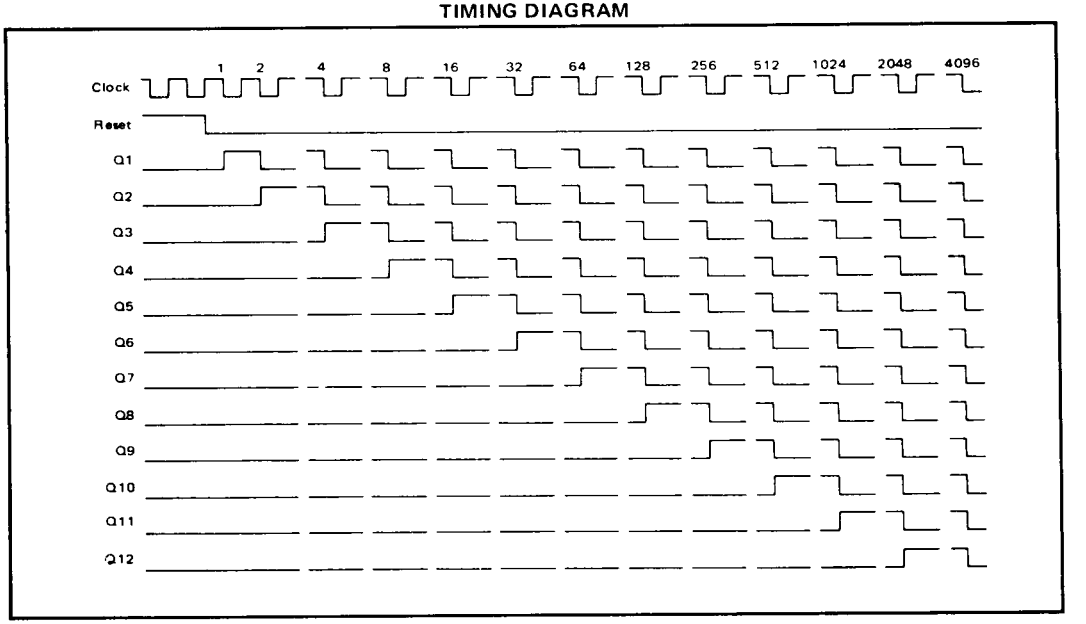


Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

TIMING DIAGRAM



TYPICAL COUNTER STAGE