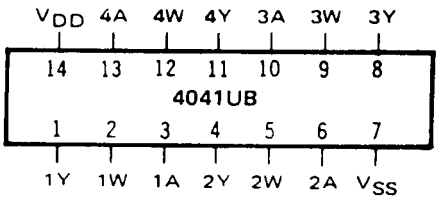
CMOS QUAD TRUE/COMPLEMENT BUFFER

FEATURES

- Both True and Complement Outputs Available Simultaneously
- High Source and Sink Current
- Diode Protection on All Inputs

CONNECTION DIAGRAM
(all packages)



DESCRIPTION

The 4041UB Quad True/Complement Buffer is a monolithic integrated circuit constructed with P-Channel and N-Channel enhancement-mode devices. The outputs have low resistance and are capable of sinking or sourcing high currents for use in driver applications where high noise immunity and low power dissipation are required.

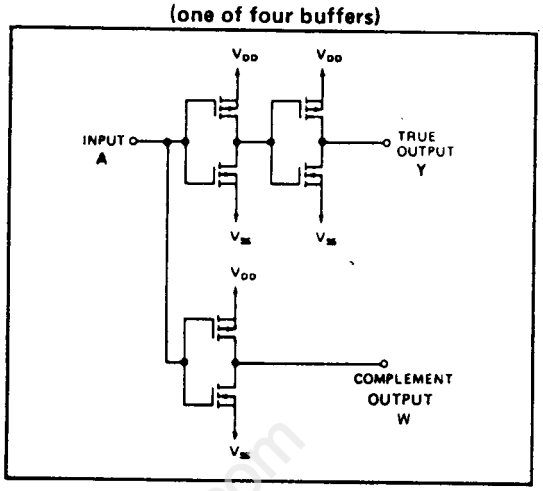
This device is useful as a line-driver, CMOS-to-TTL driver, low-power resistor-network driver for A/D and D/A conversion, display and clock drivers.

RECOMMENDED OPERATING CONDITIONS

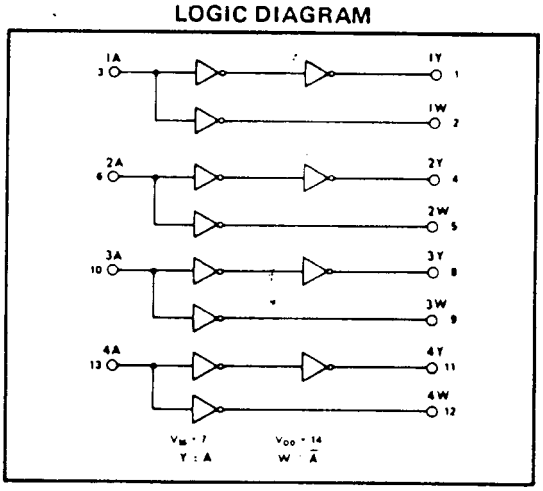
For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

SCHEMATIC DIAGRAM
(one of four buffers)



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	1.0	–	0.005	1.0	–	30	μAdc
		10	All valid input	–	2.0	–	0.01	2.0	–	60	
		15	combinations	–	4.0	–	0.02	4.0	–	120	
MINIMUM INPUT HIGH VOLTAGE	V_{IH}										
Non-Inverting Outputs		5	V_{OH}=4.5V	–	3.5	–	2.75	3.5	–	3.5	Vdc
		10	V_{OH}=9.0V	–	7.0	–	5.5	7.0	–	7.0	
		15	V_{OH}=13.5V	–	11.0	–	8.25	11.0	–	11.0	
			$\|I_O\| \leq 1\mu A$								
Inverting Outputs		5	V_{OL}=0.5V	–	4.0	–	2.75	4.0	–	4.0	Vdc
		10	V_{OL}=1.0V	–	8.0	–	5.5	8.0	–	8.0	
		15	V_{OL}=1.5V	–	12.0	–	8.25	12.0	–	12.0	
			$\|I_O\| \leq 1\mu A$								
MAXIMUM INPUT LOW VOLTAGE	V_{IL}										
Non-Inverting Outputs		5	V_{OL}=0.5V	1.5	–	1.5	2.25	–	1.5	–	Vdc
		10	V_{OL}=1.0V	3.0	–	3.0	4.5	–	3.0	–	
		15	V_{OL}=1.5V	4.0	–	4.0	6.75	–	4.0	–	
			$\|I_O\| \leq 1\mu A$								
Inverting Outputs		5	V_{OH}=4.5V	1.0	–	1.0	2.25	–	1.0	–	Vdc
		10	V_{OH}=9.0V	2.0	–	2.0	4.5	–	2.0	–	
		15	V_{OH}=13.5V	3.0	–	3.0	6.75	–	3.0	–	
			$\|I_O\| \leq 1\mu A$								
OUTPUT HIGH (SOURCE) CURRENT	I_{OH}										
Non-Inverting Outputs		5	V_{OH}=4.6V	-1.7	–	-1.4	-2.8	–	-1.0	–	mAdc
		10	V_{OH}=9.5V	-5.0	–	-4.0	-8.0	–	-2.8	–	
		15	V_{OH}=13.5V	-16	–	-13	-26	–	-9	–	
			$V_{IN}=V_{DD}$								
Inverting Outputs		5	V_{OH}=4.6V	-0.75	–	-0.6	-1.0	–	-0.42	–	mAdc
		10	V_{OH}=9.5V	-2.2	–	-1.8	-3.6	–	-1.3	–	
		15	V_{OH}=13.5V	-8.0	–	-6.5	-13	–	-4.5	–	
			$V_{IN}=V_{SS}$								
OUTPUT LOW (SINK) CURRENT	I_{OL}										
Non-Inverting Outputs		5	V_{OL}=0.4V	2.0	–	1.6	3.2	–	1.1	–	mAdc
		10	V_{OL}=0.5V	6.2	–	5.0	10	–	3.5	–	
		15	V_{OL}=1.5V	23	–	18.5	38	–	13	–	
			$V_{IN}=V_{SS}$								
Inverting Outputs		5	V_{OL}=0.4V	1.0	–	0.8	1.3	–	0.56	–	mAdc
		10	V_{OL}=0.5V	2.5	–	2.0	4.0	–	1.4	–	
		15	V_{OL}=1.5V	11	–	8.5	17	–	5.8	–	
			$V_{IN}=V_{DD}$								

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

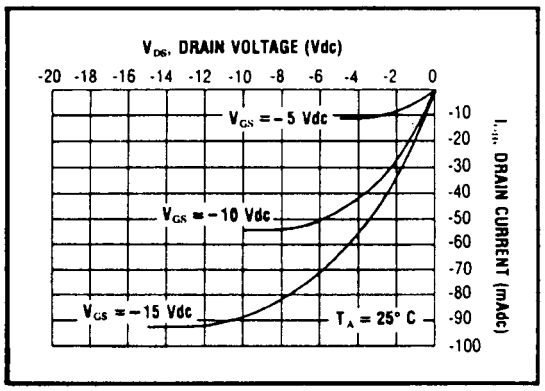
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

ELECTRICAL CHARACTERISTICS (Continued)

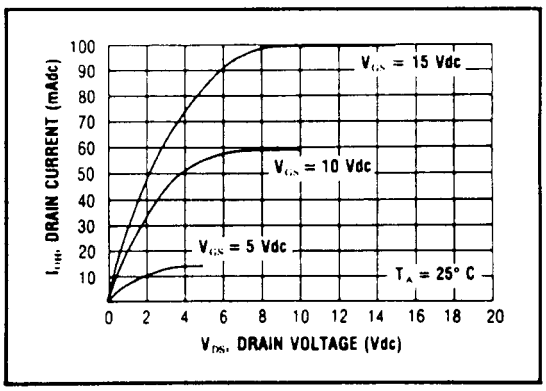
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Non-Inverting Outputs	t_{PLH}, t_{PHL}	5 10 15	– – –	60 35 25	120 70 50	ns
Inverting Outputs	t_{PLH}, t_{PHL}	5 10 15	– – –	60 35 25	120 70 50	ns
OUTPUT TRANSITION TIME Non-Inverting Outputs	t_{TLH}, t_{THL}	5 10 15	– – –	40 20 15	80 40 30	ns
Inverting Outputs	t_{TLH}, t_{THL}	5 10 15	– – –	35 20 15	70 40 30	ns
INPUT CAPACITANCE	C_{IN}	–	–	10	15	pF

NON-INVERTING (TRUE) OUTPUT

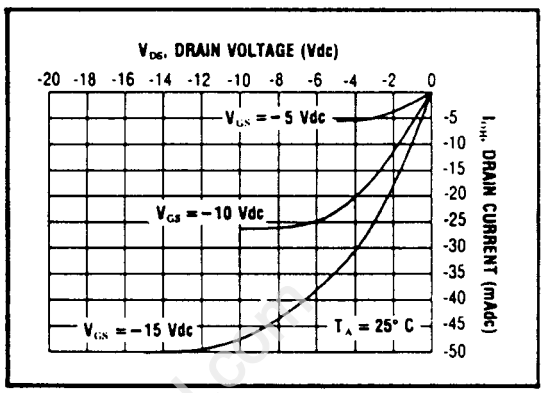


Typical P-Channel
Source Current Characteristics

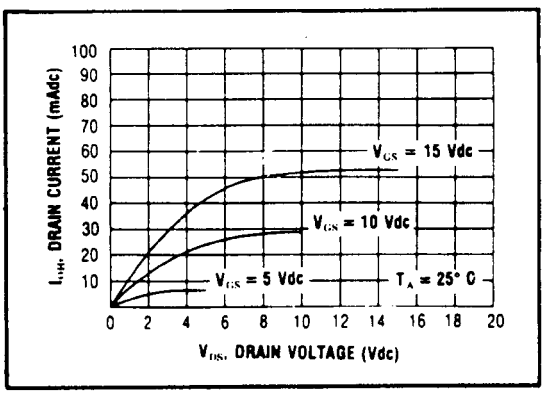


Typical N-Channel
Sink Current Characteristics

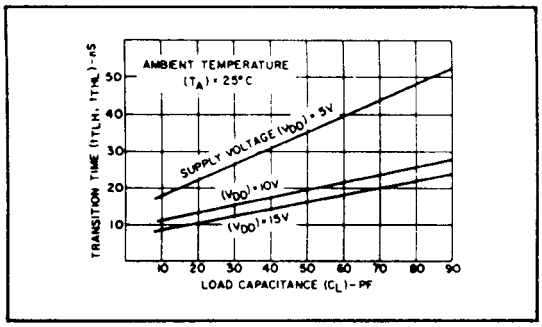
INVERTING (COMPLEMENT) OUTPUT



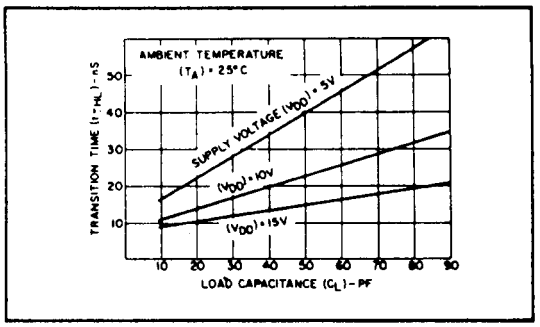
Typical P-Channel
Source Current Characteristics



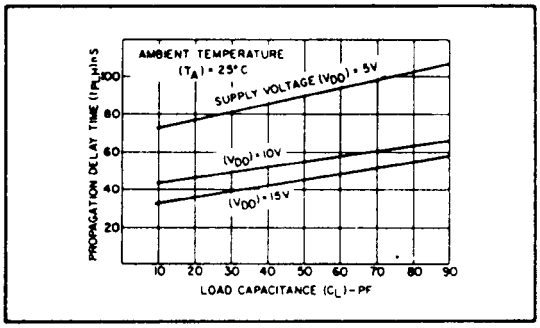
Typical N-Channel
Sink Current Characteristics



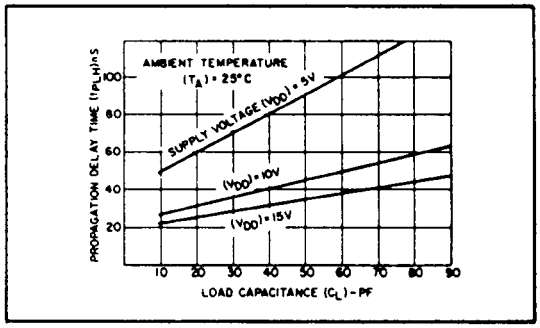
Typical transition time vs. C_L-true output.



Typical transition time vs. C_L-complement output.



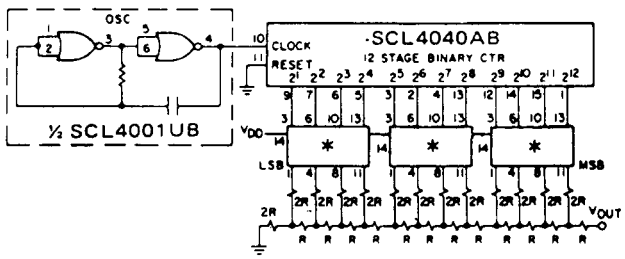
Typical propagation delay time vs. C_L-true output.



Typical propagation delay time vs. C_L-complement output.

APPLICATIONS INFORMATION

Low Power D/A Converter



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For resolution and accuracy of ± ½ least significant bit (LSB), choose the values for R (shown in Table I) where R equals the value of the external ladder resistor plus the switch source impedance.

The values have been tabulated for V_{DD} = 5V and V_{SS} = 0V. For different supply (reference) voltages, the switch source impedance must be computed and added to the value of R shown in Table I).

TABLE I. RESISTANCE VALUES AT $V_{DD}-V_{SS}$ = 5V, T_A = 25°C

RESOLUTION	ACCURACY OF 1/2 LSB	R_{min} (Ω)
4 bit	±3.25% of full scale	3.5 k
6 bit	±0.8% of full scale	14 k
8 bit	±0.2% of full scale	56 k
10 bit	±0.05% of full scale	224 k
12 bit	±0.0125% of full scale	896 k

TABLE II. ON RESISTANCE VALUES AT V_{DS} = 0.1V, T_A = 25°C

$V_{DD}-V_{SS}$ (Volts)	R_N (Ω)	R_P (Ω)
5	175 ± 50	200 ± 75
10	75 ± 25	90 ± 30