

CMOS QUAD 3-STATE R-S LATCHES

FEATURES

- ◆ Separate Set and Reset Inputs for each Latch
- ◆ Active-High (4043 B) or Active-Low (4044 B) Inputs
- ◆ 3-State Outputs with Common Enable

DESCRIPTION

4043B types are Quad cross-coupled 3-state CMOS NOR Latches, and the 4044 B types are Quad cross-coupled 3-state CMOS NAND Latches. Each latch has a separate Q output and individual Set and Reset inputs. The Q outputs are gated through transmission gates controlled by a common Enable input. A logic "1" or "high" on the Enable input, connects the latch states to the Q outputs. A logic "0" or "low" on the Enable input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs. The logic operation of the latches is summarized in the truth table below.

TRUTH TABLES

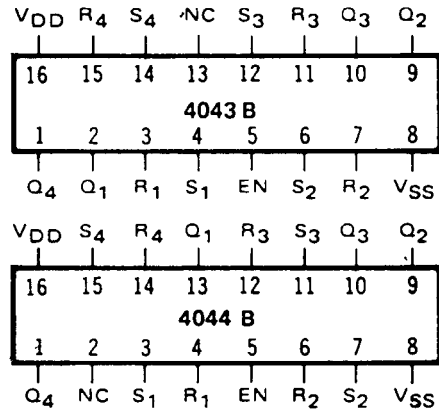
4043 B			
S	R	E	Q
X	X	0	OC*
0	0	1	NC+
1	0	1	1
0	1	1	0
1	1	1	Δ

* OPEN CIRCUIT
+ NO CHANGE
Δ DOMINATED BY S = 1 INPUT

4044 B			
S	R	E	Q
X	X	0	OC*
1	1	1	NC+
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

* OPEN CIRCUIT
+ NO CHANGE
ΔΔ DOMINATED BY R = 0 INPUT

CONNECTION DIAGRAMS (all packages)



Add suffix for package:

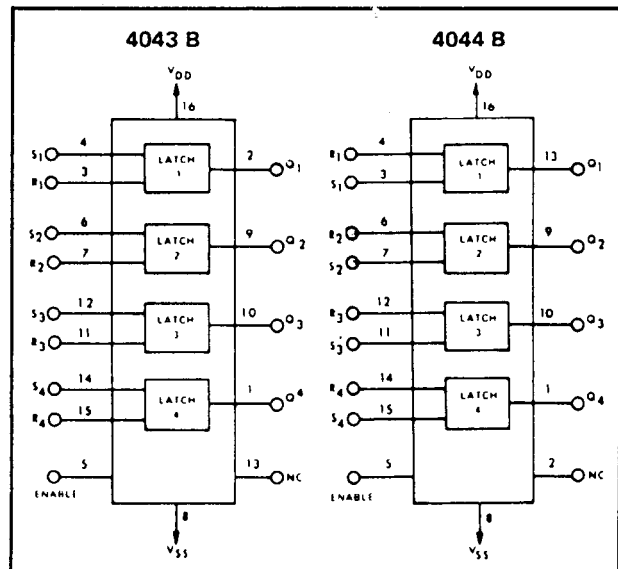
- C 16-pin Cerdip
- E 16-pin Epoxy

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
		-40 to +85	°C

BLOCK DIAGRAMS



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	-	1.0	-	0.005	1.0	-	30	μA _{dc}
			-	2.0	-	0.01	2.0	-	60	
			-	4.0	-	0.02	4.0	-	120	
3-STATE OUTPUT LEAKAGE CURRENT	I _{ZL}	Enable = V _{SS}	-	±0.1	-	±10 ⁻⁴	±0.1	-	±1.0	μA _{dc}

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

² T_{LOW} = -55°C for C

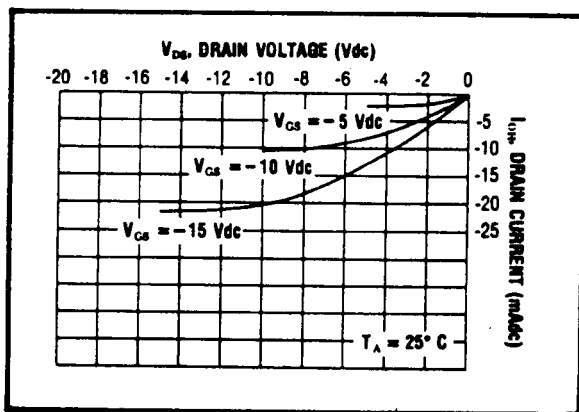
= -40°C for E

T_{HIGH} = +125°C for C

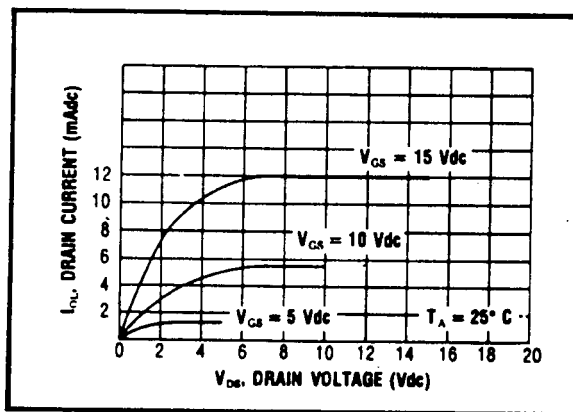
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From S or R Inputs	t _{PLH} , t _{PHL}	5	-	150	ns
		10	-	70	
		15	-	50	
From Enable Input	t _{PHZ} , t _{PLZ} t _{PZH} , t _{PZL}	5	-	75	ns
		10	-	35	
		15	-	30	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	-	100	ns
10	-	50			
15	-	40			
MINIMUM SET OR RESET PULSE WIDTH	PW _S , PW _R	5	-	80	ns
10	-	40			
15	-	30			
SET OR RESET REMOVAL TIME	t _{rem}	5	-	25	ns
10	-	15			
15	-	10			

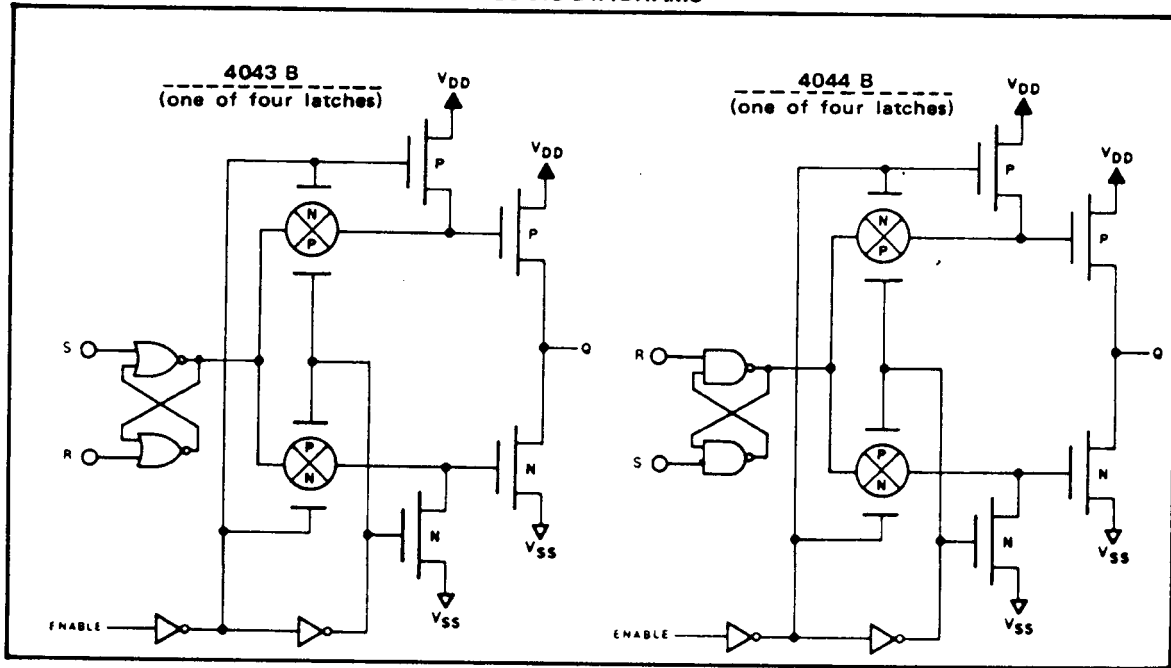


Typical P-Channel Source Current Characteristics



Typical N-Channel Sink Current Characteristics

LOGIC DIAGRAMS



APPLICATIONS INFORMATION

