

CMOS PHASE-LOCKED LOOPS

FEATURES

- ◆ Very low power consumption – 70 μ W (typ) @ $f_o = 10$ kHz, 5Vdc
- ◆ Operating frequency range (no offset) –
Up to 3MHz (typ) @ 10Vdc (4046B)
Up to 4MHz (typ) @ 10Vdc (4446B)
- ◆ Low frequency drift – 0.04%/°C (typ) @ 10Vdc
- ◆ Choice of two phase comparators:
 1. Exclusive-OR network
 2. Edge-controlled memory network with phase-pulse output for lock indication
- ◆ VCO Inhibit control for ON-OFF keying and ultra-low standby power consumption
- ◆ High VCO linearity 1% (typ)
- ◆ Source-follower output of VCO control input (Demodulator Output)
- ◆ Zener Diode to assist Supply Regulation

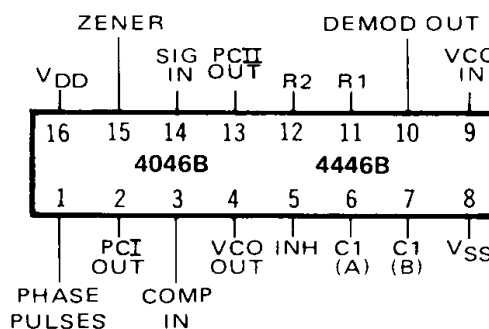
APPLICATIONS

- ◆ FM demodulator and modulator
- ◆ Frequency synthesis and multiplication
- ◆ Frequency discriminator
- ◆ Data synchronization
- ◆ Voltage-to-frequency conversion
- ◆ Tone decoding
- ◆ FSK-Modems
- ◆ Signal conditioning

DESCRIPTION

The 4046B and 4446B phase-locked loops contain two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common inputs. The Signal input can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator I (an exclusive-OR gate) provides a digital error signal PCI_{out} , and maintains 90° phase shift at the center frequency between Signal and Comparator inputs (both at 50% duty cycle). Phase comparator II (with leading edge sensing logic) provides digital error signals PCI_{out} and Phase Pulses, and maintains a 0° phase shift between input signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins C1A, C1B, R1, and R2. The source follower output, Demod Out, with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh , when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

CONNECTION DIAGRAM (all packages)



Add suffix for package:

C	16-pin Cerdip
D	16-pin Ceramic
E	16-pin Epoxy
F	16-pin Flat
H	Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

BLOCK DIAGRAM

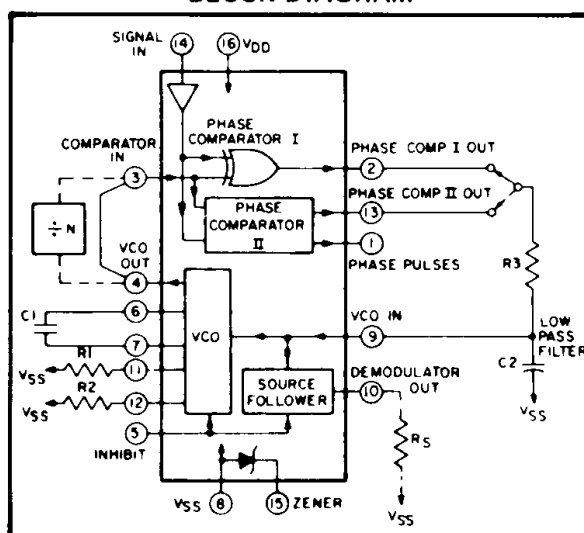


Fig. 1

VCO SECTION

The VCO requires one external capacitor (C1) and one to two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULA-

TOR OUTPUT). If this terminal is used, a load resistor (R_S) of $50k\Omega$ or more should be connected from this terminal to V_{SS} . If unused, this terminal should be left open. The VCO can be connected directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

PHASE COMPARATORS

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" $\leq 30\%$ ($V_{DD} - V_{SS}$), logic "1" $\geq 70\%$ ($V_{DD} - V_{SS}$)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analogously to an over-driven balanced mixer. To maximize the lock range, the signal and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_0).

The frequency range of input signals on which the PLL will lock, if it was initially out of lock, is defined as the frequency capture range ($2f_c$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range can not exceed the lock range.

With phase comparator I, the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180° , and is 90° at the center frequency. Figure 2 shows the (typical) triangular phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition is shown in Figure 3.

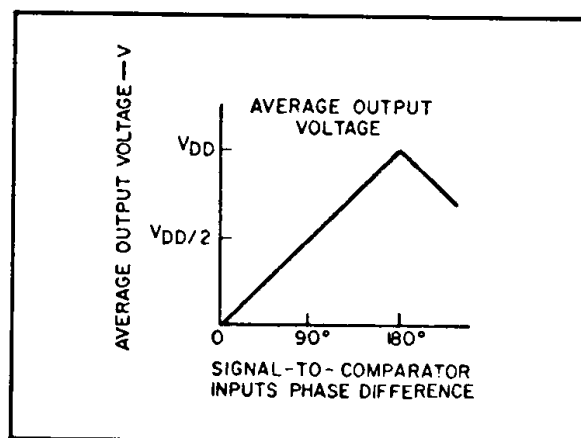


Fig. 2 — Phase-comparator I characteristics at low-pass filter output.

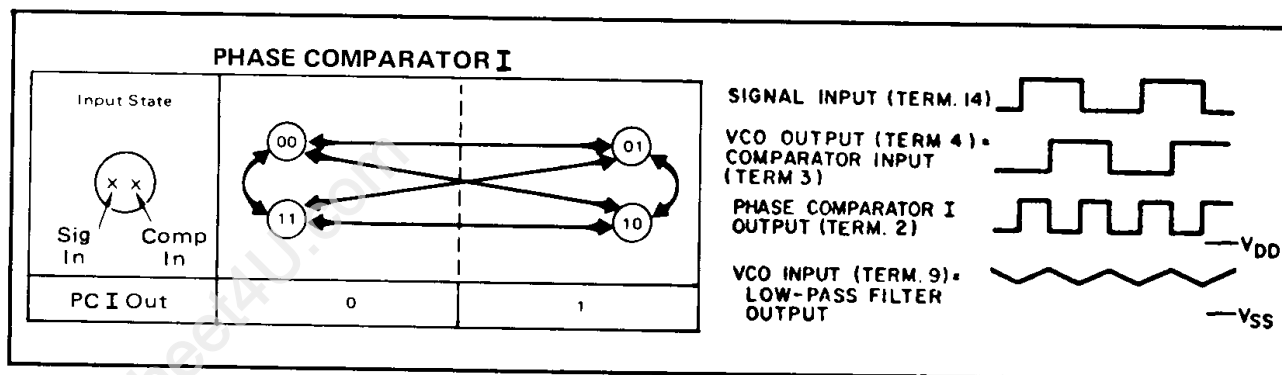
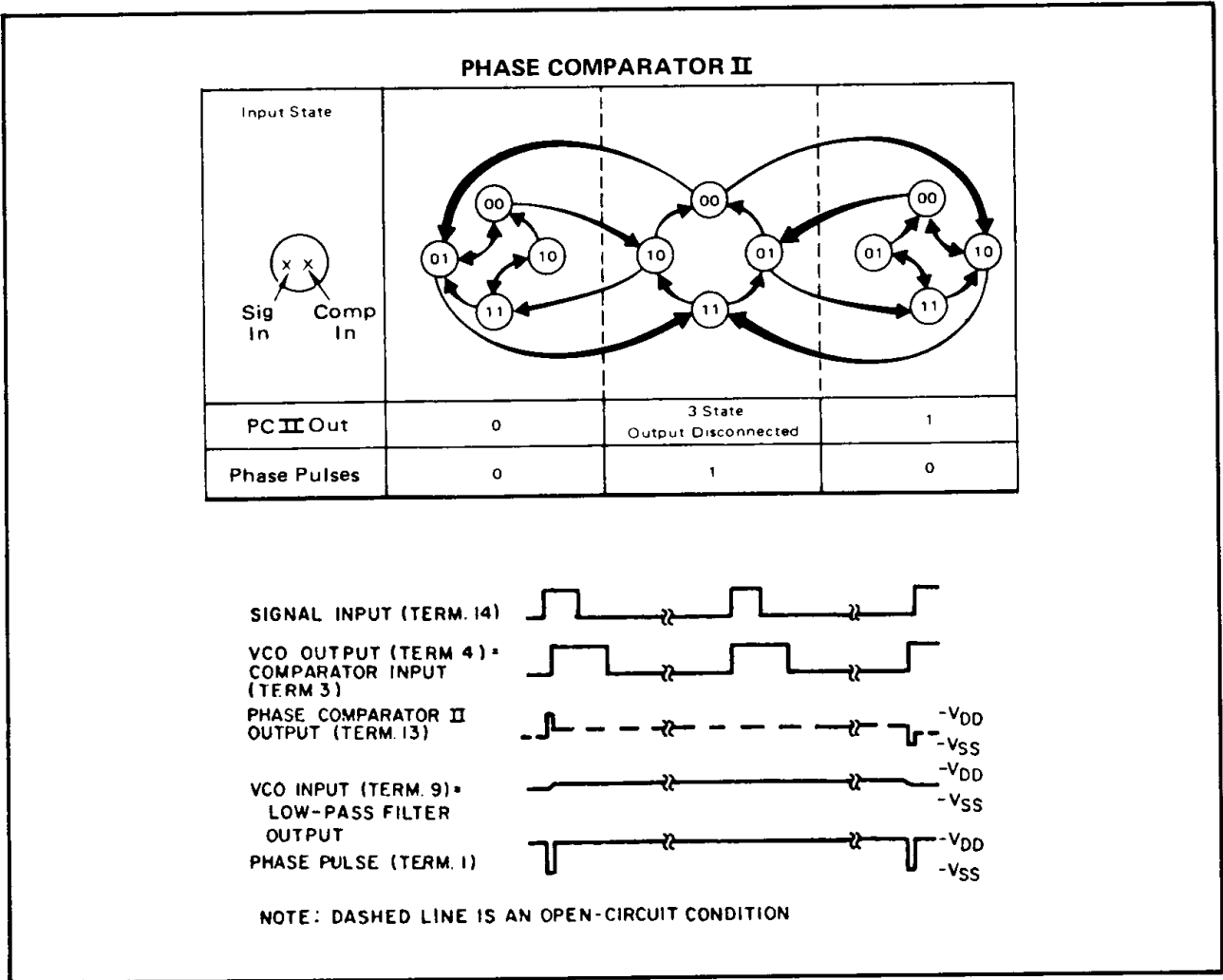


Fig. 3 — Typical waveforms employing phase comparator I in locked condition



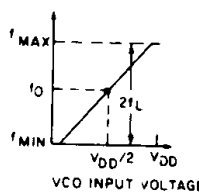
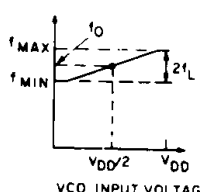
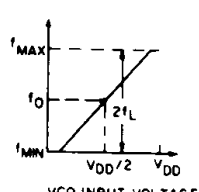
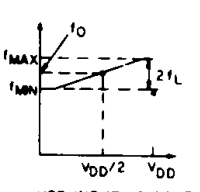
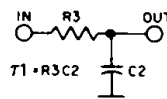
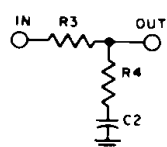
DESIGN INFORMATION

This information is a guide for approximating the values of external components for the 4046B and 4446B in a Phase-Locked Loop system. The selected external components must be within the following ranges:

$$R_1, R_2 \geq 2k\Omega, R_S \geq 10k\Omega$$

$$C_1 \geq 15pF$$

In addition to the given design information refer to Figure 5 for R_1 , R_2 , and C_1 component selections.

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, f_0		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L = \text{full VCO frequency range}$ $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$	 $2f_C \approx \frac{1}{\pi} \sqrt{\frac{2\pi f_L}{\tau_1 \cdot R_3 C_2}}$		$f_C = f_L$	
Loop Filter Component Selection	 For $2f_C$, see Ref.			
Phase Angle between Signal and Comparator	90° at center frequency (f_0), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	- Given: f_0 - Use f_0 with Fig.5a to determine R_1 and C_1	- Given: f_0 and f_L - Calculate f_{min} from the equation $f_{min} = f_0 - f_L$ - Use f_{min} with Fig. 5b to determine R_2 and C_1 - Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_0 + f_L}{f_0 - f_L}$ - Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R_2/R_1 to obtain R_1	- Given: f_{max} - Calculate f_0 from the equation $f_0 = \frac{f_{max}}{2}$ - Use f_0 with Fig.5a to determine R_1 and C_1	- Given: f_{min} & f_{max} - Use f_{min} with Fig.5b to determine R_2 and C_1 - Calculate $\frac{f_{max}}{f_{min}}$ - Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R_2/R_1 to obtain R_1

REF. G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

ELECTRICAL CHARACTERISTICS ¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	Inhibit = V _{DD} Signal Input = V _{DD}	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.01	10	—	300	
			—	20	—	0.2	20	—	600	
TOTAL POWER DISSIPATION	P _T	Inh = V _{SS} , VCO _{IN} = $\frac{V_{DD}}{2}$ f _o = 10kHz, C _L = 15pF, R1 = 1MΩ, R2 = R _S = ∞	—	—	—	0.07	—	—	—	mW
			—	—	—	0.6	—	—	—	
			—	—	—	2.4	—	—	—	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

PARAMETER		CONDITIONS	V _{DD}	25 °C			UNIT			
				Min.	Typ.	Max.				
VCO SECTION										
MAXIMUM OPERATING FREQUENCY	f _{max}	R2 = ∞ VCO _{IN} = V _{DD}	R1 C1							
			10k 50pF	5 10 15	0.5 1.0 1.3	0.8 1.5 1.9	— — —	MHz		
			5k 50pF	5 10 15	0.6 1.4 1.8	1.0 2.1 2.7	— — —	MHz		
			2k 50pF	5 10 15	— — —	1.3 2.9 3.8	— — —	MHz		
			R2 = ∞ VCO _{IN} = V _{DD}	R1 C1						
				10k 50pF	5 10 15	0.7 1.3 1.9	1.0 2.0 2.8	— — —	MHz	
		5k 50pF		5 10 15	0.9 1.9 2.6	1.3 2.9 3.9	— — —	MHz		
		2k 50pF		5 10 15	— — —	1.8 3.9 5.4	— — —	MHz		
		LINEARITY		R2 = ∞ VCO _{IN} = 2.5±0.3V, R1 ≥ 10kΩ	5	—	1	—	—	%
				VCO _{IN} = 5.0±2.5V, R1 ≥ 400kΩ	10	—	1	—	—	
				VCO _{IN} = 7.5±5.0V, R1 ≥ 1MΩ	15	—	1	—	—	

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	V _{DD}	+25°C			UNIT		
			Min.	Typ.	Max.			
VCO SECTION (Continued)								
TEMPERATURE-FREQUENCY STABILITY	No Offset	R2 = ∞	5	—	0.12-0.24	% / °C		
			10	—	0.04-0.08			
			15	—	0.015-0.03			
	With Offset	R2 ≤ 10X R1	5	—	0.06-0.12	% / °C		
			10	—	0.05-0.1			
			15	—	0.03-0.06			
INPUT RESISTANCE (VCO _{IN})	R _{IN}	5, 10, 15	—	10 ⁶	—	MΩ		
OUTPUT DUTY CYCLE		All valid input combinations and voltages	—	50	—	%		
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	C _L = 50pF	5	—	100	200	ns	
			10	—	50	100		
			15	—	40	80		
PHASE COMPARATORS								
INPUT RESISTANCE Signal Input	R _{IN}		5	1	3	—	MΩ	
			10	0.2	0.7	—		
			15	0.1	0.3	—		
Comparator Input	R _{IN}	5, 10, 15	—	10 ⁶	—	MΩ		
AC-COUPLED INPUT SENSITIVITY Signal Input	V _{IN}		5	—	200	400	mV	
			10	—	400	800		
			15	—	700	1400		
OUTPUT TRANSITION TIME	PCI, PCII Outputs	C _L = 50pF	5	—	100	200	ns	
			10	—	50	100		
			15	—	40	80		
	Phase Pulses Output		5	—	130	260		ns
			10	—	65	130		
			15	—	50	100		
DEMODULATOR OUTPUT								
OFFSET VOLTAGE	VCO _{IN} - V _{DEM}	R _S ≥ 50kΩ	5	—	1.4	2.2	V _{dc}	
			10	—	1.6	2.2		
			15	—	1.8	2.2		
LINEARITY		R _S ≥ 50kΩ VCO _{IN} = 2.5±0.3V VCO _{IN} = 5.0±2.5V VCO _{IN} = 7.5±5.0V	5	—	0.1	—	%	
			10	—	0.6	—		
			15	—	0.8	—		
ZENER DIODE								
ZENER VOLTAGE	V _Z	I _Z = 50μA	—	6.3	7.0	7.7	V	
DYNAMIC RESISTANCE	R _Z	I _Z = 1mA	—	—	100	—	Ω	

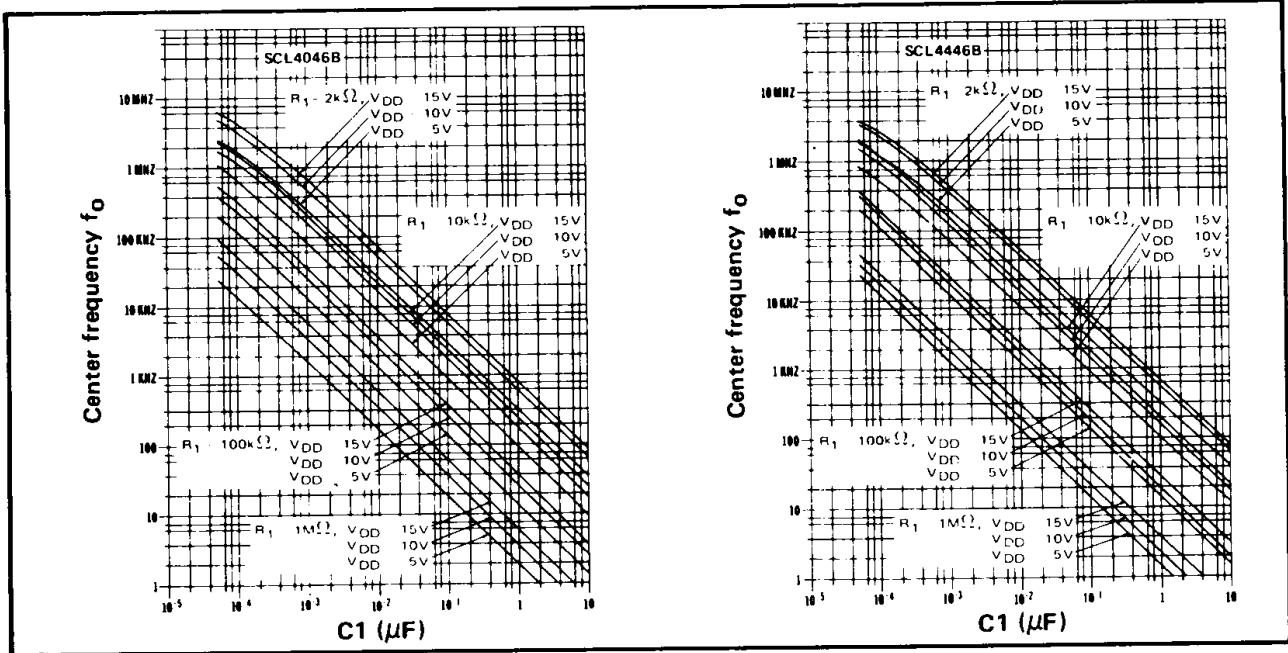


Fig. 5 (a) Typical center frequency (f_0) vs C_1 ($R_2 = \infty$, $V_{COIN} = \frac{V_{DD}}{2}$, $T_A = 25^\circ\text{C}$)

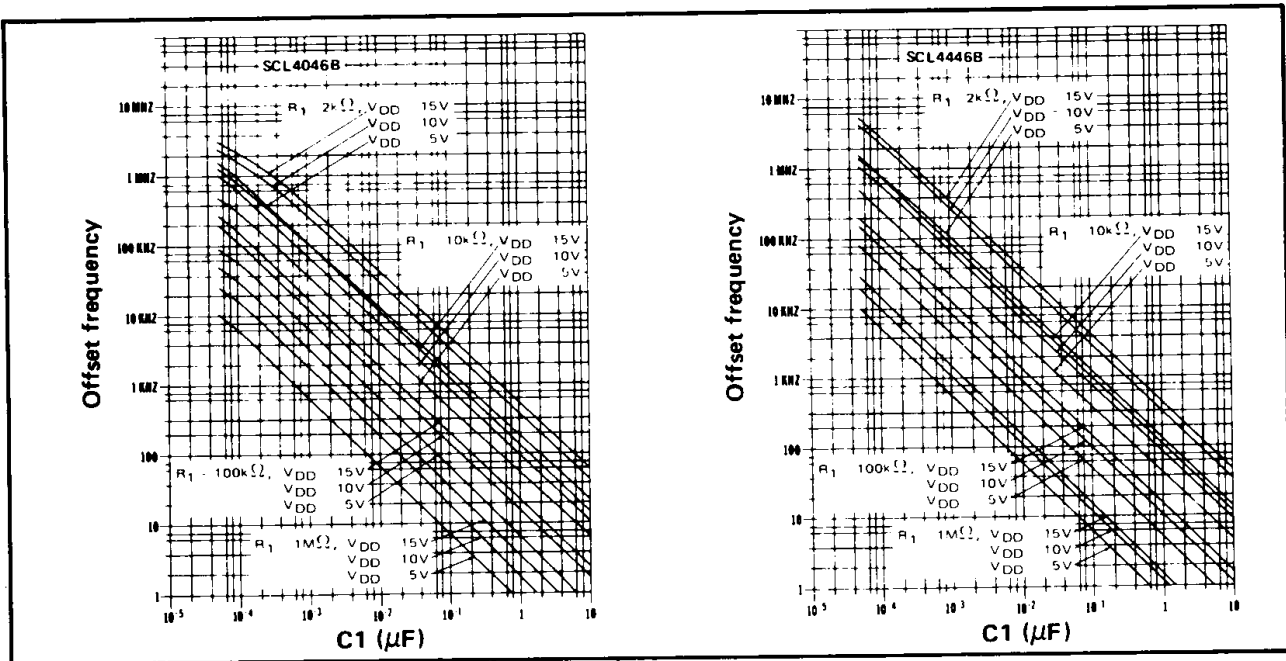


Fig. 5 (b) Typical frequency offset vs C_1 ($V_{COIN} = V_{SS}$, $T_A = 25^\circ\text{C}$)

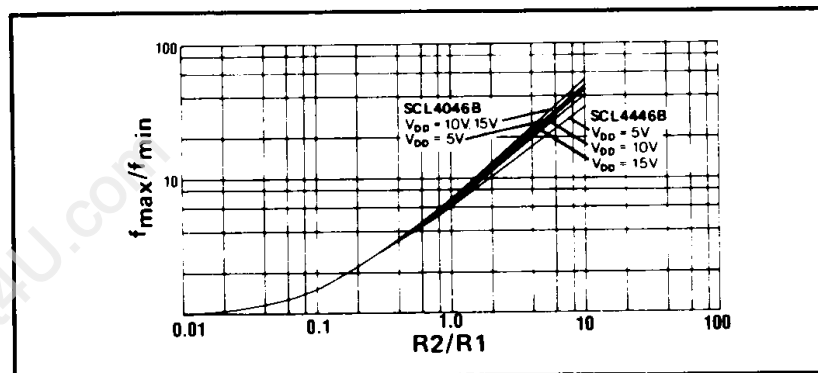


Fig. 5 (c) Typical $f_{\max}/f_{\min}$ vs R_2/R_1

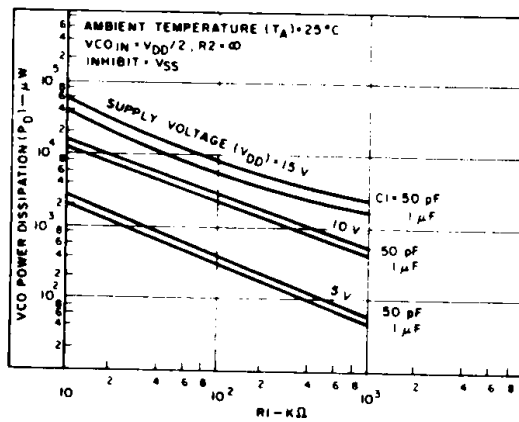


Fig. 6 (a) - Typical VCO power dissipation at center frequency vs R1.

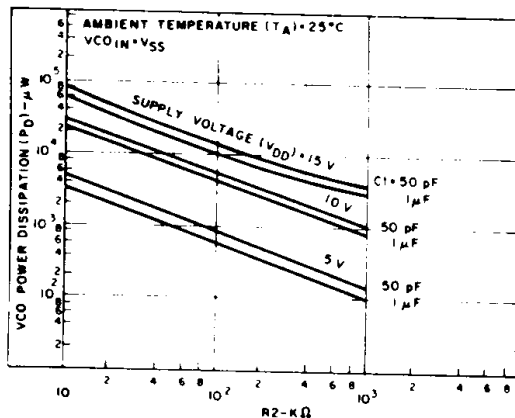


Fig. 6 (b) - Typical VCO power dissipation at f_{min} vs R2.

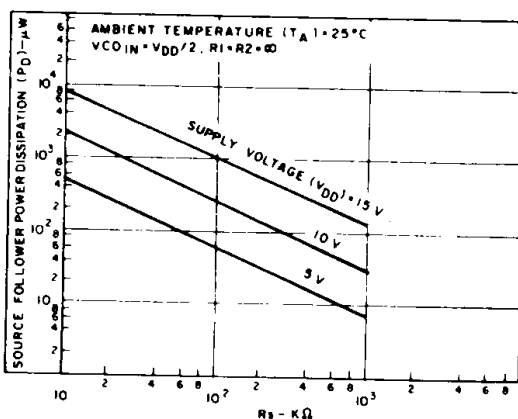


Fig. 6 (c) - Typical source follower power dissipation vs R_S .

NOTE: To obtain approximate total power dissipation of PLL system for no-signal input

$$P_D (\text{Total}) = P_D (f_0) + P_D (f_{MIN}) + P_D (R_S) \\ \text{— Phase Comparator I}$$

$$P_D (\text{Total}) = P_D (f_{MIN}) \\ \text{— Phase Comparator II}$$

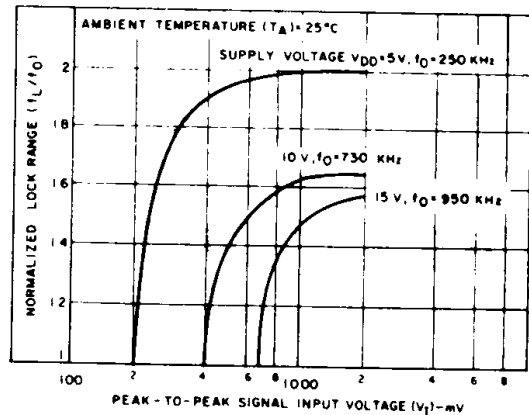


Fig. 7 - Typical lock range vs signal input amplitude

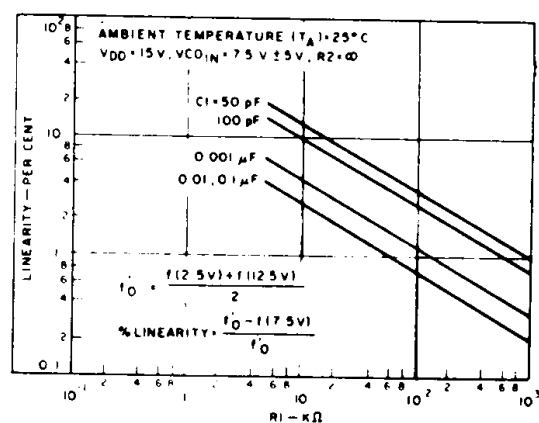
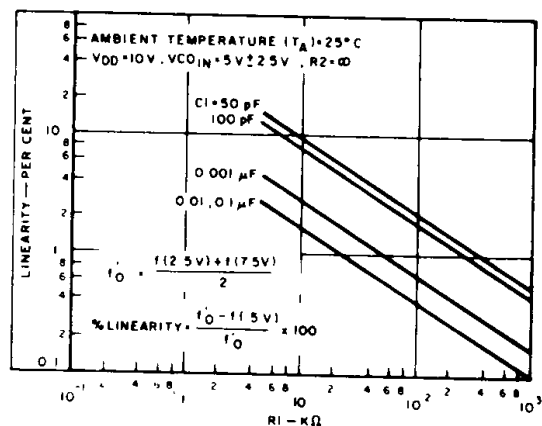


Fig. 8(a, b) - Typical VCO linearity vs R1 and C1