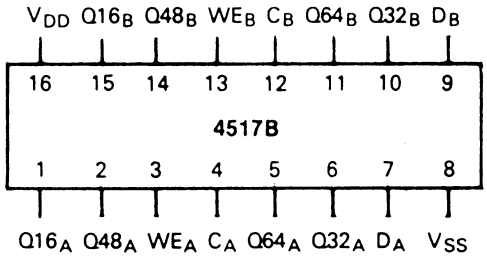
CMOS 64-BIT DUAL SHIFT REGISTER

FEATURES

- **Independent Clock, Write Enable Inputs**
- **Static Operation**
- **Positive Edge-Clocked Design**
- **6.7MHz Toggle Rate @ 10 VDC**
- **Tri-State Output at 64th Bit**
- **Balanced Output Drive Current Specifications**

CONNECTION DIAGRAM



DESCRIPTION

The SCL4517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
⌐	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 33-Bit Displayed	Content of 49-Bit Displayed	Content of 64-Bit Displayed
⌐	1	Data entered Into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 32-Bit	Data at tap entered into 48-Bit	High Impedance
¬	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
¬	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	V_{DD}	+15 to −0.5	V_{dc}
Input Voltage, all inputs	V_{IN}	V_{DD} to −0.5	V_{dc}
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range	T_A		
C		−55 to +125	°C
E		−40 to +85	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}[2]		+25°C			T_{HIGH}[2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	—	5.0	—	0.0005	5.0	—	150	μAdc
		10	All valid input	—	10.0	—	0.001	10.0	—	300	
		15	combinations	—	20.0	—	0.002	20.0	—	600	
THREE-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		—	0.1	—	—	0.2	—	1.0	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

[2] T_{LOW} = −55°C for C
= −40°C for E

T_{HIGH} = +125°C for C
= +85°C for E

SWITCHING CHARACTERISTICS* (T_A = 25°C)

CHARACTERISTIC	SYMBOL	V_{DD}	Min.	Typ. All Types	Max.	Unit
Output Transition Time (C_L = 50 pF)	t_r	5.0	—	100	200	ns
	t_{TLH}	10	—	50	100	
	t_{THL}	15	—	40	80	
Propagation Delay Time (C_L = 50 pF)	t_{PLH} t_{PHL}	5.0	—	250	500	ns
		10	—	135	270	
		15	—	110	220	
Minimum Clock Pulse Width	PW_C	5.0	—	170	250	ns
		10	—	75	100	
		15	—	60	75	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	3.0	—	MHz
		10	5.0	6.7	—	
		15	6.7	8.3	-	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	—	—	No Limit	—
		10	—	—		
		15	—	—	**	
Data to Clock Setup Time	t_{setup}	5.0	—	−40	−10	ns
		10	—	−15	0	
		15	—	0	5	
Data to Clock Hold Time	t_{hold}	5.0	—	75	120	ns
		10	—	25	50	
		15	—	10	25	
Write Enable to Clock Setup Time	t_{setup}	5.0	—	170	300	ns
		10	—	65	130	
		15	—	50	80	
Write Enable to Clock Release Time	t_{rel}	5.0	—	160	280	ns
		10	—	55	120	
		15	—	40	70	

*The formula given is for the typical characteristics only.

**When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation of the output driving stage for the output capacitance load.

AC TEST WAVEFORMS

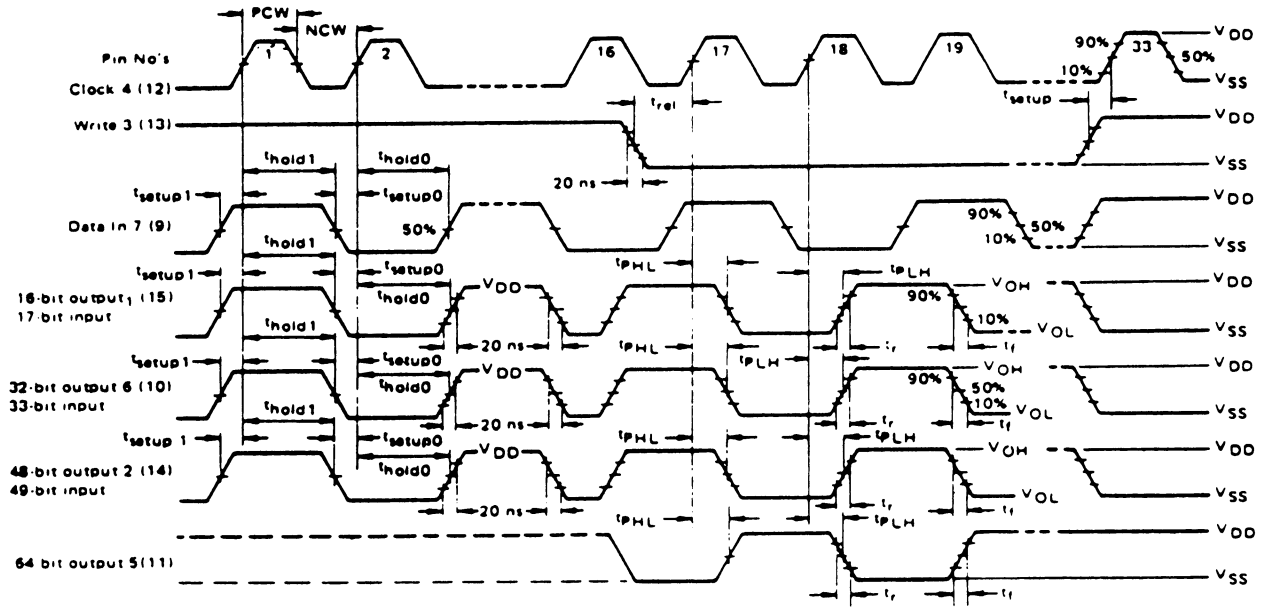
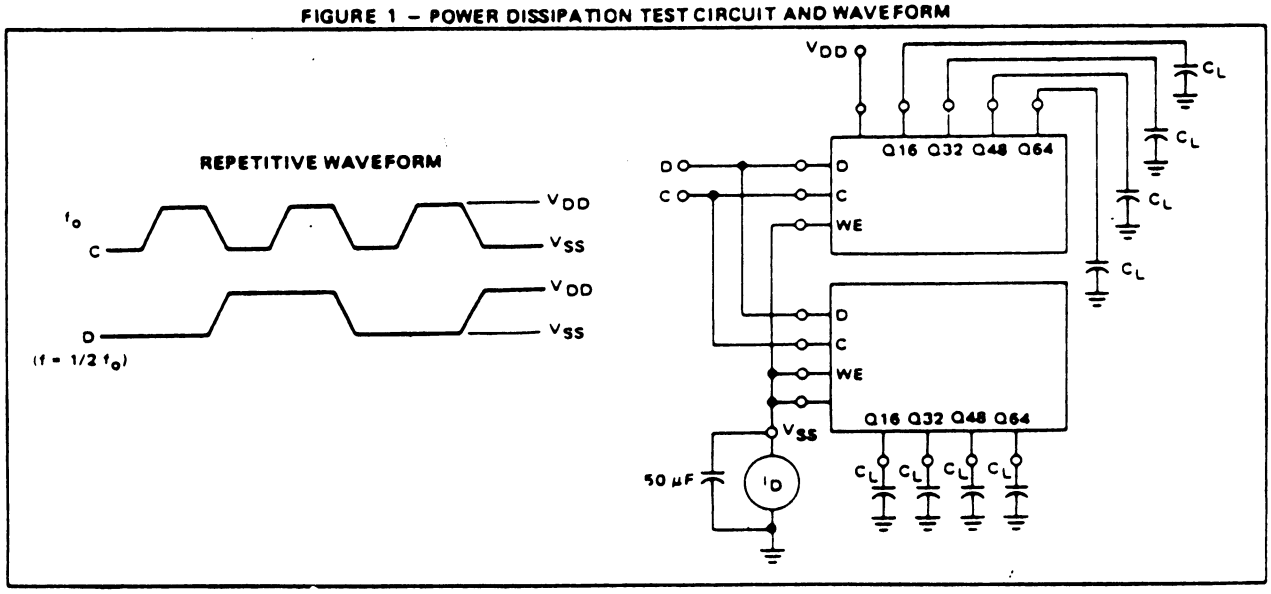


FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



EXPANDED BLOCK DIAGRAM
(1/2 OF DEVICE SHOWN)