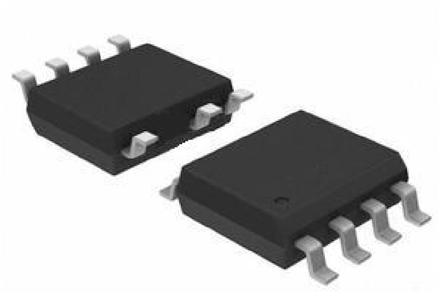
SCM1702A CC/CV Primary-Side Regulator

Features

- Primary-side regulation eliminates optocoupler
- Built-in loop compensation
- Built-in 650V start-up switch
- Built-in 650Vpower MOSFET
- Programmable cable compensation (CBC)
- Output rectifier forward drop temperature variations compensation
- Wide VDD range allows small bias capacitor
- Large capacitive loading with self-power at start-up state
- Over-voltage, over-temperature and over-current protection
- FB pin and CS pin fault protection

Package



Product package: SOP-7.

Please see “Ordering Information” for details

Applications

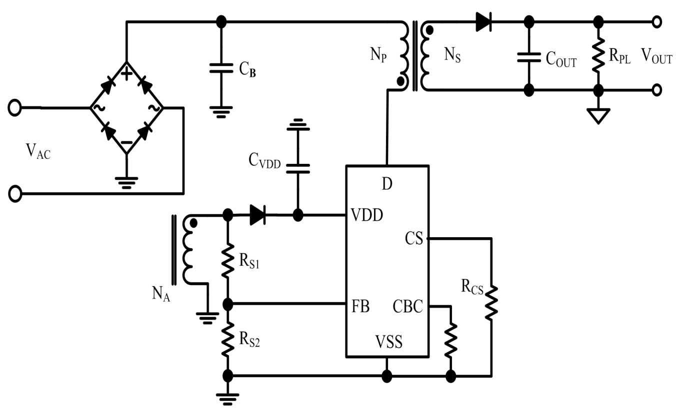
- USB-compliant adapters and chargers for consumer electronics.
- Auxiliary power supplies

Functional Description

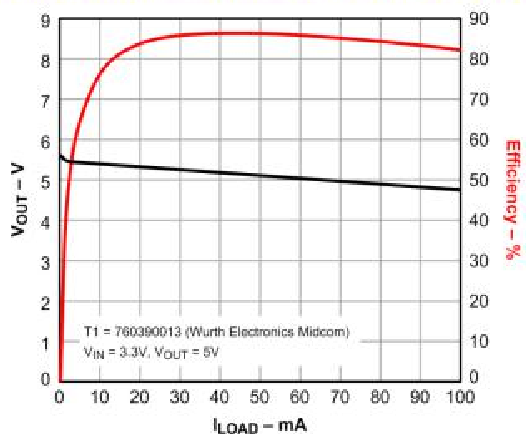
SCM1702A is a flyback primary side power supply controller. It provides isolated Constant Voltage (CV) and Constant Current (CC) output without using an opto-coupler. The devices processes information from the primary power switch and an auxiliary flyback winding for precise control of the output voltage and current. With its internal 650V startup switch, the SCM1702A can be started in a wide range of input voltage, and being supplied by the transformer auxiliary winding, the chip’s power consumption remains relatively low.

The SCM1702A controller provides high performance, output precision, advanced dynamic response and low output temperature coefficient due to numerous built-in auxiliary and compensation functions. The built-in functions include protection for over temperature, output overvoltage and over current, feedback (FB pin) and current share (CS pin) faults, so the safety requirements can be easily met.

Typical Application Circuit

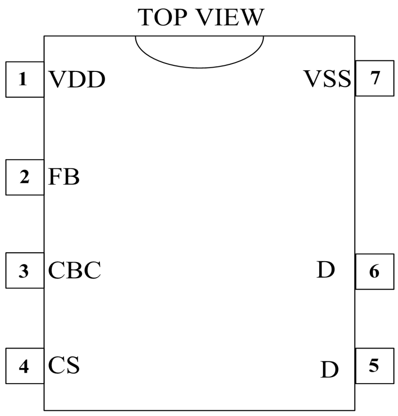


Functional Curve

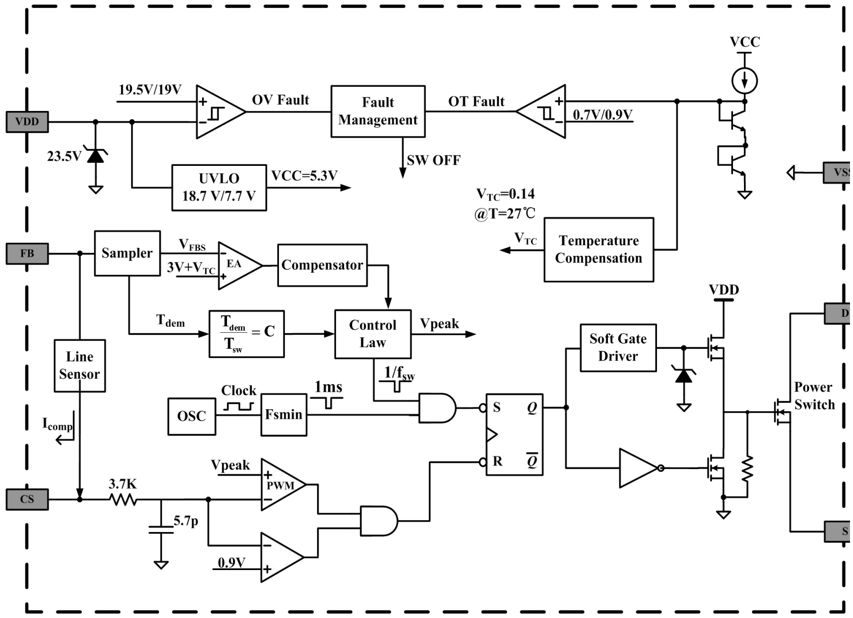


Contents

Pins



Internal Block Diagram



Pin Description

NUMBER	NAME	I/O	DESCRIPTION
1	VDD	I	The VDD input pin is the bias-supply from the transformer auxiliary winding to the controller. It requires a bypass capacitor to GND (VSS).
2	FB	I	This pin is connected to a voltage divider between an auxiliary winding and GND. The ratio of the upper resistor to the lower resistor is used to set the output voltage. The value of the upper resistor of this divider is also used to program the line compensation at the CS pin.
3	CBC	I	The cable compensation pin can be used for programming the compensation of cable voltage drop.
4	CS	I	Current sense PIN
5	D	O	This connects to the internal MOSFET drain and the high voltage (D) pin may be connect directly to the transformer, providing the charge current to the VDD capacitor for starting up the power supply.
6		O	
7	VSS	P	The VSS ground (GND) pin is both, the controller reference pin and the drive outputs low-side return. Special care must be taken to keep all AC-decoupling capacitors returns as close as possible to this pin and avoiding any lengthy common traces with analog signal return paths.

Absolute Maximum Ratings

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), voltage reference is ground.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Bias Supply Voltage, VDD	V_{DD}		22	V
D Pin Voltage	VDS	-0.6	650	V
Control pin voltage (FB, CS, CBC)	V_{FB}, V_{CS}, V_{CBC}	-0.6	6	V
Operating Junction Temperature Range	T_J	-40	150	℃
Storage Temperature Range	T_{STG}	-40	150	
Lead Temperature 0.6 mm from Case	Soldering for 10 seconds		260	
Electro Static Discharge (ESD) rating	Human Body Model （HBM）		2000	V
	Charged Device Model （CDM）		1000	
Rms Current Of Power MOSFET	I_{D1P}，I_{D2P}		1	A
Maximum Dissipation Power	P_{TOT}			mW

Important: Exposure to absolute-maximum-rated conditions for extended periods may severely affect device reliability, stress levels exceeding the "Absolute Maximum Ratings" may resu in permanent damage.

Recommended Operating Conditions

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), V_{DD}=12V，GATE=no load.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Bias supply operating voltage	V_{VDD}	9	20	V
VDD bypass capacitor	C_{VDD}	0.047	20	uF
Full Load Operating frequency	F_{SW}	68	120	kHz
Operating junction temperature	T_J	-40	125	℃

Electrical Characteristics

Test conditions: Free-air, normal operating temperature range (unless otherwise specified), V_{DD}=12V，GATE=no load.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH VOLTAGE STARTUP						
I_{STL}	Startup Current out of VDD	V_D=100V，V_{VDD}=0V，Startup current out of VDD	250	400	550	uA
I_{STH}	Startup Current out of VDD	V_D=100V，V_{VDD}=5V，Startup current out of VDD	0.8	2.5	4	mA
I_{STLKG}	Leakage Current at V_{IN}	V_{VIN}=400V, run state		1		uA
BIAS SUPPLY INPUT						
I_{VDD_STATE}	Static Supply Current	I_{GATE}=0	400	550	700	uA
UNDERVOLTAGE LOCKOUT						
V_{VDD_ON}	VDD Turn-on Threshold	V_{VDD} low to high	15	16.25	17.5	V
V_{VDD_OFF}	VDD Turn-off Threshold	V_{VDD} high to low	7.8	8.4	9	V
CS INPUT						
R_{LC}	Internal Line Compensation Resistance			2.4		kΩ
V_{CST_MAX}	Max CS Threshold Voltage		0.77	0.8	0.83	V
V_{CST_MIN}	Min CS Threshold Voltage		0.26	0.27	0.28	V
K_{AM}	PWM Control Ratio	V_{CST_MAX} / V_{CST_MIN}		3		V/V
K_{LC}	Line Compensation Current Ratio	FB pin output current/ CS pin output current		23/2		A/A
K_{DS}	Maximum Ratio of T_{DS}/T	V_{FB}=2V		0.5		S /S
FB INPUT						
V_{FBR}	Regulating Level	Measured at no-load condition	3.77	3.808	3.846	V
V_{FBNC}	Negative Clamp Level	I_{FB} = -300 μA		-35		mV
CABLE COMPENSATION						
V_{CFB_MAX}	Maximum Cable Compensation Voltage	V_{CBC} = 0V, at full load		277		mV
V_{CFB_MIN}	Minimum Cable Compensation Voltage	V_{CBC} = open, at full load		37.8		mV
Timing						
T_{FB_LEB}	FB Sample Blanking Time			1.4		uS

$F_{SW\_start-up}$	Startup Frequency	VFB=2V	17.8	20.9	24.0	kHz
F_{SW_MIN}	Minimum Switching Frequency	V_{FB}=V_{FBR}	558	656	754	Hz
T_{ON_MAX}	Maximum Gate On-Time	CS connect to GND	10.2	12.2	14.2	uS
T_{PD}	Protection Delay Time	FB, CS fault or over-temperature state or V_{FBS}=V_{OVP}		6		T_{SW}
$T_{VDD\_STOP\_MAX}$	Maximum Startup Switch Supply Time			3072		T_{SW}
PROTECTION						
V_{OVP}	Over voltage Threshold	At FB input, T_J = 25 °C	4.12	4.32	4.52	V
V_{CSF}	Over current Threshold	At CS input	1.52	1.60	1.68	V
T_{J_STOP}	Thermal Shutdown Temperature	Internal junction temperature		155		℃
$T_{J\_RESTART}$	Thermal Restart Temperature	Internal junction temperature		98		℃
DRIVERS						
I_{GTS}	Internal GATE source current	V_{VDD}=15V，C_{GS}=1nF		50.2		mA
V_{GT_CLAMP}	Internal GATE clamp voltage		16.2	17.4	18.6	V
R_{DS_ON}	Power MOS ON-State Resistance	V_{GS} =10V, I_D =0.5A	-	-	16	Ω
V_{BR_DSS}	Power MOS Breakdown Voltage	V_{GS} =0V, I_D =250μA	650	-	-	V
I_{DSS}	OFF-State Current	V_{DS} =650V, V_{GS} =0V	-	-	1	uA

note 1：T_{SW} is switching cycle, typical value of T_{PD} is 6 times the T_{SW}。

Typical Curve

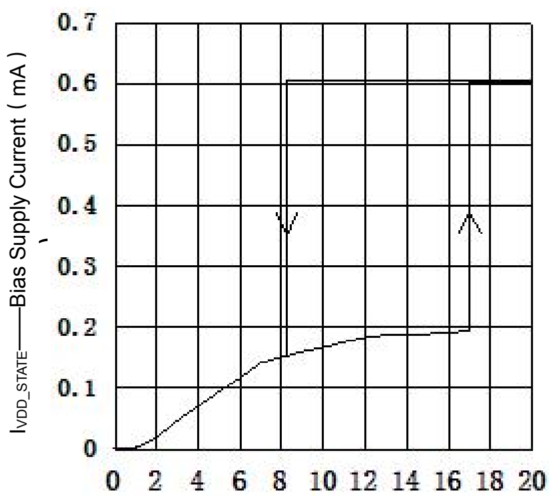


Fig. 1 Bias Supply Current vs. Bias Supply Voltage

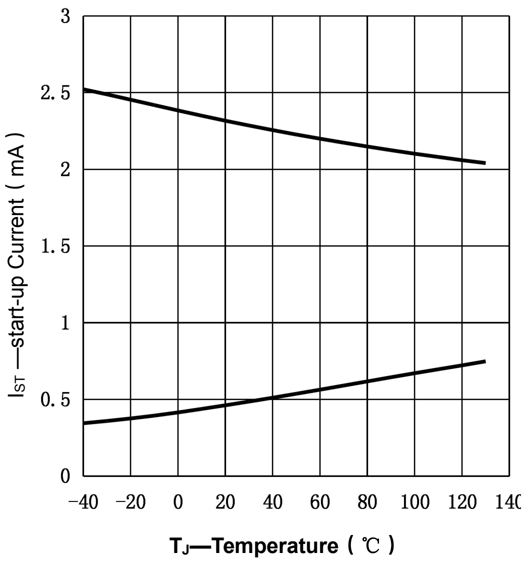


Fig. 2 Start-up Current vs. Temperature

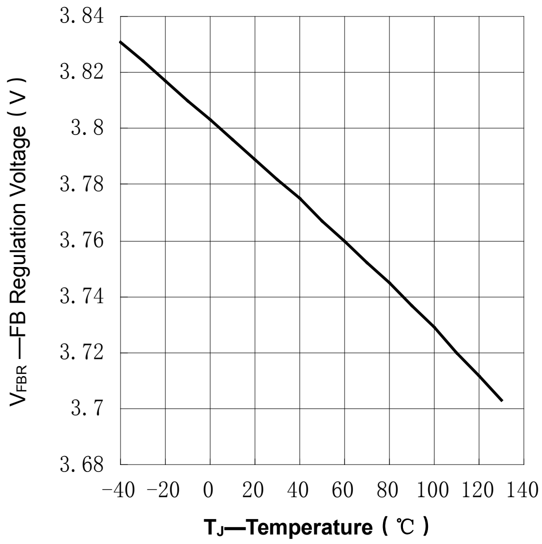


Fig. 3 FB Regulation Voltage vs. Temperature

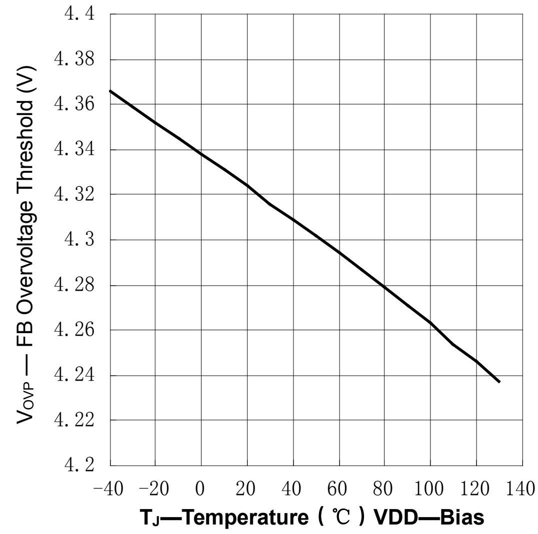


Fig. 4 FB Over-voltage threshold vs. Temperature

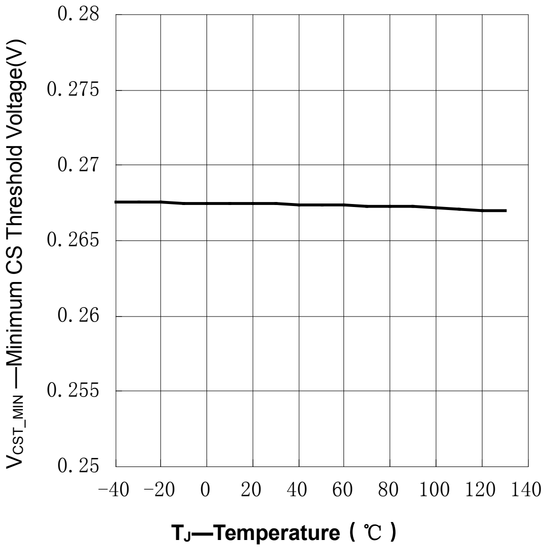


Fig. 5 Minimum CS Threshold vs. Temperature

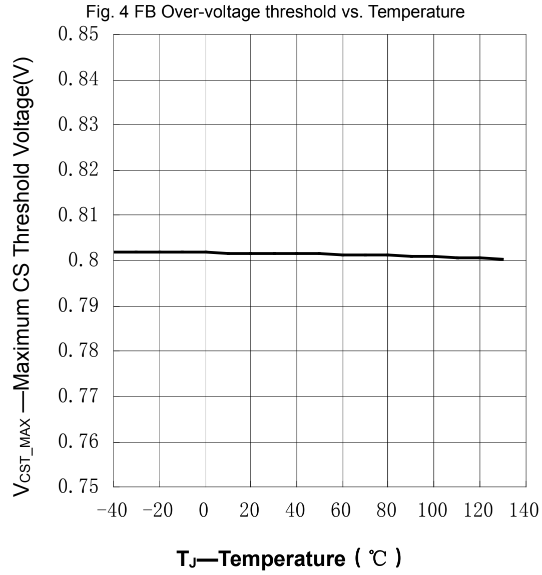


Fig. 6 Maximum CS Threshold vs. Temperature

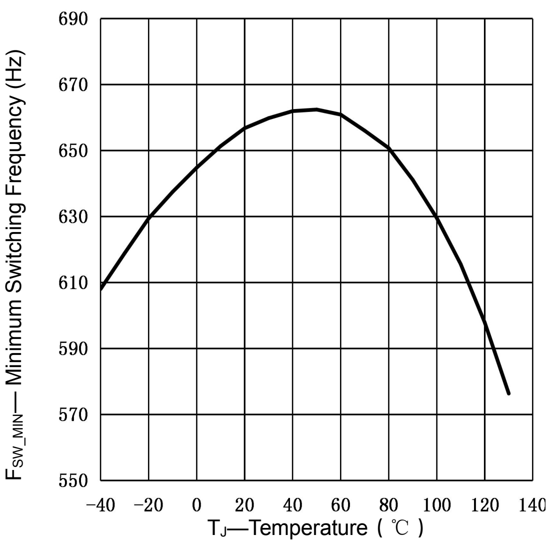


Fig. 7 Minimum Switching Frequency vs. Temperature

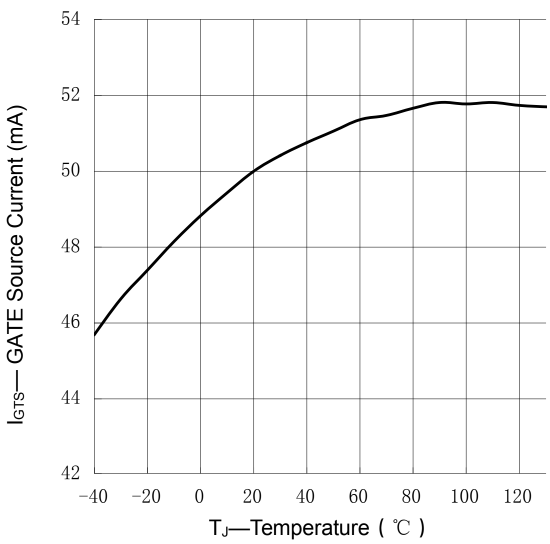


Fig. 8 GATE Source Current vs. Temperature

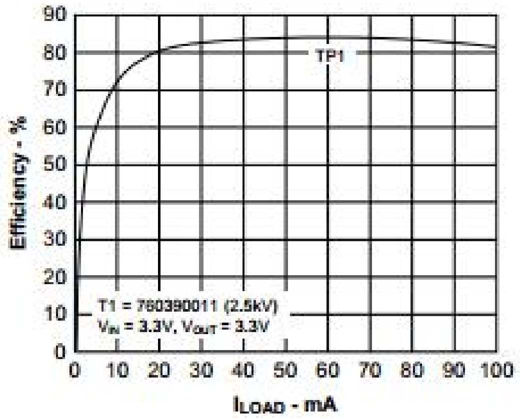


Fig. 9 Efficiency vs. Load Current

Parameter Test Information

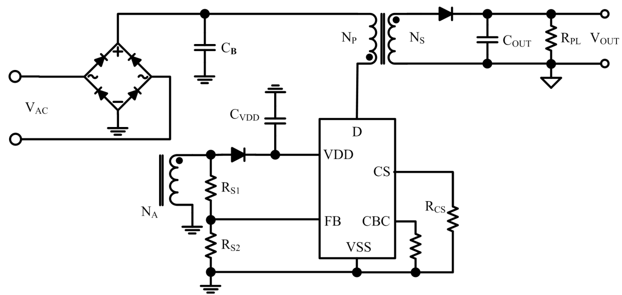


Fig. 10 Functional Curve Test Circuit

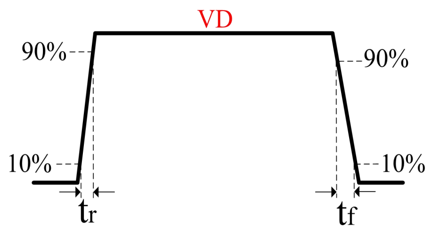


Fig. 11 Definition Of Rise Time and Fall Time

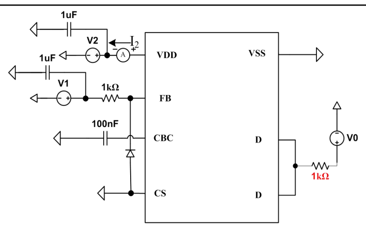


Fig. 12 Switching Character Test Circuit

Transformer Work Mode

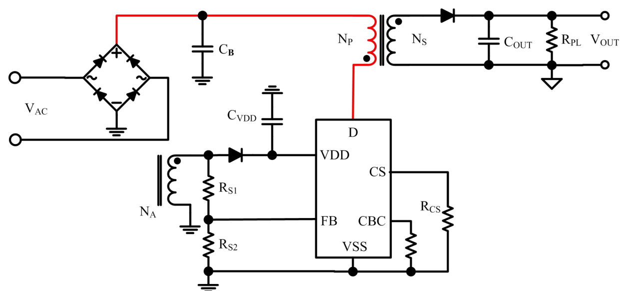


Fig. 13 Magnetization Phase Of Flyback Converter

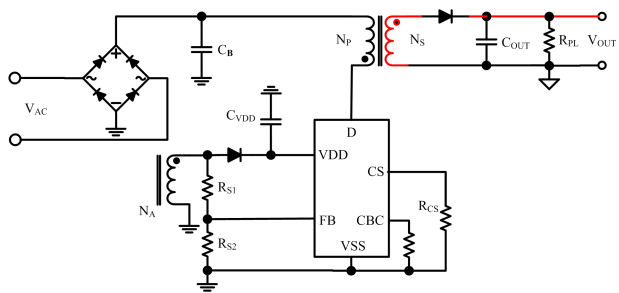


Fig. 14 Demagnetization Phase Of Flyback Converter

Detailed Application Description

SCM1702A integrated an 1A/650V Power MOSFET, with typical application is PSR flyback converter, as shown in Fig. 15. By sensing the auxiliary coil's voltage, you can sense the output voltage of converter, and realize loop control. You can set the ratio of the resistor Rs1 and Rs2 or the ratio of the turns NS and NA, to set the converter's output voltage. The feedback voltage feed to the pin FB. By the way, you can also set the cable compensation voltage using a suitable resistor. And with a suitable sensing resistor to the pin CS, you can set the power level of the converter, ie limited current.

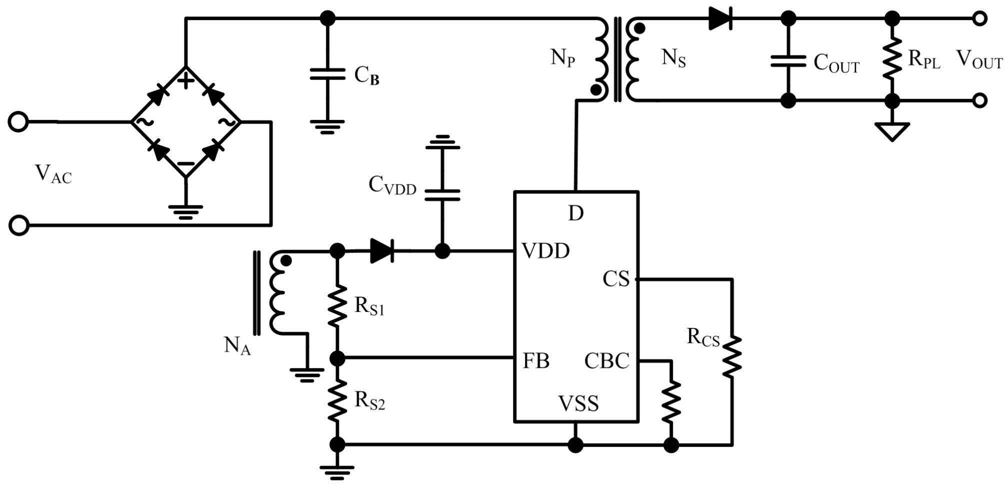


Fig. 15 Typical Application Circuit

High Voltage Startup Operation

An internal high voltage startup switch is connected to the primary side of the transformer and continuously charges the VDD capacitor from the voltage of the bulk capacitor C_B, see also Fig. 16.

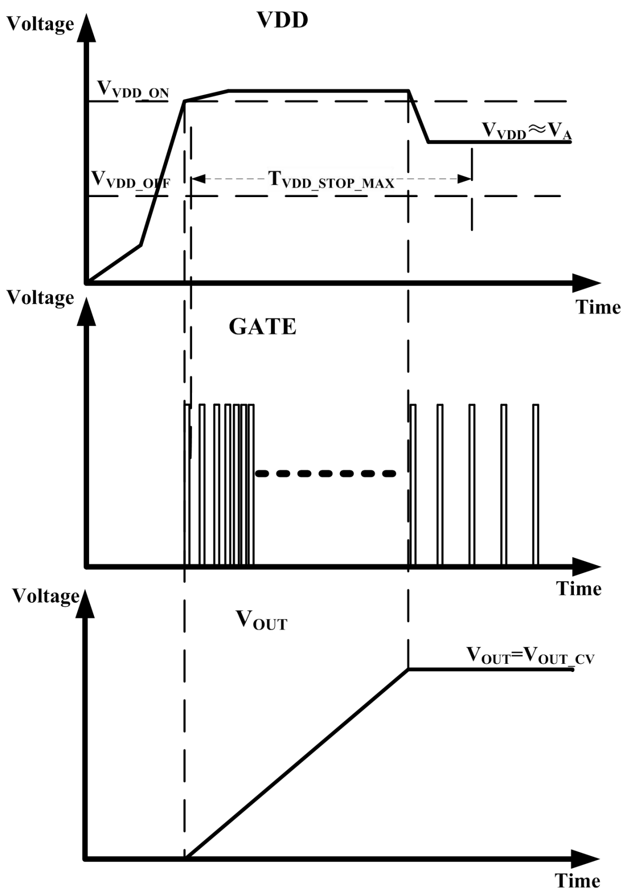


Fig. 16: Startup timing

When the VDD voltage is below 2.4V, the built-in startup circuit charges the VDD capacitor with lower current I_{STL}. When the VDD voltage exceeds 2.4V, the built-in startup circuit charges the VDD capacitor with higher current I_{STH}. When VDD reaches V_{VDD_ON} the controller is enabled, the converter starts switching, the high voltage startup switch continues charging the VDD capacitor until the VDD voltage is 20.8V. The VDD voltage starts to drop once the controllers run state current becomes larger than the high limit of the startup current. The controller is self-power and independent from VDD voltage changes. The maximum self-powered on time of the supply is $T_{VDD\_STOP\_MAX}$ and self-power stops either when the converter output voltage reaches the target voltage V_{OUT_CV} or the converter into protected state. Refer to Electrical Characteristics for I_{STL}, I_{STH}, V_{DD_ON} and $T_{VDD\_STOP\_MAX}$ values.

Over Current point (constant current point) Design

The SCM1702A controller sets the ratio (K_{DS}) between the demagnetization time T_{DEM} and the switching period T_{SW}. The secondary average output current I_{O_MAX} is determined by the primary peak current, the turns-ratio, the demagnetization time T_{DEM} and the switching period T_{SW}:

$$I_{O\_MAX} = \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot K_{DS} \cdot \eta_{XFMR} \cdot I_{PEAK\_MAX} \quad (1)$$

where

N_P/N_S is the transformer primary to secondary turns-ratio (a typical ratio for 5V output is 13 to 15)
K_{DS} is the ratio of the demagnetization time and the switching period T_{DEM}/T_{SW}
η_{XFMR} is the transformer efficiency at full power
I_{PEAK_MAX} is the maximum of primary peak current.
The over current point design of the transformer is modulated through N_P/N_S and I_{PEAK_MAX}.
In CC mode, the controller defined the K_{DS} ratio (ratio of demagnetization time T_{DEM} and switching period T_{SW}). The over current point is confirmed, once the parameters of the transformer and the maximum primary peak current are established.

$$I_{PEAK\_MAX} = \frac{V_{CST\_MAX}}{R_{CS}} \quad (2)$$

Example: With a transformer core and winding loss of 5%, a primary to secondary leakage inductance of 3.5% and bias power to output power ratio of 0.15%, the η_{XFMR} value at full power is approximately: η_{XFMR} = 1-0.05-0.035-0.015 = 0.9.
A converter design of 5V/0.6A (3W) has an over current capacity of 10% and a transformer primary to secondary turns ratio of 14. The current sense resistor value is calculated as follows：

$$\begin{aligned} R_{CS} &= \frac{V_{CST\_MAX}}{2I_{O\_MAX}} \cdot \frac{N_P}{N_S} \cdot K_{DS} \cdot \eta_{XFMR} \quad (3) \\ &= \frac{0.8}{2 \times 0.66} \times 14 \times 0.5 \times 0.9 \\ &\approx 3.8\Omega \end{aligned}$$

Output Voltage Design

The waveform of the auxiliary winding consists of three parts as shown in Fig. 17. The first part is the MOSFET switch on time T_{ON}, where the voltage is V_{BULK}/N_{PA}. The second part is demagnetization time T_{DEM}, the voltage is (V_{OUT}+V_F) N_{AS}. The third part is primary inductance and capacitance resonance time T_{RING}.

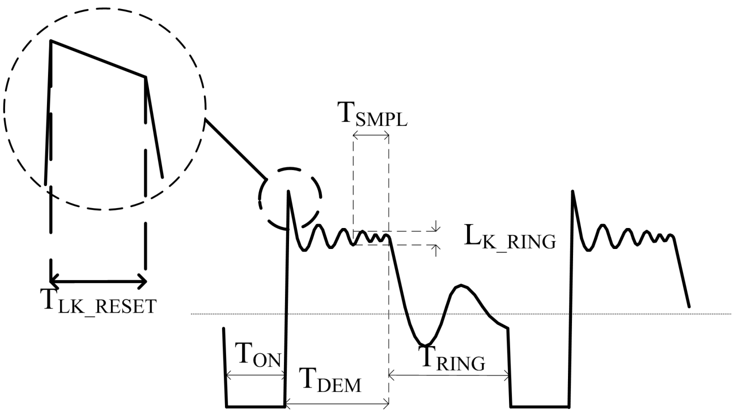


Fig. 17: Auxiliary winding, detailed waveform

The SCM1702A includes an FB signal sampler, employing signal discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are however some details of the auxiliary winding signal to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. A detailed illustration of waveform and criteria to ensure a reliable sample on the FB pin is shown in Fig. 17. The first detail to observe is the duration of the leakage inductance reset pedestal $T_{LK\_RESET,}$ because this can mimic the waveform of the secondary current decay, followed by a sharp downslope. It is important to keep the leakage reset time smaller than the FB sample blank time T_{FBLEB}. The second detail observed is the amplitude of ringing on the V_{AUX} waveform following T_{LK_RESET}. The peak to peak voltage at the FB pin should be less than approximately 100mVp-p at least 200 ns before the end of the demagnetization time.In constant voltage mode, the output voltage has the following relation:

$$V_{OUT\_CV} = \frac{N_S}{N_A} \cdot (1 + \frac{R_{S1}}{R_{S2}}) \cdot V_{FBR} - V_F \quad (4)$$

Where

N_P/N_S is the transformer primary to secondary turns-ratio
R_{S1} is the high-side resistor value of the VS divider
R_{S2} is the low-side resistor value of the VS divider
V_{FBR} is the CV regulation level at the VS input (see the table),
V_F is the output rectifier forward drop at near zero current.

During CV regulation, the frequency and amplitude modulation modes are shown in Fig. 18, where I_{PP} and F_{SW} is normalized curves relative to the output of the error amplifier. The FB feedback signal is filtered by a compensation filter and results in the output of the error amplifier. The value of the output of EA is approximately equal to FB voltage at steady state. The controller limits the maximum switching frequency F_{SW_MAX} and the minimum switching frequency F_{SW_MIN} (see electrical characteristics). The recommended operating switching frequency is between 68kHz and 110kHz and higher switching frequencies affect the converters efficiency and EMI performance. The maximum switching frequency is defined by the primary inductor and the primary peak current (see also switching frequency design).

The FB sampling time T_{FBLEB} is fix at 1.4us. The minimum demagnetization time T_{DEM} is the smallest under light load peak current. Therefore the design must ensure that under light load condition, T_{DEM} minimum is greater than the FB sampling time T_{FBLEB}. As shown in the formula (5), it is recommended to set T_{DEM_MIN}>2*T_{FBLEB}.

$$T_{DEM\_MIN} = \frac{L_m \cdot \frac{V_{CST\_MIN}}{R_{CS}}}{\frac{N_P}{N_S} \cdot V_{OUT}} \geq 2 \cdot T_{FBLEB} \quad (5)$$

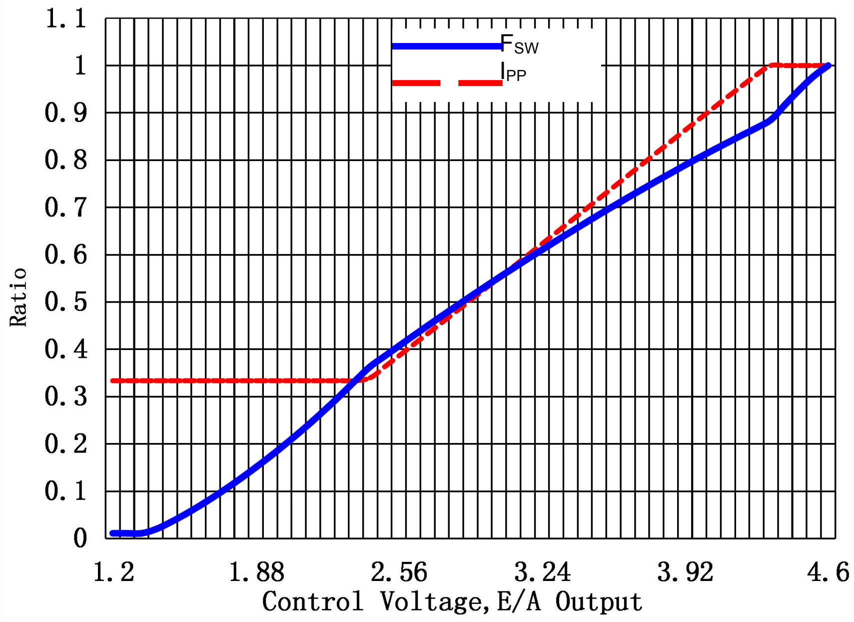


Fig. 18: Frequency and Amplitude Modulation Modes

Cable Compensation (CV mode only)

With cable compensation in CV mode, the converter can provide more accurate output voltage across the entire load range. With load variation, the level of the FB pin regulation voltage V_{FBR} will change and compensate for the voltage drop across the cable. The compensation amount is determined by the output of the error amplifier (EA) which is related to the load. The increment voltage V_{CFB} on regulating level voltage V_{FBR} has the relationship like that:

$$V_{CFB} = \left(\frac{V_{EA} - V_{GSN}}{66.1k\Omega + (14.9k\Omega + R_{CBC})||264.3k\Omega} - 4uA\right) \times \frac{2}{5} \times 24.4k\Omega \quad (6)$$

where

V_{EA} is the output of the error amplifier. V_{EA}≈4.6V at maximum load, and V_{EA}≈1.5V at minimum load

V_{GSN} is the N-MOSFET gate to source voltage. V_{GSN}≈2V at maximum load and V_{GSN}≈1.1V at minimum load

R_{CBC} is a resistor between CBC pin and ground

When the CBC pin is open (R_{CBC}=∞), V_{CFB_MIN} = 37.8mV at maximum load and the sample voltage on the FB pin is stable at V_{FBR}+V_{CFB_MIN}. When the CBC pin is connected to ground (R_{CBC}=0), V_{CFB_MAX} = 277mV at minimum load and the sample voltage on the FB pin is stable at V_{FBR}+V_{CFB_MAX}.

Temperature Compensation

In offline flyback converters, the secondary side rectifiers used are generally diodes and their forward voltage drop has a negative temperature coefficient which will reduce the output voltage accuracy in PSR.

SCM1702A has an integrated temperature compensation. By detecting the forward voltage of a PN junction in the chip, a voltage V_{BE} results. Then the voltage V_{BE} is reduced to 1/3 and results in compensation voltage V_{TC}. This V_{TC} voltage is being overlaid over the FB pin regulation voltage level. V_{TC} also includes negative temperature coefficient, thus compensating for the diode forward voltage drop.

The specified value of V_{FBR} in electrical characteristics, is compensated for temperature internally. Therefore V_{FBR} in equation (5) can be used to directly calculate the output voltage.

Switching Frequency

Once the constant current and over current points are established, then both the maximum primary peak current I_{PEAK_MAX} as well as the over power point Po_max are confirmed. The maximum the switching frequency of the converter is calculated as follows:

$$F_{SW\_MAX} = \frac{2 \cdot P_{O\_MAX}}{L_M \cdot I_{PEAK\_MAX}^2 \cdot \eta_{XFMR}} \quad (7)$$

Modulate L_M to acquire F_{SW_MAX}. SCM1702A's maximum frequency limited to 168kHz.

Line Sensor Compensation

The waveform of the auxiliary winding consists of three parts as shown in Fig. 10: First part is the MOSFET switch on time T_{ON}, where the voltage is V_{BULK}/N_{PA}. Second part is demagnetization time T_{DEM}, the voltage is $(Vo+V_F)\ N_{AS}$. Third part is primary inductance and capacitance resonance time T_{RING}. According to the flyback converter concept, the voltage is V_{BULK}/N_{PA} when the MOSFET switch is on and T_{ON} time and T_{DEM} time are two separate parts. The line sensor uses the FB pin voltage during T_{ON} time.

This patented method (patent pending), simply works by clamping the FB voltage with a NPN bipolar transistor during the MOSFET on-time. This pin also senses the FB current generated through R_{S1} by the reflected bulk capacitor voltage to provide run and stop thresholds for AC-input and to compensate the current sense threshold across the AC input range. The line sensor current is given by:

$$I_{COMP} = \frac{1}{K_{LC}} \cdot \frac{\frac{N_A}{N_P} \cdot V_{IN} - V_{FBNC}}{R_{S1}} \quad (8)$$

The line sensor voltage V_{RLC} realizes the feed forward compensation and ensures the consistency of the over current point at the high and low voltage level. The voltage of the feed forward resistance RLC can be calculated by the following formula:

$$V_{RLC} = I_{COMP} \times R_{LC} = \frac{V_{IN} \times T_D}{L_P} \times R_{CS} \quad (9)$$

T_D is the total current sense delay consisting of the MOSFET turnoff delay, plus an internal delay of approximately 50ns
L_P is the transformer primary inductance
V_{FANC} is the negative clamp level of the FB pin (see electrical characteristics)
K_{LC} is line compensation current ratio (see electrical characteristics)
R_{LC} is the value of the SCM1702A controllers internal line sensor resistor (see electrical characteristics)

Fault Protection

SCM1702A controller provides extensive fault protection including the following:
Output short to ground protection
Output over voltage protection
FB pin fault protection
CS pin fault protection
Internal over temperature protection

NOTE: The following Fig.s 18 and 19 show the controller just after start-up. VDD is the voltage at the VDD pin, C_{VDD} is the VDD bypass capacitor and V_{GATE} is the pulsating voltage of the gate driver.

Output Short protection

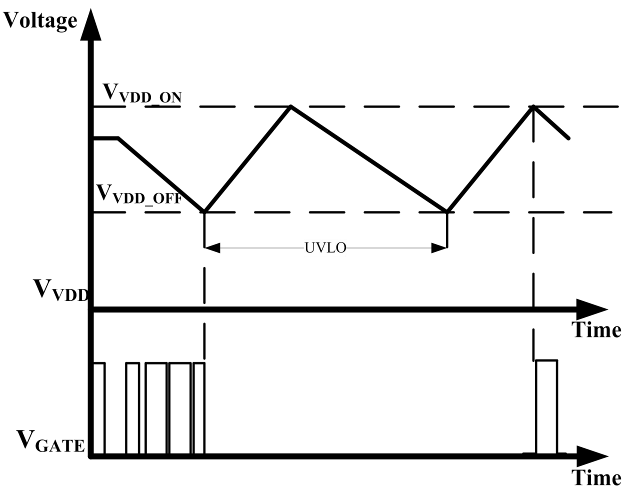


Fig. 19 Timing and waveform with output short circuit

During the first stage shown in Fig. 19, the controller can't get power from auxiliary winding if the output is shorted, then the VDD bypass capacitor voltage starts to drop, the controller can't output any gate pulse until the VDD bypass capacitor voltage drops to $V_{DD(OFF)}$ level (see electrical characteristics).

In the second stage, the controller stops to generate gate pulses when $V_{VDD}=V_{VDD\_OFF}$, the internal high voltage startup device is active until $V_{VDD}=V_{VDD\_ON}$. The typical startup current I_{STH} (see electrical characteristics) provides fast charging of the VDD capacitor. The controller's power consumption causes V_{VDD} to fall below V_{DD_OFF} again and the GATE can't output a driver signal during this time. The second stage time is longer than the first stage because the power consumption is smaller.

In the third stage, the device returns to the start state and a startup sequence is initiated. The internal high voltage startup device is active until $V_{VDD}=V_{VDD\_ON}$.

If the output to ground short remains, the above process, also called UVLO process, repeats itself periodically until the short circuit is removed.

The over current point is limited by the chip, meaning that if the converter is over loaded, then the output voltage will drop to maintain the output power constant. The controller cannot get any power from the auxiliary winding because the output has dropped to the lower limit and the controller will repeat the same process.

Output Overvoltage Protection

The output overvoltage function is determined by the voltage feedback on the FB pin V_{FBS}. If the stage when $V_{FBS} \geq V_{OVP}$ exceeds the T_{PD} delay time, the device stops switching and the internal current consumption will let the VDD capacitor voltage drop to V_{VDD_OFF}. Consequently, the device returns to the start state and enters a startup sequence as shown in Fig.20.

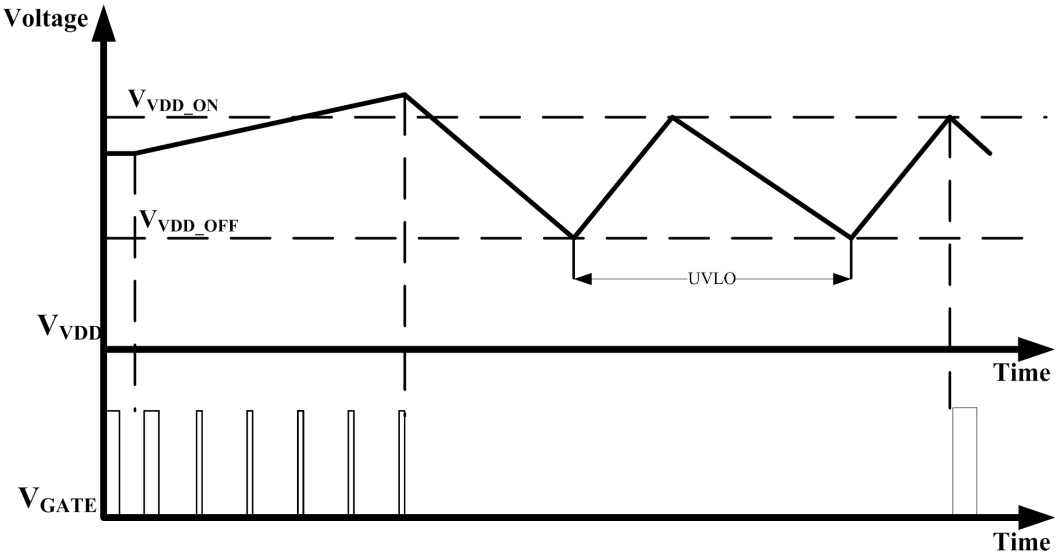


Fig. 20: Timing and waveform of output over voltage protection

Fault Protection, FB Pin

If the FB is short cut,open circuit or R_{S2} is disconnected for the duration of the delay time T_{PD}, the SCM1702A will stop switching. Then the SCM1702A goes into an UVLO reset/restart sequence.

Fault Protection, CS Pin

The SCM1702A always operates with cycle-by-cycle primary peak current control with a normal operating voltage range of the CS pin between 0.8V and 0.27V. Once An the CS pin voltage reaches 1.6V for the duration of the delay time $T_{PD,}$ an additional protection that is not filtered by leading-edge blanking sets in, which the results in an UVLO reset/restart sequence of the controller.

Over Temperature Protection

The device initiates an UVLO reset cycle if the junction temperature reaches the internal over temperature-protection threshold T_{J_STOP} as described in Electrical Characteristics. When the temperature remains the threshold at end of the UVLO cycle, the protection cycle repeats itself and only once the temperature falls below $T_{J\_RESTART}$ (see electrical characteristics), the device exits the protection mode and resumes normal operation.

Ordering Information

Part Number	Package Type	No. of Pins	Silk Screen Marking	Reel information
SCM1702ASA	SOP-7	7	SCM 1702ASA YM	3K/REEL

Product marking

SCM1702XYZ：

(1) SCM1702 = Product designation.

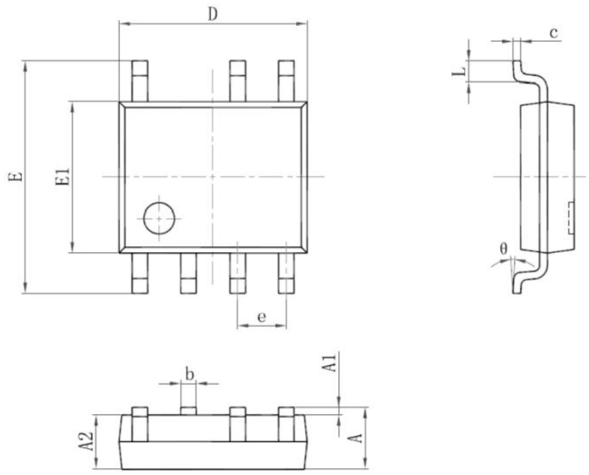
(2) x = Version information (Letter from A-Z).

(3) y = Package definition; (S = SOP package).

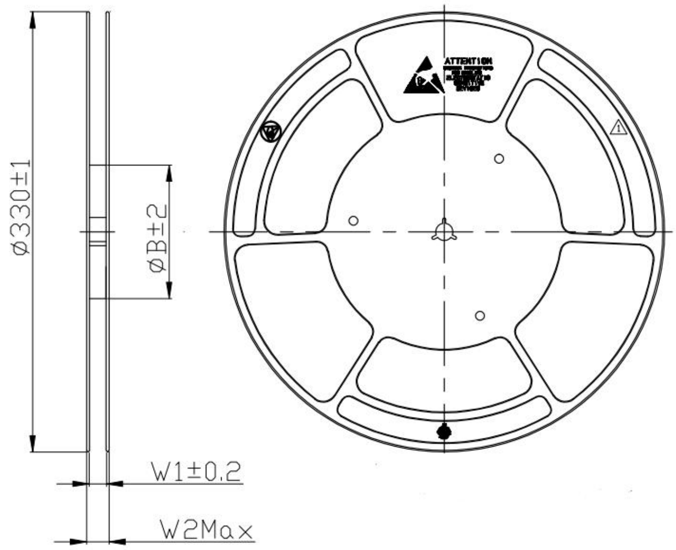
(4) Z = Operating temperature range (C = 0℃ to +70℃, I =-40℃ to +85℃, A =-40℃ to +125℃, M = -55℃ to +125℃) .

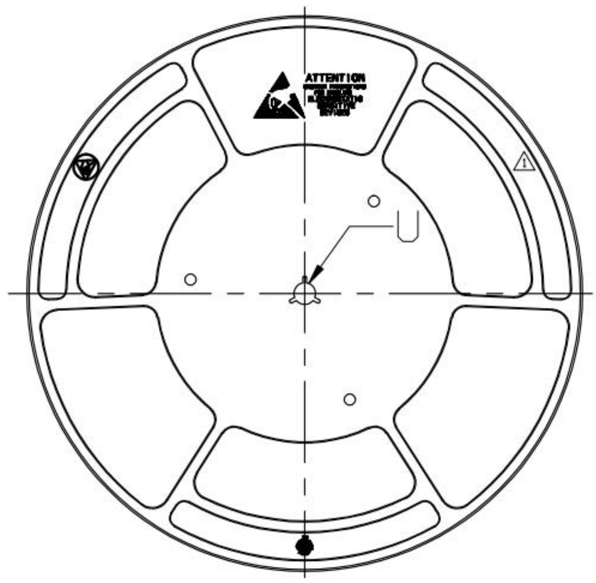
(5) YM = Date code for product traceability; Y = code for production year; M = code for production month.

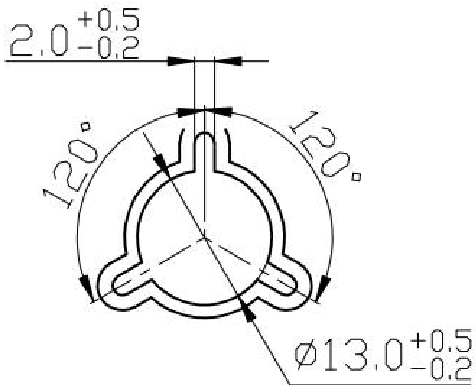
Mechanical Package Information



SOP-7				
Symbol	Dimensions in millimeters		Dimensions in inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
e	1.270（BSC）		0.050（BSC）	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	0.800	0.016	0.032
θ	0°	8°	0°	8°


ATTENTION
Ø330±1
ØB±2
W1±0.2
W2Max


ATTENTION
U


2.0 +0.5 -0.2
120°
120°
Ø13.0 +0.5 -0.2

U
4 : 1

Basic Disk Dimensions（mm）				
Package Type	Load Band Width	B	W1	W2Max
SOP-7	12	180	12.4	18.4

Technical requirement：

1. Color：Blue（Reference color number：
   PANTONE DS 196-1 C ; C100 M70 Y0 K0
   PANTONE DS 197-1 C; C100 M70 Y0 K10
   PANTONE DS 205-1 C; C100 M60 Y0 K20
   PANTONE DS 205-2 C; C85 M50 Y0 K20
   PANTONE DS 206-2 C; C85 M50 Y0 K35
   PANTONE DS 219-1 C; C90 M50 Y5 K15）
2. Dimensions and tolerances according to ANSI/EIA-481-C-2003;
3. Disk surface good finish, no warping deformation；
4. External packing in good condition, no damage or pollution.

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