300 mA CMOS Low Dropout Regulator

SCP114

The SCP114 is 300 mA LDO that provides the engineer with a very stable, accurate voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the SCP114 employs the dynamic quiescent current adjustment for very low I_Q consumption at no-load.

Features

- Operating Input Voltage Range: 1.7 V to 5.5 V
- Available in Fixed Voltage Options
- Very Low Quiescent Current of Typ. 50 μA
- Standby Current Consumption: Typ. 0.1 μA
- ±1% Accuracy at Room Temperature
- High Power Supply Ripple Rejection: 75 dB at 1 kHz
- Thermal Shutdown and Current Limit Protections
- Stable with a 1 μF Ceramic Output Capacitor
- Available in UDFN 1.0 mm x 1.0 mm Package
- These are Pb-Free and Halide-Free Devices

Typical Applications

- PDAs, Mobile phones, GPS, Smartphones
- Wireless Handsets, Wireless LAN, Bluetooth®, Zigbee®
- Portable Medical Equipment
- Other Battery Powered Applications

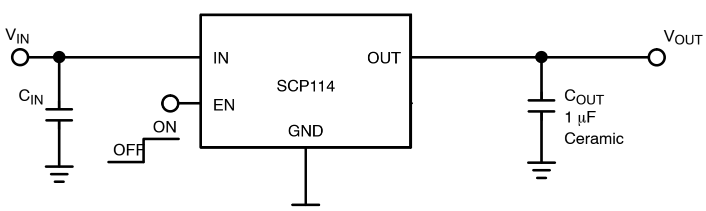
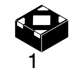
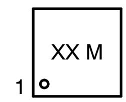


Figure 1. Typical Application Schematic



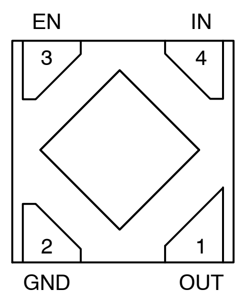
UDFN4
MX SUFFIX
CASE 517CU

MARKING DIAGRAMS



XX = Specific Device Code
M = Date Code

PIN CONNECTIONS



(Bottom View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 14.

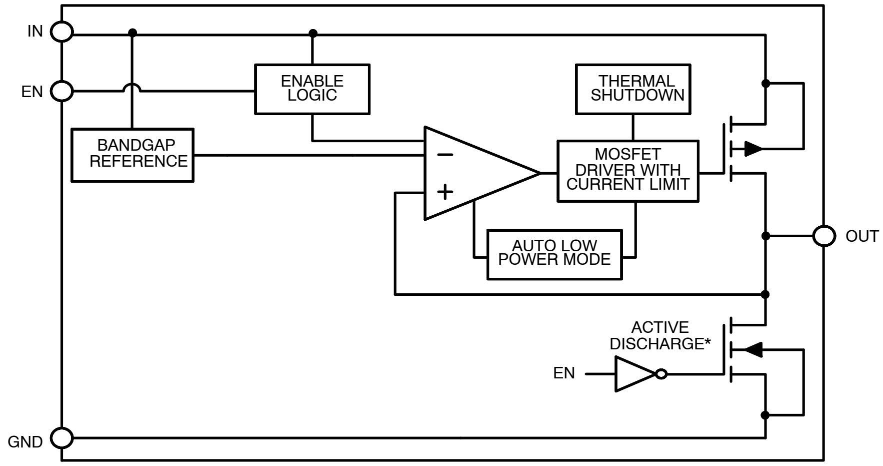


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT	Regulated output voltage pin. A small ceramic capacitor with minimum value of 1 μF is needed from this pin to ground to assure stability.
2	GND	Power supply ground.
3	EN	Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
4	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability.
–	EPAD	Exposed pad should be connected directly to the GND pin. Soldered to a large ground copper plane allows for effective heat removal.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6 V	V
Output Voltage	V_{OUT}	−0.3 V to V_{IN} + 0.3 V or 6 V	V
Enable Input	V_{EN}	−0.3 V to V_{IN} + 0.3 V or 6 V	V
Output Short Circuit Duration	t_{SC}	∞	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22-A114,
   ESD Machine Model tested per EIA/JESD22-A115,
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics, uDFN4 1x1 mm Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	170	°C/W

3. Single component mounted on 1 oz, FR 4 PCB with 645 mm^2 Cu area.

ELECTRICAL CHARACTERISTICS

−40 °C ≤ T_J ≤ 85 °C; V_{IN} = $V_{OUT(NOM)}$ + 1 V for V_{OUT} options greater than 1.5 V. Otherwise V_{IN} = 2.5 V, whichever is greater; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 µF, unless otherwise noted. V_{EN} = 0.9 V. Typical values are at T_J = +25 °C. Min./Max. are for T_J = −40 °C and T_J = +85 °C respectively (Note 4).

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.7		5.5	V
Output Voltage Accuracy	−40 °C ≤ T_J ≤ 85 °C		V_{OUT}	−2		+2	%
Line Regulation	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V (V_{IN} ≥ 1.7 V)		Reg_{LINE}		0.01	0.1	%/V
Load Regulation	I_{OUT} = 1 mA to 300 mA		Reg_{LOAD}		12	30	mV
Load Transient	I_{OUT} = 1 mA to 300 mA or 300 mA to 1 mA in 1 µs, C_{OUT} = 1 µF		$Tran_{LOAD}$		−50/ +30		mV
Dropout Voltage (Note 5)	I_{OUT} = 300 mA	V_{OUT} = 1.8 V	V_{DO}		245	330	mV
		V_{OUT} = 2.8 V			155	230	
		V_{OUT} = 3.0 V			145	220	
Output Current Limit	V_{OUT} = 90% $V_{OUT(nom)}$		I_{CL}	300	600		mA
Ground Current	I_{OUT} = 0 mA		I_Q		50	95	µA
Shutdown Current	V_{EN} ≤ 0.4 V, V_{IN} = 5.5 V		I_{DIS}		0.01	1	µA
EN Pin Threshold Voltage							V
High Threshold	V_{EN} Voltage increasing		V_{EN_HI}	0.9			
Low Threshold	V_{EN} Voltage decreasing		V_{EN_LO}			0.4	
EN Pin Input Current	V_{EN} = 5.5 V		I_{EN}		0.3	1.0	µA
Power Supply Rejection Ratio	V_{IN} = 2.8 V, V_{OUT} = 1.8 V I_{OUT} = 150 mA	f = 1 kHz	PSRR		75		dB
Output Noise Voltage	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, I_{OUT} = 150 mA f = 10 Hz to 100 kHz		V_N		70		$µV_{rms}$
Thermal Shutdown Temperature	Temperature increasing from T_J = +25 °C		T_{SD}		160		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}		T_{SDH}		20		°C
Active Output Discharge Resistance	V_{EN} < 0.4 V		R_{DIS}		100		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_J = T_A = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Characterized when V_{OUT} falls 100 mV below the regulated voltage at V_{IN} = $V_{OUT(NOM)}$ + 1 V.

TYPICAL CHARACTERISTICS

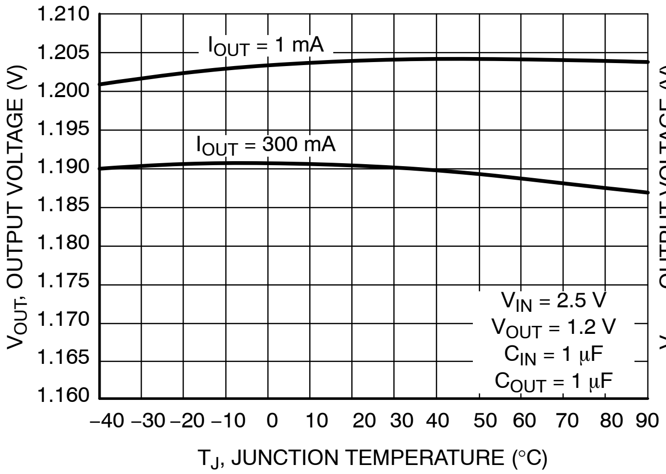


Figure 3. Output Voltage vs. Temperature V_{OUT} = 1.2 V (UDFN)

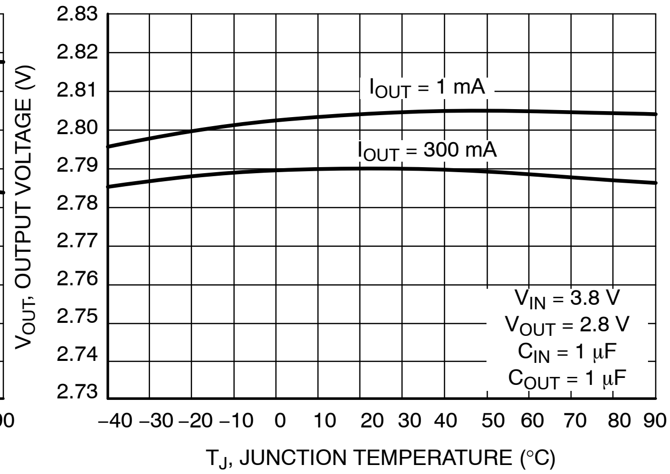


Figure 4. Output Voltage vs. Temperature V_{OUT} = 2.8 V (UDFN)

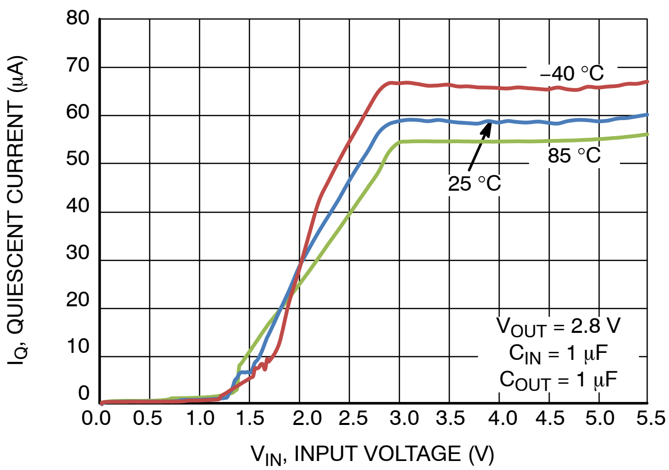


Figure 5. Quiescent Current vs. Input Voltage

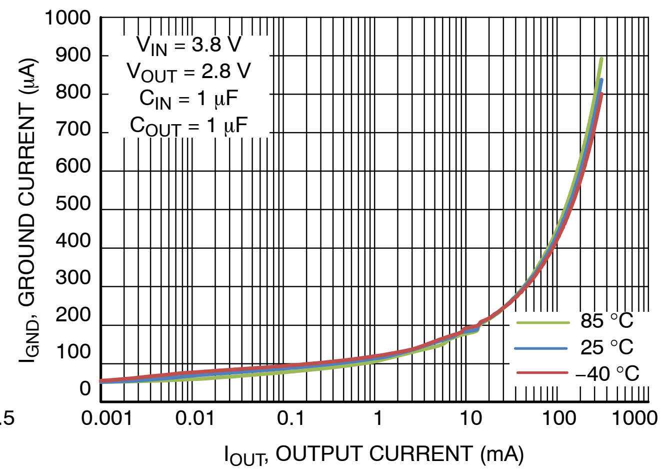


Figure 6. Ground Current vs. Output Current

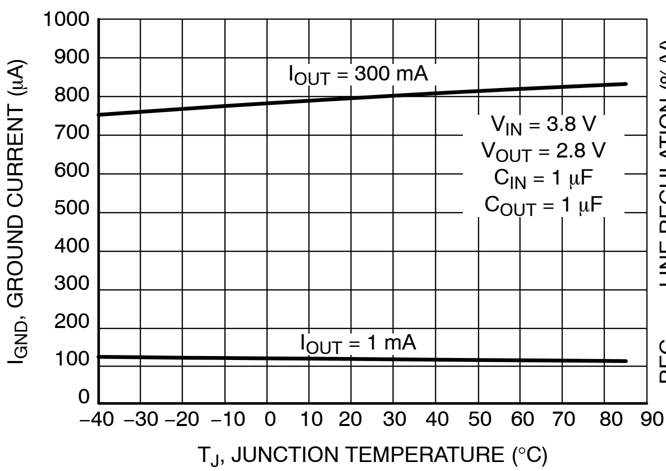


Figure 7. Ground Current vs. Temperature

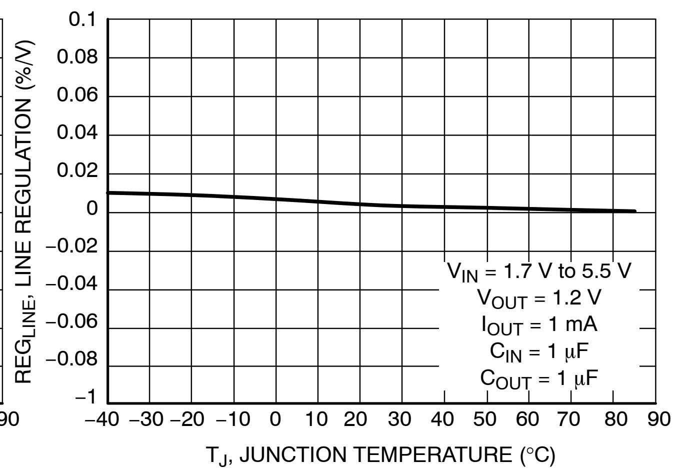


Figure 8. Line Regulation vs. Output Current V_{OUT} = 1.2 V

TYPICAL CHARACTERISTICS

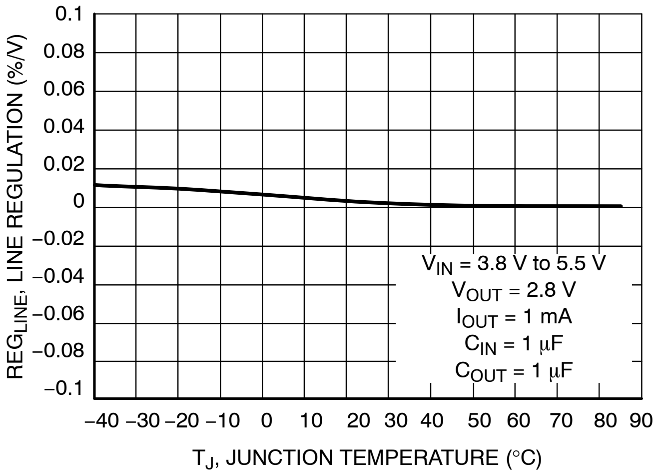


Figure 9. Line Regulation vs. Temperature V_{OUT} = 2.8 V

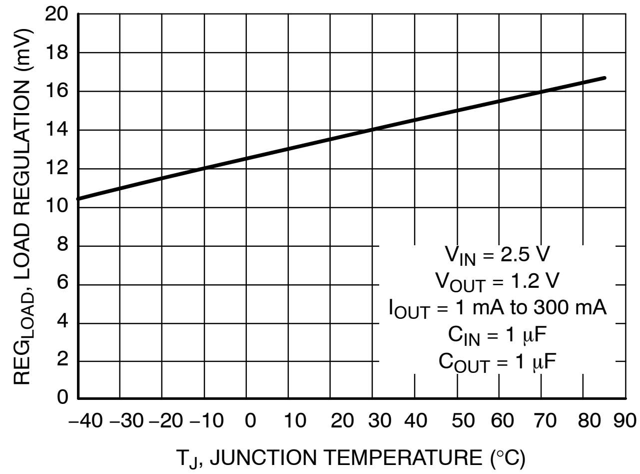


Figure 10. Load Regulation vs. Temperature V_{OUT} = 1.2 V (UDFN)

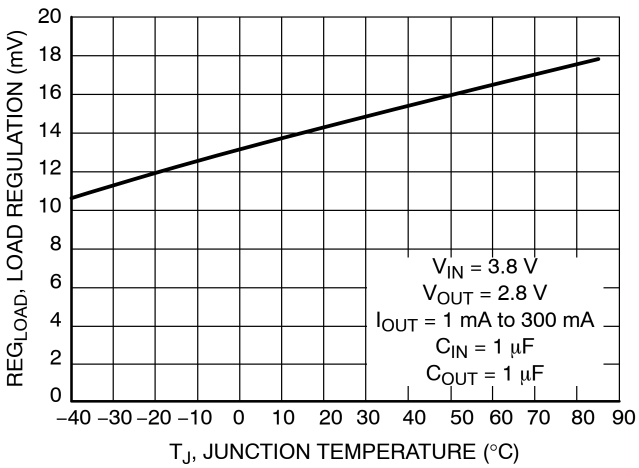


Figure 11. Load Regulation vs. Temperature V_{OUT} = 2.8 V (UDFN)

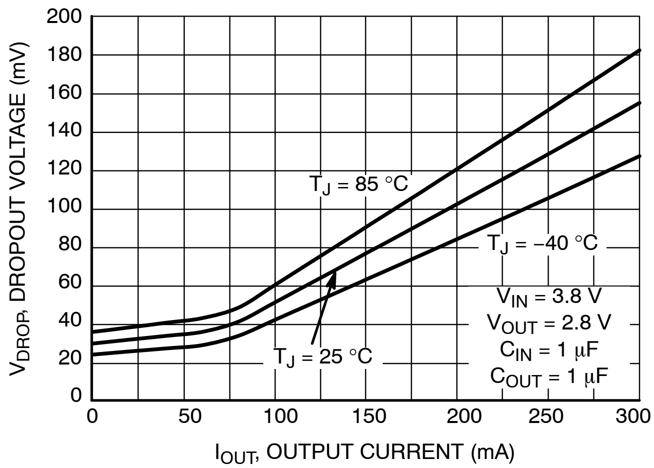


Figure 12. Dropout Voltage vs. Output Current V_{OUT} = 2.8 V (UDFN)

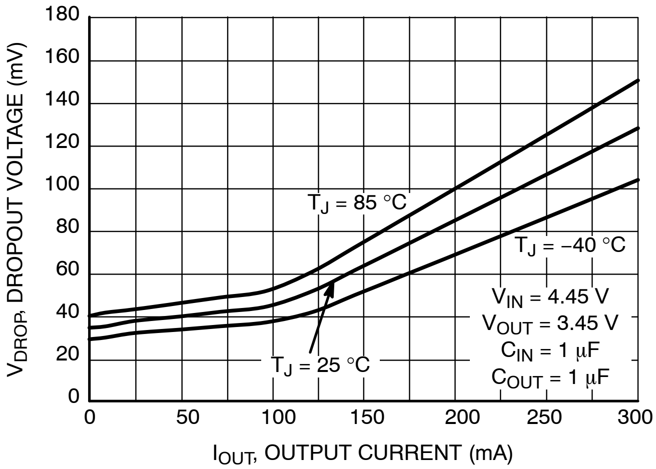


Figure 13. Dropout Voltage vs. Output Current V_{OUT} = 3.45 V (UDFN)

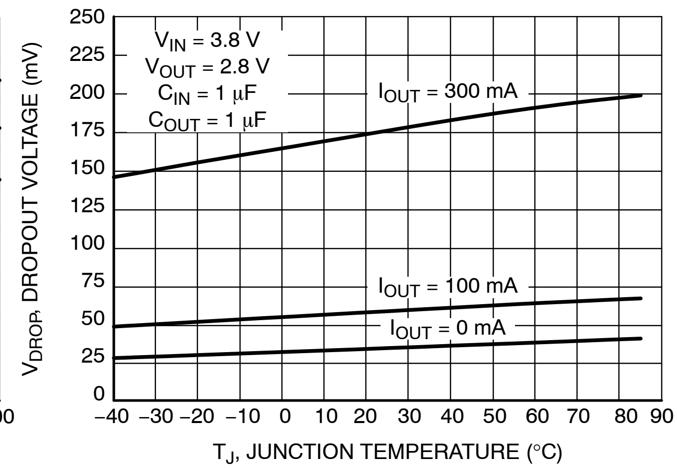


Figure 14. Dropout Voltage vs. Temperature V_{OUT} = 2.8 V (UDFN)

TYPICAL CHARACTERISTICS

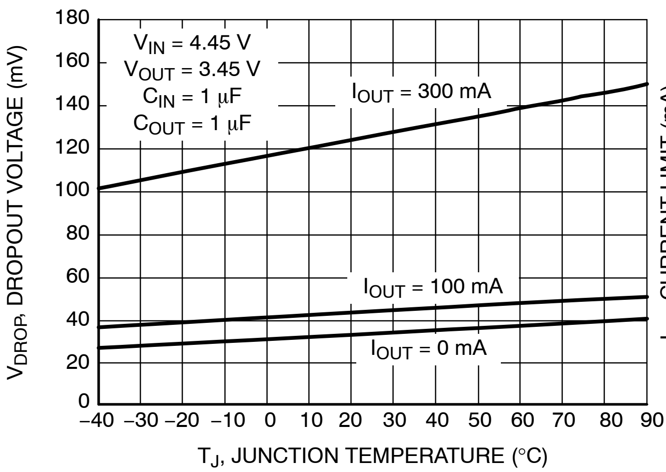


Figure 15. Dropout Voltage vs. Temperature V_{OUT} = 3.45 V (UDFN)

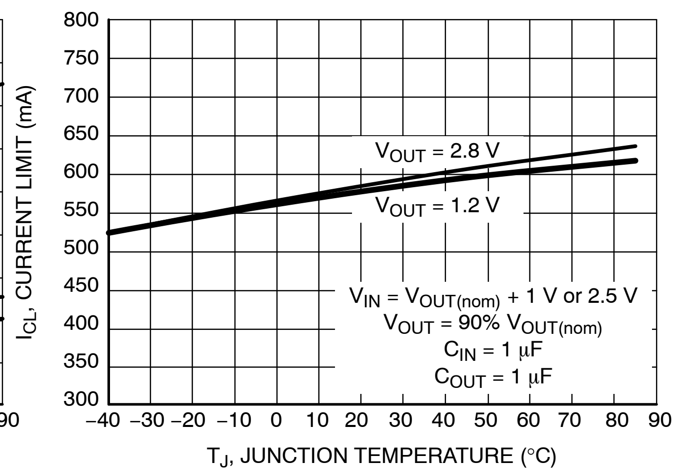


Figure 16. Current Limit vs. Temperature

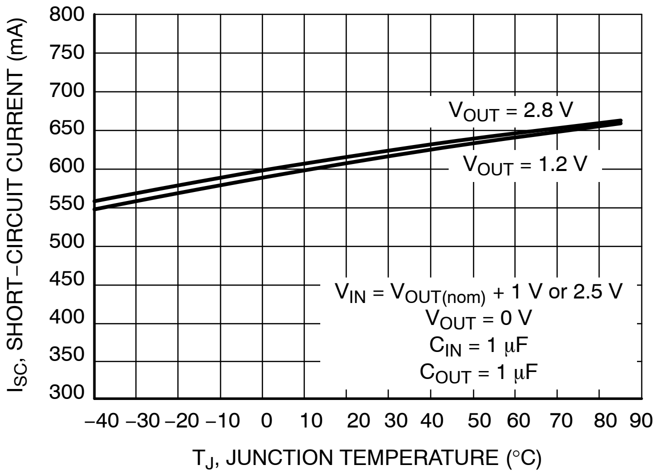


Figure 17. Short-Circuit Current vs. Temperature

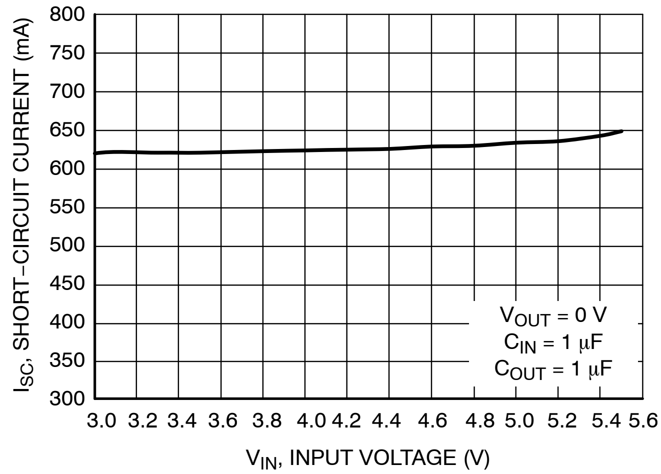


Figure 18. Short-Circuit Current vs. Input Voltage

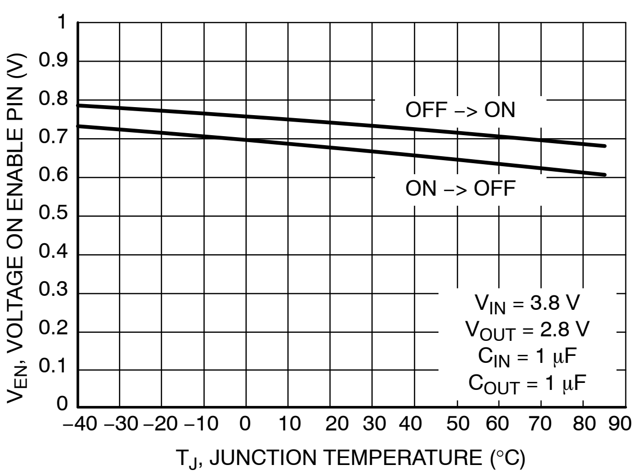


Figure 19. Enable Voltage Threshold vs. Temperature

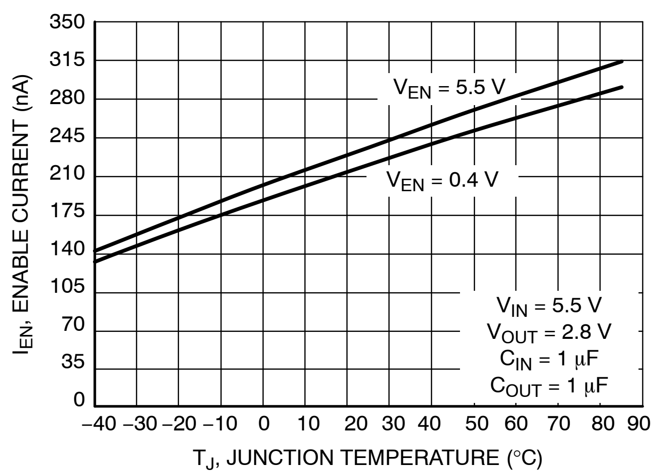


Figure 20. Current to Enable Pin vs. Temperature

TYPICAL CHARACTERISTICS

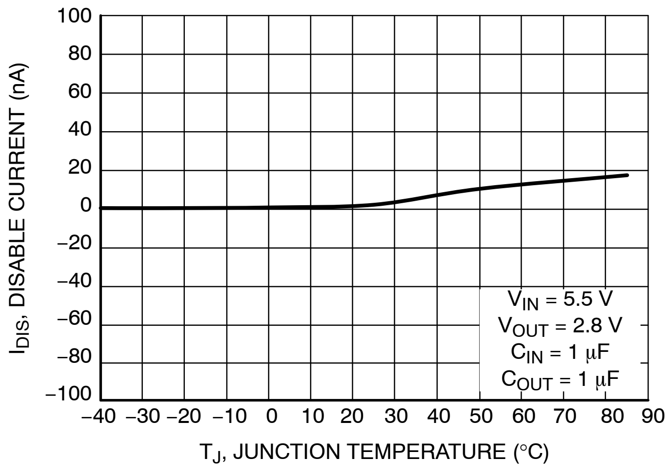
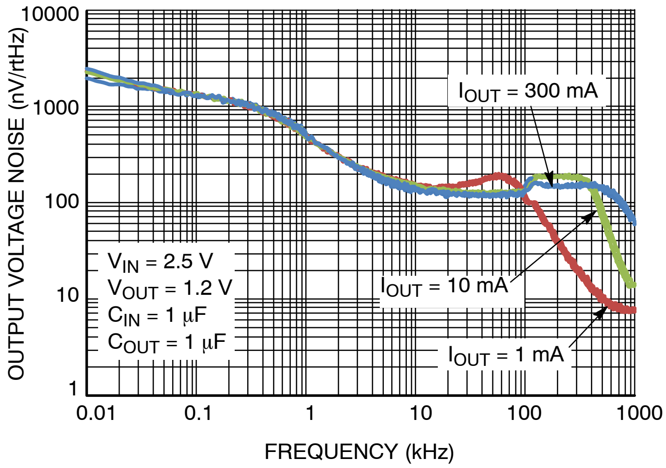


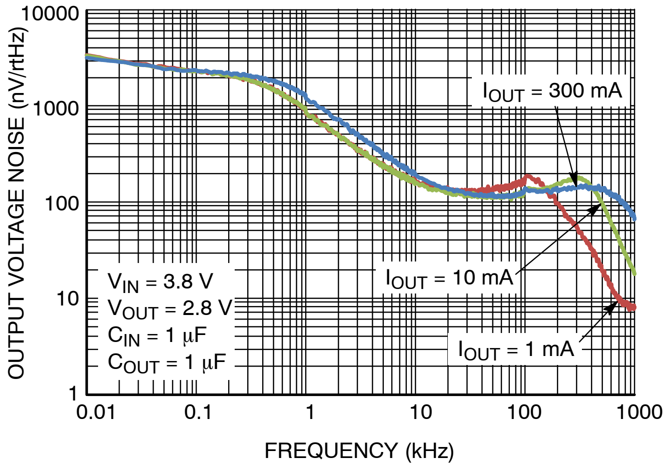
Figure 21. Disable Current vs. Temperature

TYPICAL CHARACTERISTICS



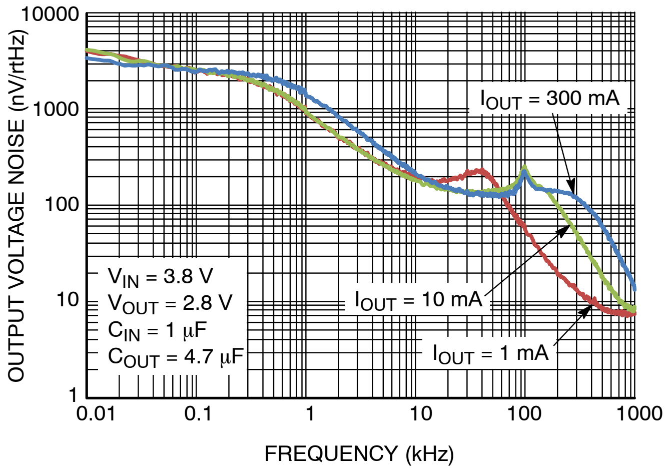
I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	60.93	59.11
10 mA	52.73	50.63
300 mA	52.06	50.17

Figure 22. Output Voltage Noise Spectral Density for V_{OUT} = 1.2 V, C_{OUT} = 1 μF



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	79.23	74.66
10 mA	75.03	70.37
300 mA	87.74	83.79

Figure 23. Output Voltage Noise Spectral Density for V_{OUT} = 2.8 V, C_{OUT} = 1 μF



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	80.17	75.29
10 mA	81.28	76.46
300 mA	93.23	89.62

Figure 24. Output Voltage Noise Spectral Density for V_{OUT} = 2.8 V, C_{OUT} = 4.7 μF

TYPICAL CHARACTERISTICS

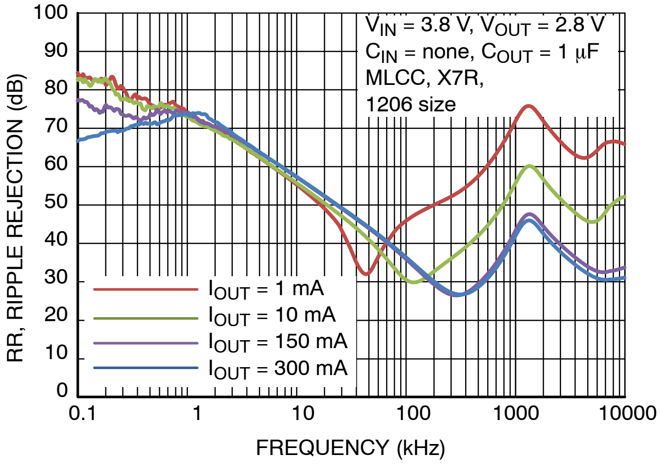


Figure 25. Power Supply Rejection Ratio, V_{OUT} = 2.8 V, C_{OUT} = 1 μF

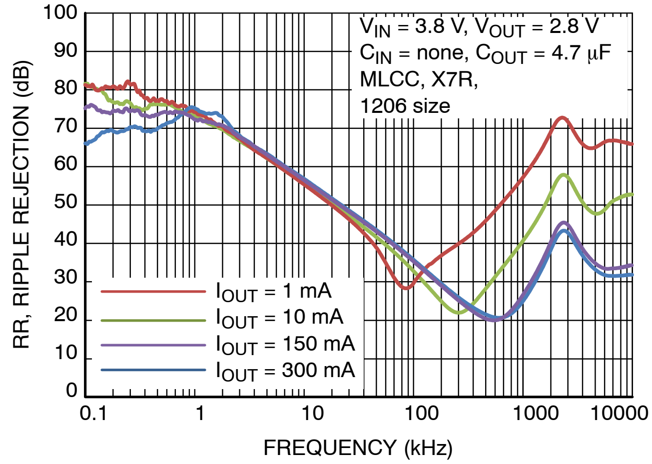


Figure 26. Power Supply Rejection Ratio, V_{OUT} = 2.8 V, C_{OUT} = 4.7 μF

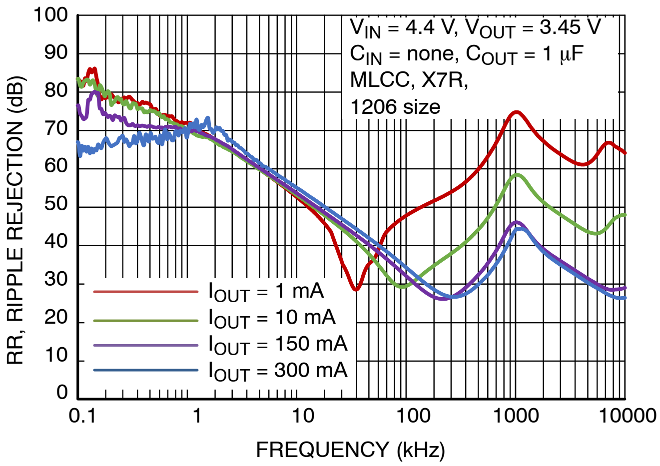


Figure 27. Power Supply Rejection Ratio, V_{OUT} = 3.45 V, C_{OUT} = 1 μF

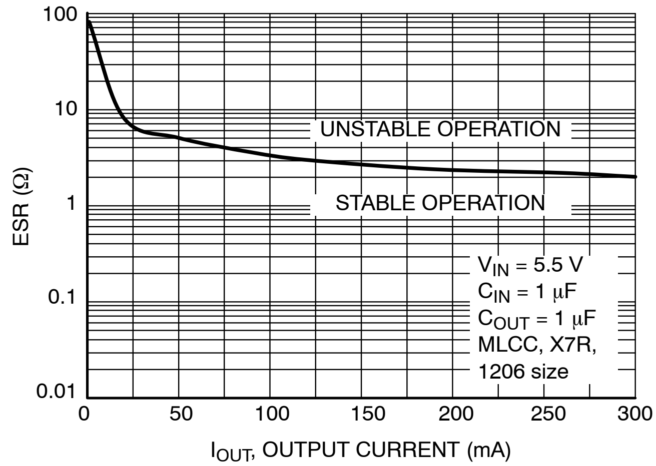


Figure 28. Output Capacitor ESR vs. Output Current

TYPICAL CHARACTERISTICS

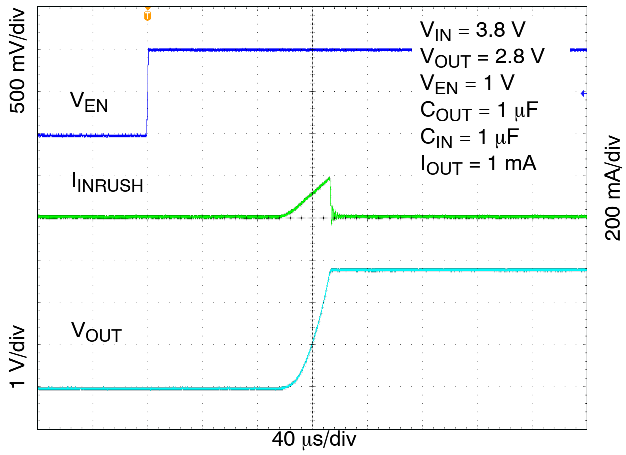


Figure 29. Enable Turn-on Response, C_{OUT} = 1 µF, I_{OUT} = 1 mA

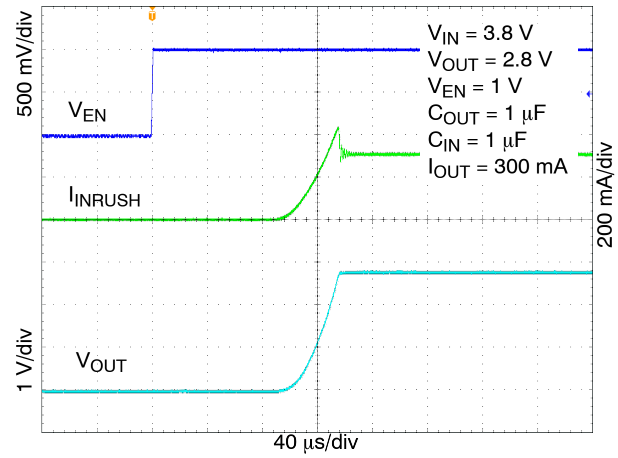


Figure 30. Enable Turn-on Response, C_{OUT} = 1 µF, I_{OUT} = 300 mA

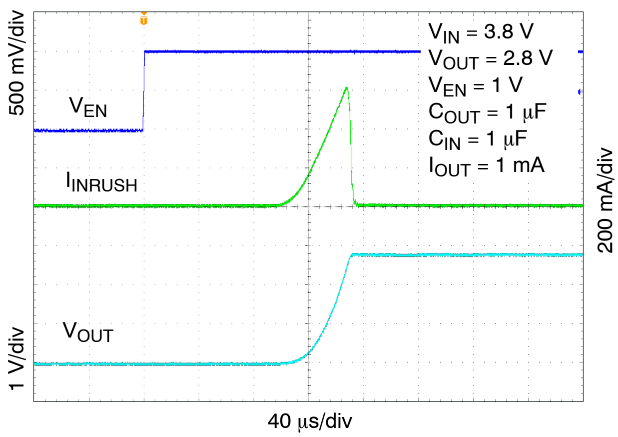


Figure 31. Enable Turn-on Response, C_{OUT} = 4.7 µF, I_{OUT} = 1 mA

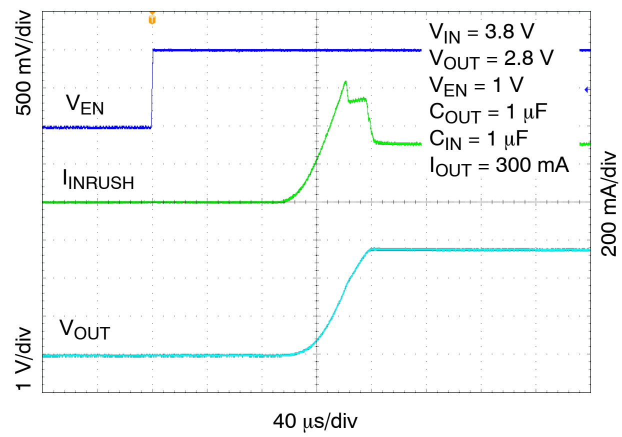


Figure 32. Enable Turn-on Response, C_{OUT} = 4.7 µF, I_{OUT} = 300 mA

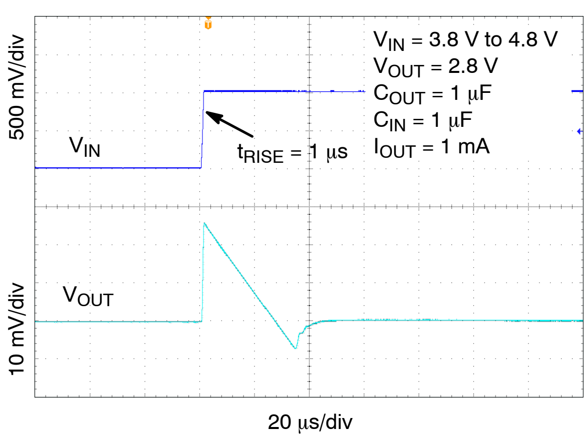


Figure 33. Line Transient Response – Rising Edge, V_{OUT} = 2.8 V, I_{OUT} = 1 mA

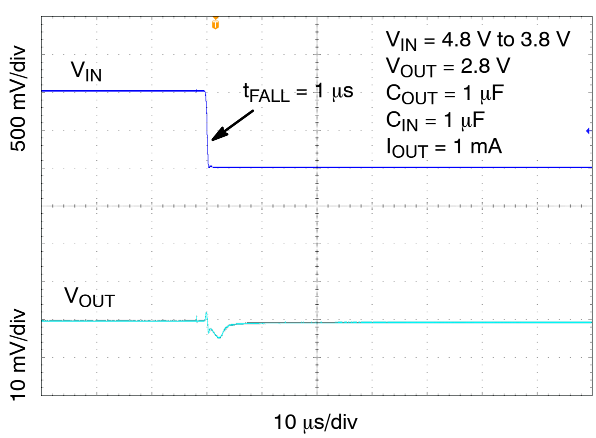


Figure 34. Line Transient Response – Falling Edge, V_{OUT} = 2.8 V, I_{OUT} = 1 mA

TYPICAL CHARACTERISTICS

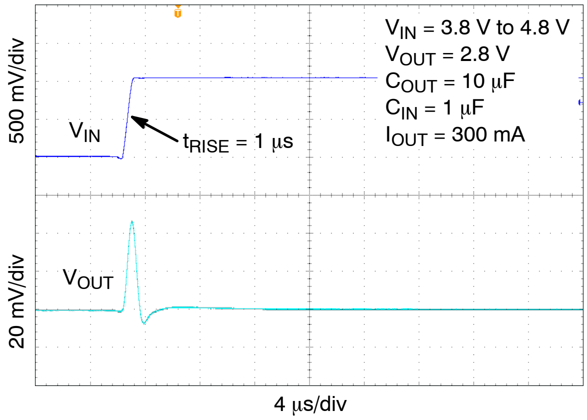


Figure 35. Line Transient Response – Rising Edge, V_{OUT} = 2.8 V, I_{OUT} = 300 mA

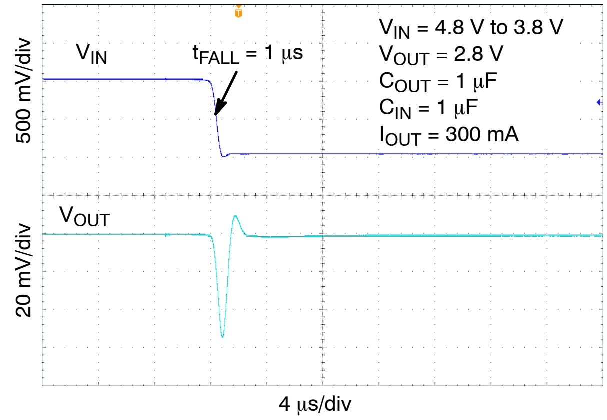


Figure 36. Line Transient Response – Falling Edge, V_{OUT} = 2.8 V, I_{OUT} = 300 mA

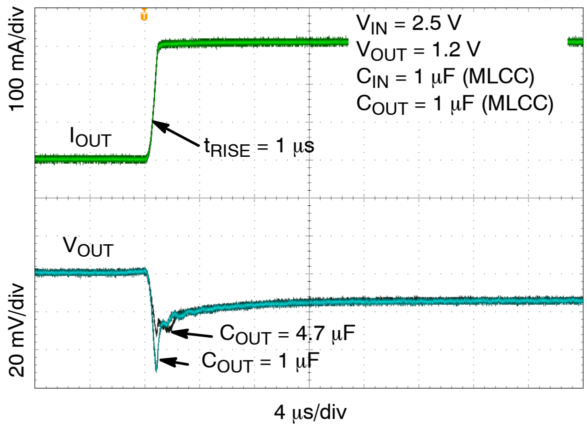


Figure 37. Load Transient Response – Rising Edge, V_{OUT} = 1.2 V, I_{OUT} = 1 mA to 300 mA, C_{OUT} = 1 µF, 4.7 µF

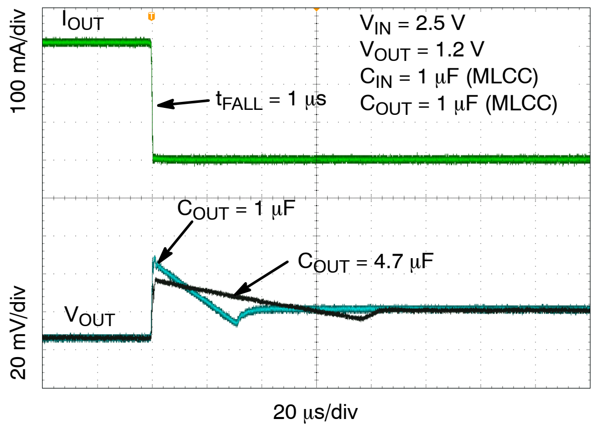


Figure 38. Load Transient Response – Falling Edge, V_{OUT} = 1.2 V, I_{OUT} = 1 mA to 300 mA, C_{OUT} = 1 µF, 4.7 µF

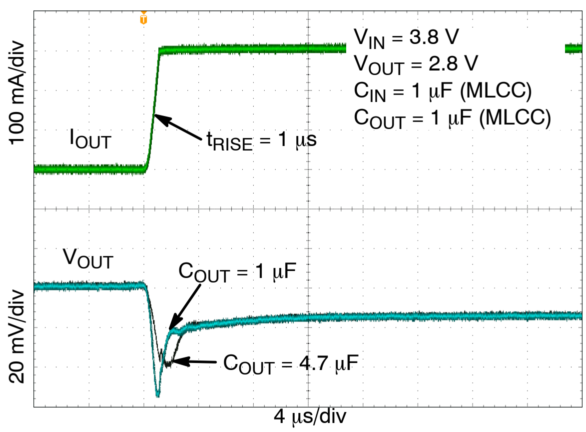


Figure 39. Load Transient Response – Rising Edge, V_{OUT} = 2.8 V, I_{OUT} = 1 mA to 300 mA, C_{OUT} = 1 µF, 4.7 µF

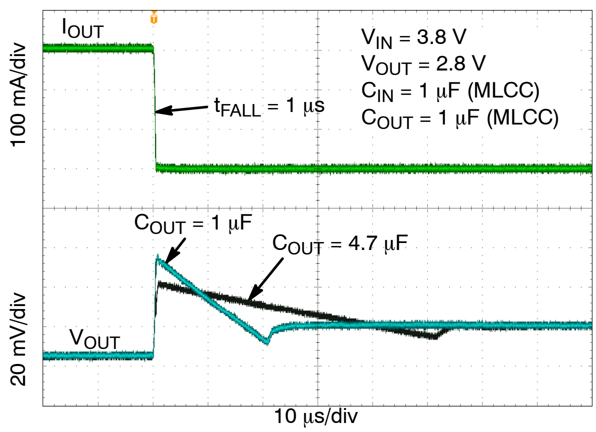


Figure 40. Load Transient Response – Falling Edge, V_{OUT} = 2.8 V, I_{OUT} = 1 mA to 300 mA, C_{OUT} = 1 µF, 4.7 µF

TYPICAL CHARACTERISTICS

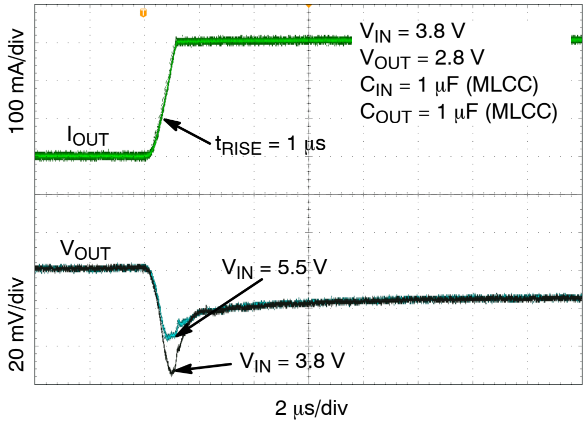


Figure 41. Load Transient Response – Rising Edge, V_{OUT} = 2.8 V, I_{OUT} = 1 mA to 300 mA, V_{IN} = 3.8 V, 5.5 V

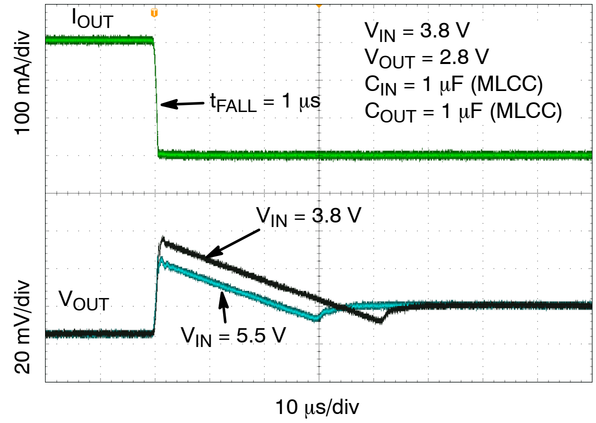


Figure 42. Load Transient Response – Falling Edge, V_{OUT} = 2.8 V, I_{OUT} = 1 mA to 300 mA, V_{IN} = 3.8 V, 5.5 V

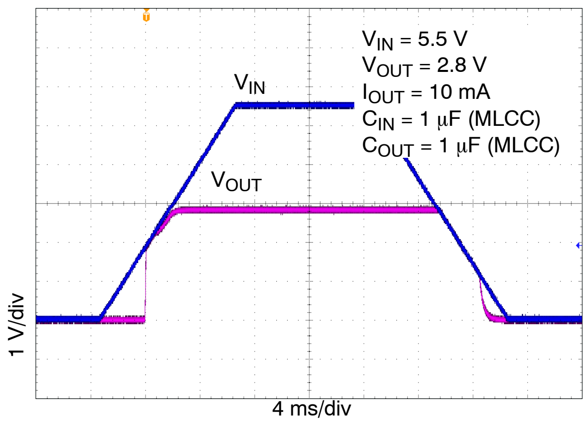


Figure 43. Turn-on/off – Slow Rising V_{IN}

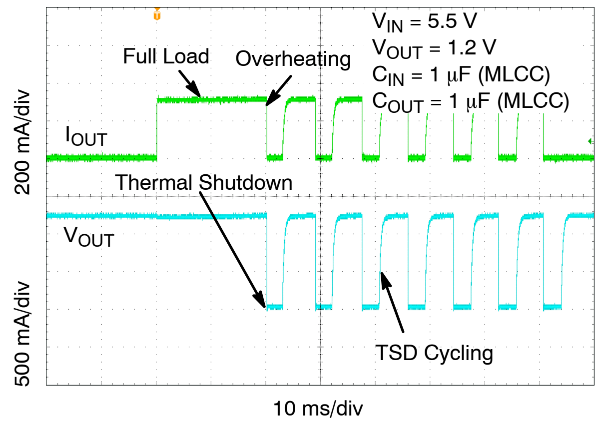


Figure 44. Short-Circuit and Thermal Shutdown

APPLICATIONS INFORMATION

General

The SCP114 is a high performance 300 mA Low Dropout Linear Regulator. This device delivers very high PSRR and excellent dynamic performance as load/line transients. In connection with very low quiescent current this device is very suitable for various battery powered applications such as tablets, cellular phones, wireless and many others. The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor Selection (C_{IN})

It is recommended to connect at least a 1 μF Ceramic X5R or X7R capacitor as close as possible to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. /max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes. Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

Output Decoupling (C_{OUT})

The SCP114 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The SCP114 is designed to remain stable with minimum effective capacitance of 0.22 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0402 the effective capacitance drops rapidly with the applied DC bias.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 2 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The SCP114 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned-off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 100 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}.

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The SCP114 regulates the output voltage and the active discharge transistor is turned-off.

The EN pin has internal pull-down current source with typ. value of 300 nA which assures that the device is turned-off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

Output Current Limit

Output Current is internally limited within the IC to a typical 600 mA. The SCP114 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 630 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} – 160 °C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} – 140 °C typical). Once the IC temperature falls below the 140 °C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the SCP114 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the SCP114 can handle is given by:

$$P_{D(MAX)} = \frac{\left[125\,°C - T_A\right]}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the SCP114 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}@I_{OUT}\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

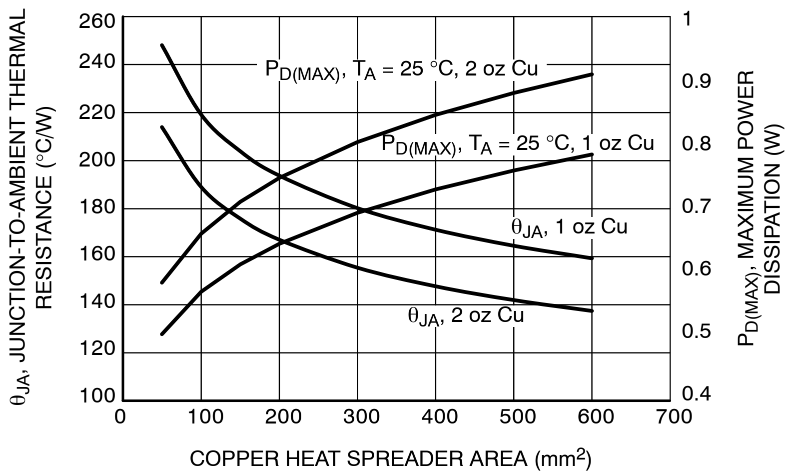


Figure 45. θ_{JA} vs. Copper Area (uDFN4)

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The SCP114 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz − 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Turn-On Time

The turn-on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT} and T_A. For example typical value for V_{OUT} = 1.0 V, C_{OUT} = 1 μF, I_{OUT} = 1 mA and T_A = 25 °C is 90 μs.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad should be tied the shortest path to the GND pin.

ORDERING INFORMATION

Device	Voltage Option	Marking	Marking Rotation	Option	Package	Shipping†
SCP114AMX120TCG	1.2 V	T	0°	With active output discharge function	uDFN4 (Pb-Free)	3000 / Tape & Reel
SCP114AMX280TCG	2.8 V	2	0°	With active output discharge function	uDFN4 (Pb-Free)	3000 / Tape & Reel

DISCONTINUED (Note 6)

SCP114AMX180TCG	1.8 V	J	180°	With active output discharge function	uDFN4 (Pb-Free)	3000 / Tape & Reel
SCP114AMX300TCG	3.0 V	4	0°	With active output discharge function	uDFN4 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

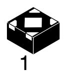
6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

REVISION HISTORY

Revision	Description of Changes	Date
2	Update to new formatting and discontinue some OPNs	2/10/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

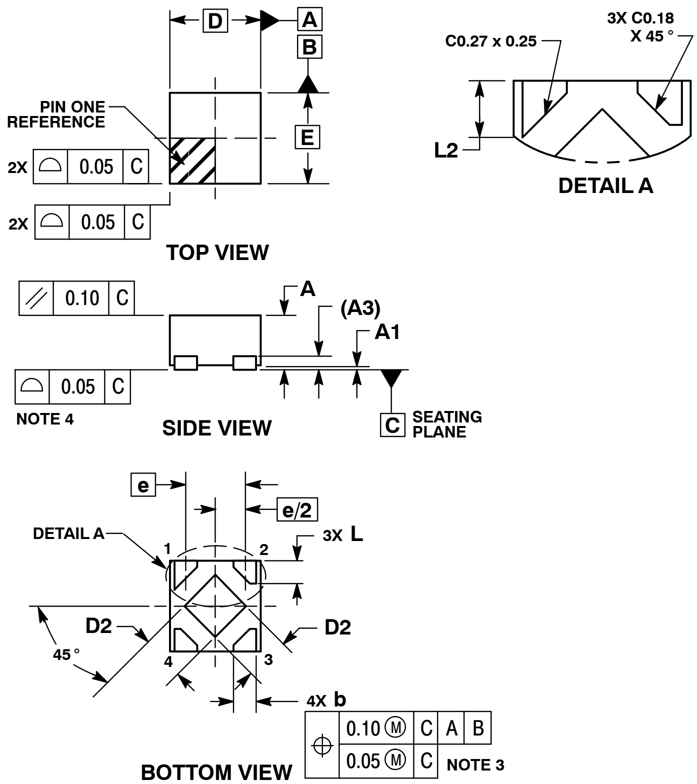
PACKAGE DIMENSIONS



SCALE 4:1

UDFN4 1.0x1.0, 0.65P
CASE 517CU
ISSUE A

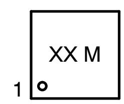
DATE 18 DEC 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.03 AND 0.07 FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	---	0.60
A1	0.00	0.05
A3	0.15 REF	
b	0.20	0.30
D	1.00 BSC	
D2	0.38	0.58
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.27	0.37

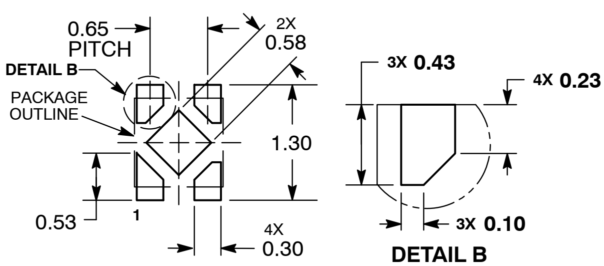
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales