1.7V-5.5V Vin, 500mA, 8uA I_Q, Low-Dropout Regulator

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide Input Range: 1.7V-5.5V
- Maximum Output Current: 500mA
- Output Voltage:
  - 1.2V, 1.8V and 3.3V (Fixed Output)
  - 0.7V~5V (Adjustable Output Version-SCT71005A01Q)
  - 0.5V~5V (Adjustable Output Version-SCT71005A02Q)
- Output Voltage Accuracy:
  - T_J= 25℃：±1%
  - T_J= -40℃~ 125℃：±2%
- Low Quiescent Current: 8uA
- Ultra-Low Shutdown Current: 0.02uA
- Low Dropout Voltage：
  - 54mV at 200mA load current
  - 143mV at 500mA load current
- Support Output Capacitors Range:
  - 2.2uF~220uF
  - Low-ESR: 0.001Ω~ 5 Ω
- 2.3ms Internal Soft-start Time(V_{REF}=500mV)
- Integrated Short-Circuit Protection with OCFB (Over Current Fold-back) Feature
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Over-Temperature Protection
- Power-Good Feature is available
- Active Output Discharge
- Available Package: SOT23-5/ TDFN2x2-6/ TDFN2x3-8

APPLICATIONS

- Battery-Powered Systems
- Automotive infotainment
- Navigation systems
- Portable appliances

DESCRIPTION

The SCT71005Q series products is a low-dropout linear regulator designed to operate with a wide input-voltage range from 1.7 V to 5.5 V and 500mA output current with enable control and Power-Good feature. The SCT71005Q series products is stable with 2.2uF~220uF output capacitors, and 10uF ceramic capacitor is recommended.

Only 8-μA typical quiescent current at light load makes the SCT71005Q series products ideal choices for portable devices with battery power supply and an optimal solution for powering microcontrollers (MCUs) and CAN/LIN transceivers in always-on systems.

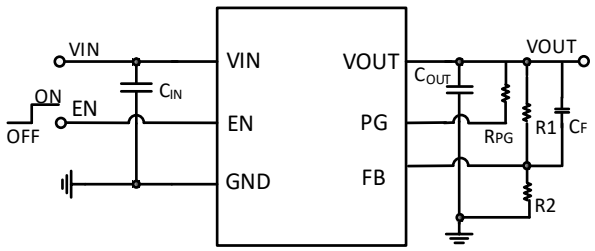
The SCT71005Q series products implements power good circuit (PG) which indicates that output voltage is in regulation. This signal could be used for power sequencing or as a microcontroller reset.

The SCT71005Q series products integrated short-circuit and overcurrent protection with OCFB (Over Current Fold-back) feature, which makes the device more reliable during transient high-load current faults or shorting events.

The SCT71005Q series products provide fixed 1.2V,1.8V and 3.3V output voltage versions, and also could provide adjust output voltage version with 0.7V、0.5V feedback voltage.

The SCT71005Q series products is available in SOT23-5, TDFN2x2-6 and TDFN2x3-8 packages, for other package options, please contact SCT sales.

TYPICAL APPLICATION



REVISION HISTORY

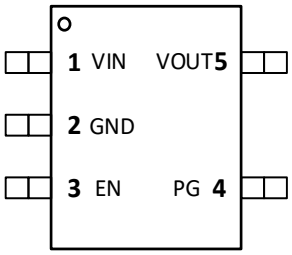
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Sampling.

DEVICE ORDER INFORMATION

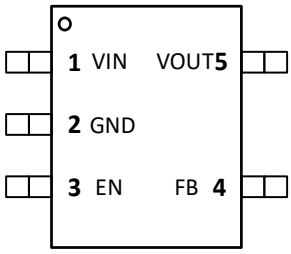
Part Number	Output Voltage	Package	Package Marking	Transport Media, Quantity
SCT71005F33QTWDR	Fixed 3.3V	SOT23-5	5F33Q	Tape & Reel, 3000
SCT71005F18QTWDR	Fixed 1.8V	SOT23-5	5F18Q	Tape & Reel, 3000
SCT71005F12QTWDR	Fixed 1.2V	SOT23-5	5F12Q	Tape & Reel, 3000
SCT71005A01QTWDR	Adjust	SOT23-5	5A01Q	Tape & Reel, 3000
SCT71005F33QDVAR	Fixed 3.3V	TDFN2X2-6	5F33Q	Tape & Reel, 3000
SCT71005F18QDVAR	Fixed 1.8V	TDFN2X2-6	5F18Q	Tape & Reel, 3000
SCT71005F12QDVAR	Fixed 1.2V	TDFN2X2-6	5F12Q	Tape & Reel, 3000
SCT71005A02QDTDR	Adjust	TDFN2X3-8	5A02Q	Tape & Reel, 5000

PIN CONFIGURATION



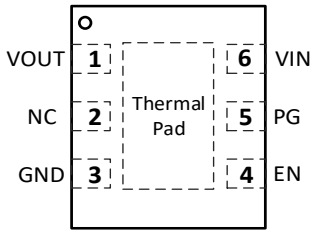
SCT71005FxxQTWDR

SOT23-5 Package



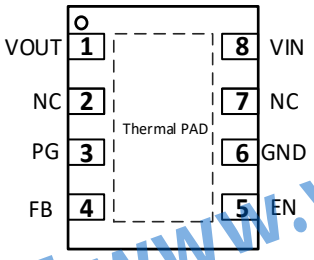
SCT71005A01QTWDR

SOT23-5 Package



SCT71005FxxQDVAR

TDFN2x2-6 Package



SCT71005A02QDTDR

TDFN2x3-8 Package

PIN FUNCTIONS

SOT23-5/SCT71005FxxQ:

NAME	NAME	PIN FUNCTION
1	VIN	Input voltage pin
2	GND	Ground reference pin.
3	EN	Enable input pin. This pin has an internal resistor($R_{EN\_pulldown}$) to hold the regulator off by default. A low voltage($V_{EN} < V_{EN\_L}$) on this pin turns the regulator off and discharges the output pin to GND through an internal pulldown resistor($R_{discharge}$).A high voltage($V_{EN} > V_{EN\_H}$) on this pin enables the regulator output.The pulldown resistor($R_{EN\_pulldown}$). $R_{EN\_pulldown}$ Is disconnected to reduce input current when $V_{EN} > V_{EN\_H}$.
4	PG	Power-good pin
5	VOUT	Regulated output voltage pin

SOT23-5/SCT71005A01Q:

NAME	NAME	PIN FUNCTION
1	VIN	Input voltage pin
2	GND	Ground reference pin.
3	EN	Enable input pin. This pin has an internal resistor($R_{EN\_pulldown}$) to hold the regulator off by default. A low voltage($V_{EN} < V_{EN\_L}$) on this pin turns the regulator off and discharges the output pin to GND through an internal pulldown resistor($R_{discharge}$).A high voltage($V_{EN} > V_{EN\_H}$) on this pin enables the regulator output.The pulldown resistor($R_{EN\_pulldown}$). $R_{EN\_pulldown}$ Is disconnected to reduce input current when $V_{EN} > V_{EN\_H}$.
4	FB	Feedback voltage pin
5	VOUT	Regulated output voltage pin

TDFN2x2-6/SCT71005FxxQ:

NAME	NAME	PIN FUNCTION
1	VOUT	Regulated output voltage pin
2	NC	No connection
3	GND	Ground reference pin.
4	EN	Enable input pin. This pin has an internal resistor($R_{EN\_pulldown}$) to hold the regulator off by default. A low voltage($V_{EN} < V_{EN\_L}$) on this pin turns the regulator off and discharges the output pin to GND through an internal pulldown resistor($R_{discharge}$).A high voltage($V_{EN} > V_{EN\_H}$) on this pin enables the regulator output.The pulldown resistor($R_{EN\_pulldown}$). $R_{EN\_pulldown}$ Is disconnected to reduce input current when $V_{EN} > V_{EN\_H}$.
5	PG	Power-good pin
6	VIN	Input voltage pin
7	Thermal Pad	Connect the thermal pad to a large area GND plane for improved thermal performance.

TDFN2x3-8/SCT71005A02Q:

NAME	NAME	PIN FUNCTION
1	VOUT	Regulated output voltage pin
2	NC	No connection

3	PG	Power-good pin
4	FB	Feedback voltage pin
5	EN	Enable input pin. This pin has an internal resistor($R_{EN\_pulldown}$) to hold the regulator off by default. A low voltage($V_{EN} < V_{EN\_L}$) on this pin turns the regulator off and discharges the output pin to GND through an internal pulldown resistor($R_{discharge}$).A high voltage($V_{EN} > V_{EN\_H}$) on this pin enables the regulator output.The pulldown resistor($R_{EN\_pulldown}$). $R_{EN\_pulldown}$ Is disconnected to reduce input current when $V_{EN} > V_{EN\_H}$.
6	GND	Ground reference pin.
7	NC	No connection
8	VIN	Input voltage pin
9	Thermal Pad	Connect the thermal pad to a large area GND plane for improved thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	1.7	5.5	V
V_{OUT}	Fixed Output voltage	1.2	3.3	V
	Adjustable Output Version-SCT71005A01Q	0.7	5	V
	Adjustable Output Version-SCT71005A02Q	0.5	5	V
V_{EN}	Enable input voltage	0	V_{IN}	V
V_{PG}	Power-good pin voltage	0	5.5	V
C_{IN}	Input capacitor	2.2	--	uF
C_{OUT}	Output capacitor	2.2	220	uF
ESR	Output capacitor ESR requirements	0.001	5	Ω
T_J	Operating junction temperature	-40	150	°C

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted (1)

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range	-0.3	6	V
V_{OUT}	Maximum output voltage range	-0.3	6	V
V_{EN}	Maximum enable input voltage	-0.3	V_{IN}	V
V_{PG}	Maximum power-good pin voltage	-0.3	6	V
T_J (2)	Junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-7	+7	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

The value of $R_{\theta JA}$ and $R_{\theta JC}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. Because they were simulated in accordance with JESD 51-7. They do not represent the performance obtained in an actual application. For design information see Power Dissipation and Thermal Performance section.

The value of $R_{\theta JA\_EVM}$ is the tested results based on our EVM, and is more useful for thermal design. Even if it still do not represent the thermal performance of customer's PCB design, but it was a good starting point for thermal performance design.

The PCB information of our EVM: 4-layer,1oz Cu (inner 0.5oz Cu), 50mm x 30mm size.2-layer(only for DFN1X1-4), 1oz Cu, 50mm x 30mm size.

The values given in this table are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB), thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the device. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual values of the below table.

Package Type	$R_{\theta JA}$(1)	Ψ_{JT}	Ψ_{JB}	$R_{\theta JCtop}$ (2)	$R_{\theta JA\_EVM}$(3)	UNIT
SOT23-5	TBD	TBD	TBD	TBD	TBD	°C/W
TDFN2X2-6	83.37	18.82	38.76	35.88	TBD	
TDFN2X3-8	81.76	20.11	38	36.64	59.04	
DFN1X1-4 (2-layer)	TBD	TBD	TBD	TBD	TBD	

(1) $R_{\theta JA}$ is junction to ambient thermal resistance, based on JESD51-7.

(2) $R_{\theta JC}$ is junction to case thermal resistance, based on JESD51-7.

(3) $R_{\theta JA\_EVM}$ is junction to ambient thermal resistance, which is tested on SCT EVM.

ELECTRICAL CHARACTERISTICS

V_{IN}=V_{OUT}+1V, C_{OUT}=10uF, T_J= -40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		1.7		5.5	V
V_{UVLO}	V_{IN} UVLO Threshold	V_{IN} rising		1.5	1.6	V
	Hysteresis			100		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, V_{OUT}=1.8V, V_{IN}=2.8V, T_J= 25°C		0.02	0.1	μA
I_Q	Quiescent current from GND pin	EN float, no load, V_{IN}=V_{OUT}+1V		8		μA
Regulated Output Voltage and Current						
V_{OUT}	Output voltage accuracy	T_J= 25°C	-1%		1%	
		T_J= -40°C~125°C	-2%		2%	
V_{REF}	Feedback voltage accuracy	T_J= 25°C(SCT71005A01Q)		700		mV
		T_J= -40°C~125°C(SCT71005A01Q)		700		mV
		T_J= 25°C(SCT71005A02Q)	495	500	505	mV
		T_J= -40°C~125°C(SCT71005A02Q)	490	500	510	mV
ΔV_{OUT}	Line regulation	V_{IN}=V_{OUT}+1V to 5.5V, Iout=10mA		1	10	mV
	Load regulation	Iout=1mA to 500㎃		1.8		mV
V_{DROP}	Dropout voltage(1)	V_{IN}=V_{OUT}-0.1V ,Iout =100mA		28		mV
		V_{IN}=V_{OUT}-0.1V ,Iout =200mA		54		mV
		V_{IN}=V_{OUT}-0.1V ,Iout =500mA		143		mV
I_{OUT}	Output current	V_{OUT} in regulation	0		500	mA
I_{OC}	Output current limit	V_{OUT} short to 90% × V_{OUT}		800		mA
Isc	Short current limit	V_{OUT}=0V		290		mA
PSRR	Power supply rejection ratio(2)	V_{OUT}=1.2V,I_{OUT}=10mA, f=1kHz, C_{OUT}=10μF		47		dB
		V_{OUT}=1.2V,I_{OUT}=10mA, f=10kHz, C_{OUT}=10μF		31		dB
		V_{OUT}=1.2V,I_{OUT}=10mA, f=100kHz, C_{OUT}=10μF		44		dB
Over Voltage Protection						
OVP_H	overshoot of Vout when discharge occur	V_{IN}=3.3V		115%		
OVP_L	overshoot of Vout when discharge disappear	V_{IN}=3.3V		105%		
OVP_{Hys}	overshoot of Vout hysteresis			10%		
Enable and Soft-startup						
V_{EN_H}	Enable rising threshold	$V_{EN\_H\_1.8}$(V_{IN}=1.8V)		0.63		V
		$V_{EN\_H\_3.3}$(V_{IN}=3.3V)		0.75		V
		$V_{EN\_H\_5}$(V_{IN}=5V)		0.867		V
V_{EN_L}	Enable falling threshold	$V_{EN\_L\_1.8}$(V_{IN}=1.8V)		0.607		V
		$V_{EN\_L\_3.3}$(V_{IN}=3.3V)		0.66		V
		$V_{EN\_L\_5}$(V_{IN}=5V)		0.685		V
V_{EN_Hys}	Enable threshold hysteresis	$V_{EN\_Hys\_1.8}$(V_{IN}=1.8V)		23		mV

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
		$V_{EN\_Hys\_3.3}$(V_{IN}=3.3V)		85		mV
		$V_{EN\_Hys\_5}$(V_{IN}=5V)		180		mV
I_{EN_0V}	Enable pin current	EN=0			0.1	μA
T_{SS}	Soft-start time	V_{REF}=700mV		TBD		ms
		V_{REF}=500mV		2.3		ms
Power Good						
V_{PG_R}	PG rising threshold percentage	V_{OUT}/$V_{OUT(NOM)}$,when V_{OUT} rising		90%		
V_{PG_F}	PG falling threshold percentage	V_{OUT}/$V_{OUT(NOM)}$,when V_{OUT} falling		80%		
V_{PG_LOW}	PG output low voltage	PG sink 0.5mA		82		mV
R_{PG}	PG pull down resistor	R_{PG}=V_{PG_LOW}/0.5mA		165		Ω
I_{PG_LKG}	PG leakage current	PG=5V, V_{OUT} in regulation		2		nA
$Td_{\_PGR}$	PG signal turn to high delay	From V_{OUT}>0.90x$V_{OUT(NOM)}$ to PG rising edge delay time		167		us
$Td_{\_PGF}$	PG signal turn to low delay	From V_{OUT}<0.80x$V_{OUT(NOM)}$ to PG falling edge delay time		66		us
Active Discharge						
$R_{discharge}$	Low output NMOS on resistance	EN=0,V_{IN}=3.3V		133		Ω
Thermal Protection						
T_{SD}	Thermal shutdown threshold(3)	T_J rising		170		°C
		Hysteresis		15		°C

(1) The dropout voltage is defined as V_{IN}-V_{OUT}, when force V_{IN} is 100mV below the value of V_{OUT} for V_{IN}=$V_{OUT(NOM)}$+1V.

(2) PSRR is derived from bench characterization, not production test.

(3) Thermal shutdown threshold is derived from bench characterization, not production test.

TYPICAL CHARACTERISTICS

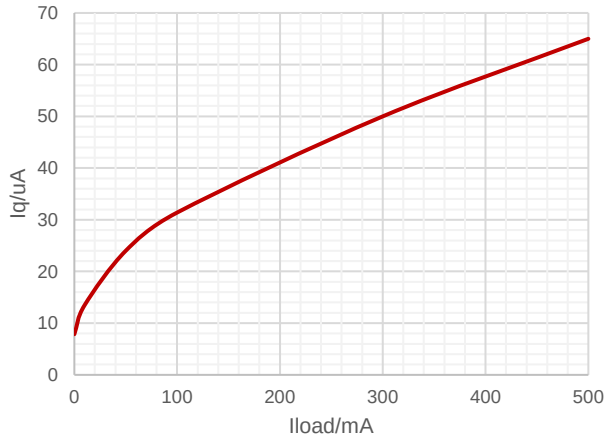


Figure 1. Quiescent Current vs Output Current

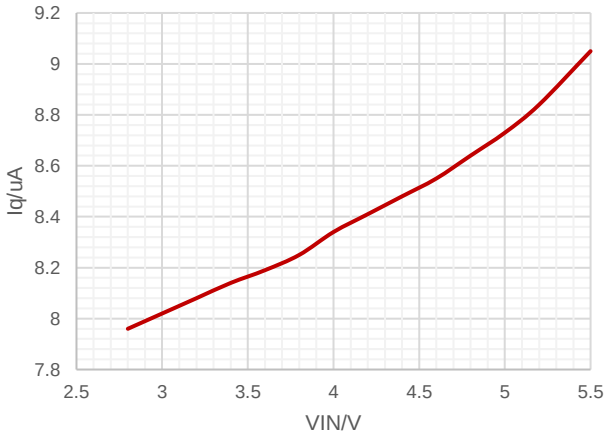


Figure 2. Quiescent Current vs Input Voltage, No load

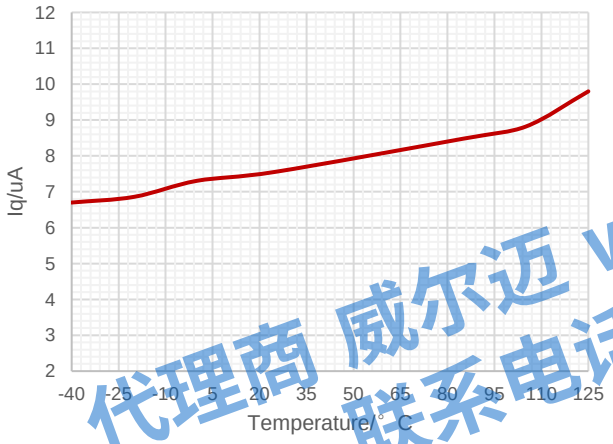


Figure 3. Quiescent Current vs Ambient Temperature

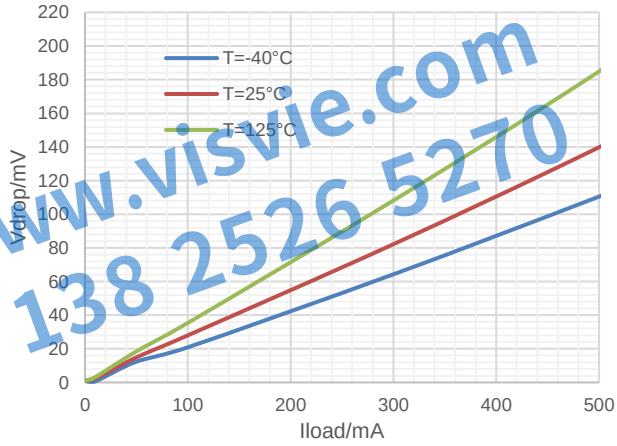


Figure 4. Dropout Voltage vs Output Current

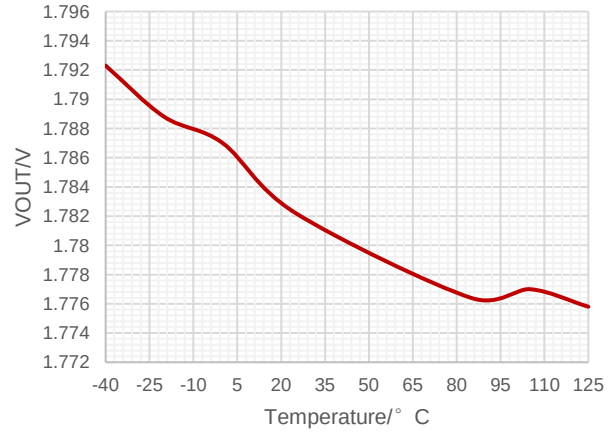


Figure 5. Output Voltage vs Ambient Temperature at VOUT=1.8V

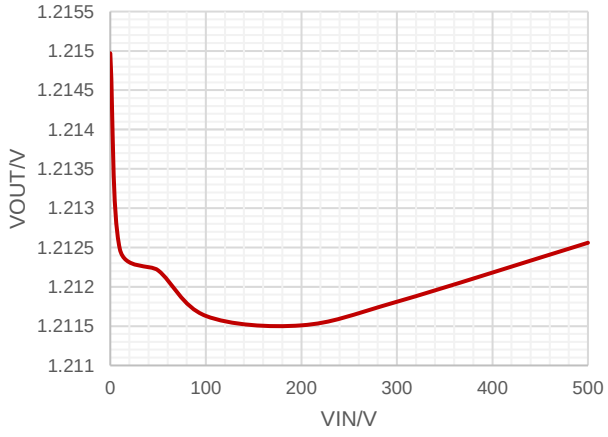


Figure 6. Output Voltage vs Input Voltage

TYPICAL CHARACTERISTICS (continued)

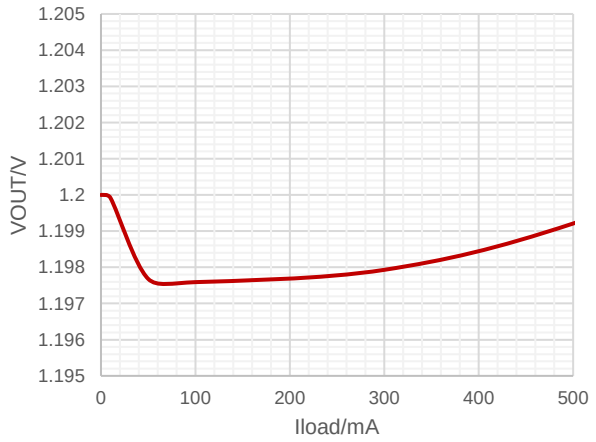


Figure 7. Output Voltage vs Output Current

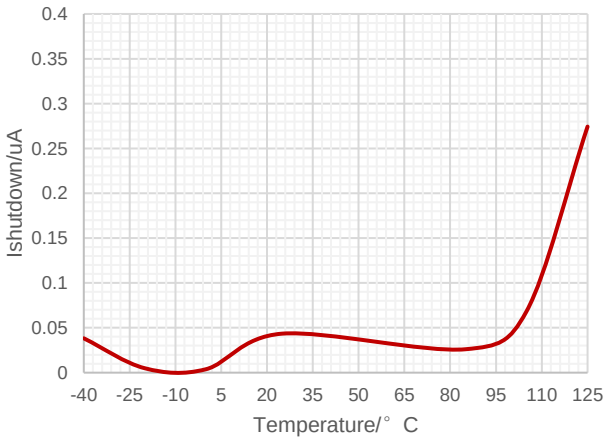


Figure 8. Shutdown Current vs Ambient Temperature

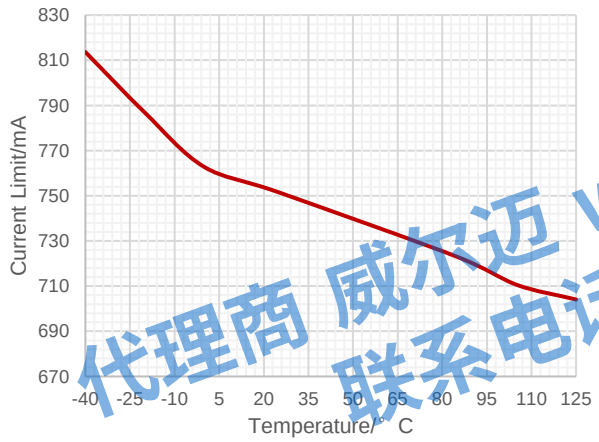


Figure 9. Output Current Limit vs Ambient Temperature

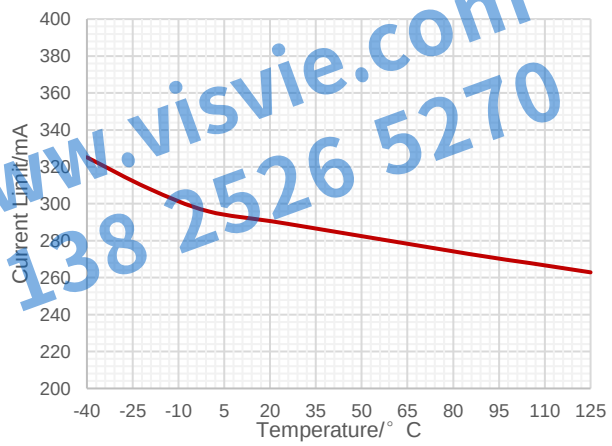


Figure 10. Short Current Limit vs Ambient Temperature

TYPICAL CHARACTERISTICS (continued)

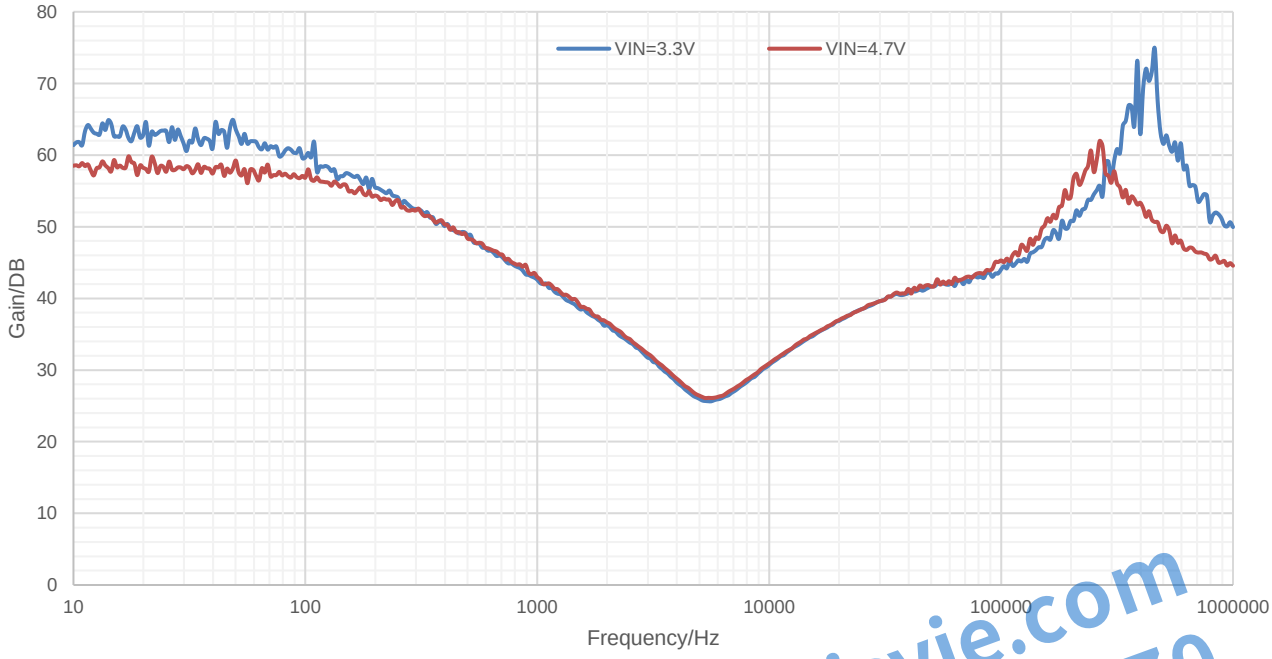


Figure 11. PSRR vs Frequency
VOUT=1.2V,Cf=33pF,COUT=10uF,IOUT=10mA

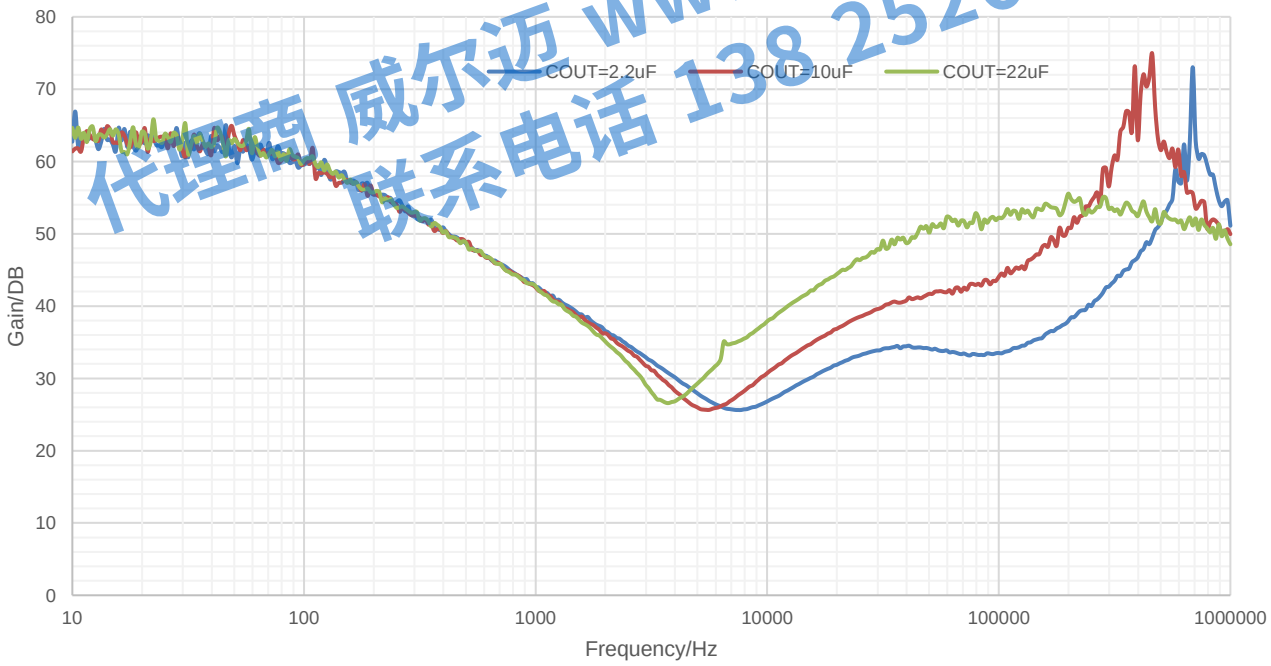


Figure 12. PSRR vs Frequency
VIN=3.3V,VOUT=1.2V,Cf=33pF,IOUT=10mA

TYPICAL CHARACTERISTICS (continued)

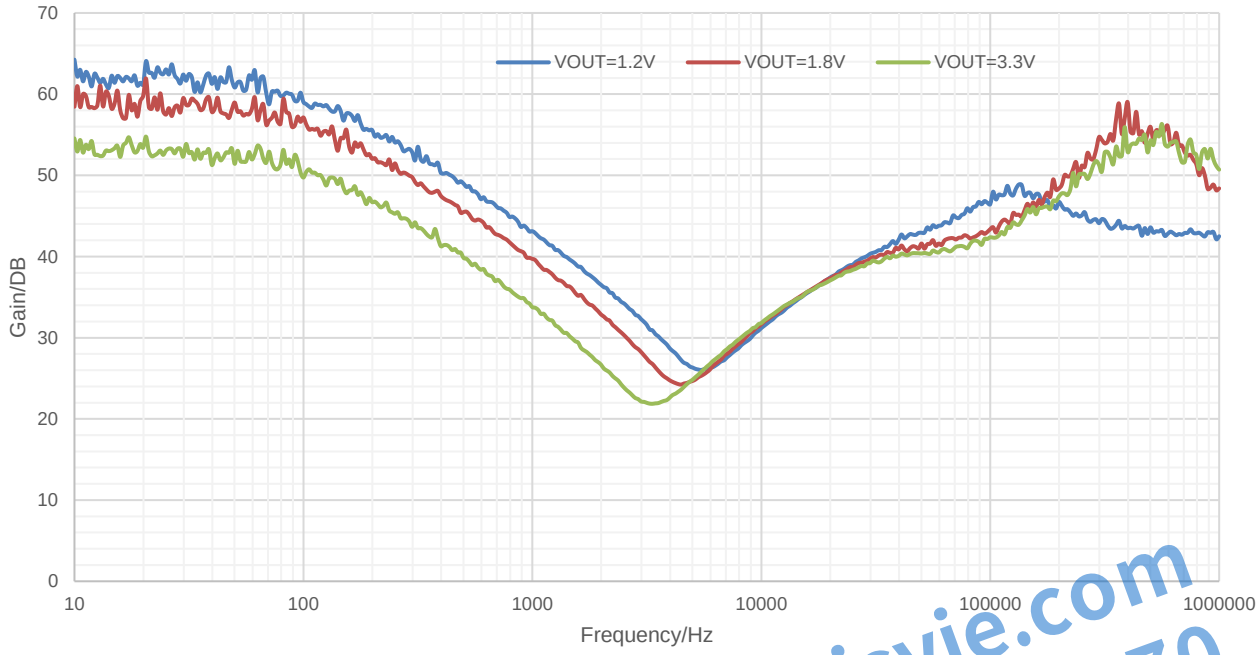


Figure 13. PSRR vs Frequency
VIN=4.3V, Cf=33pF,COUT=10uF,IOUT=10mA

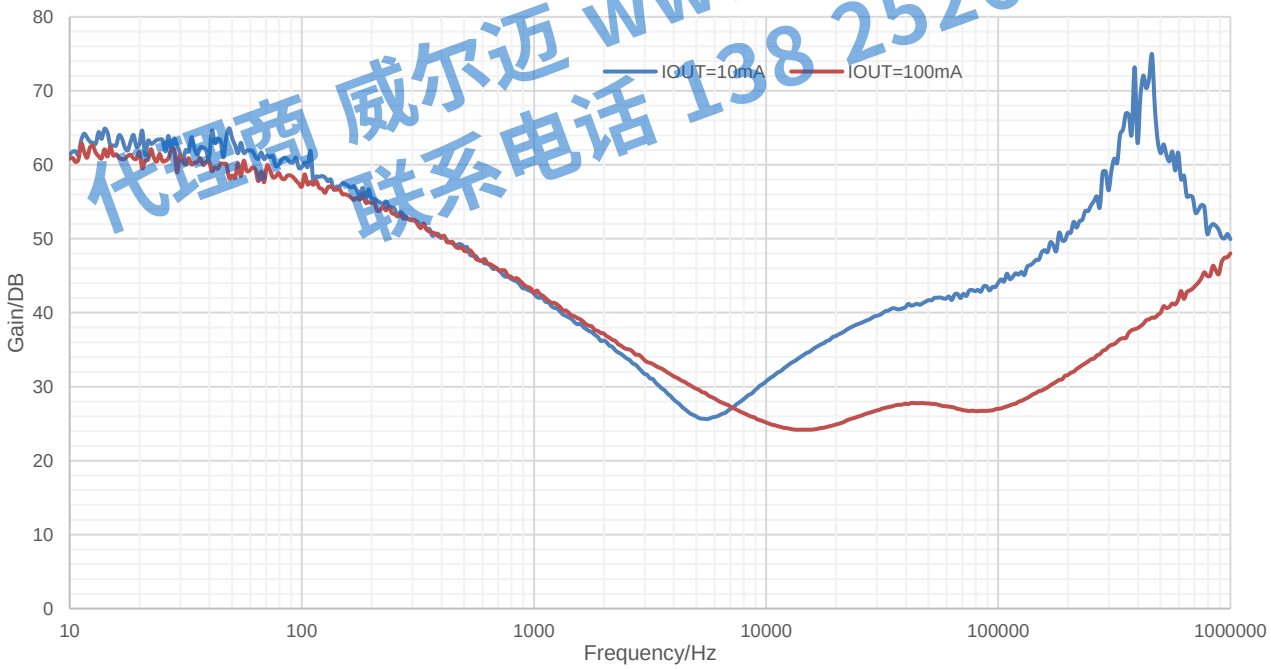


Figure 14. PSRR vs Frequency
VIN=3.3V,VOUT=1.2V,Cf=33pF,COUT=10uF

FUNCTIONAL BLOCK DIAGRAM

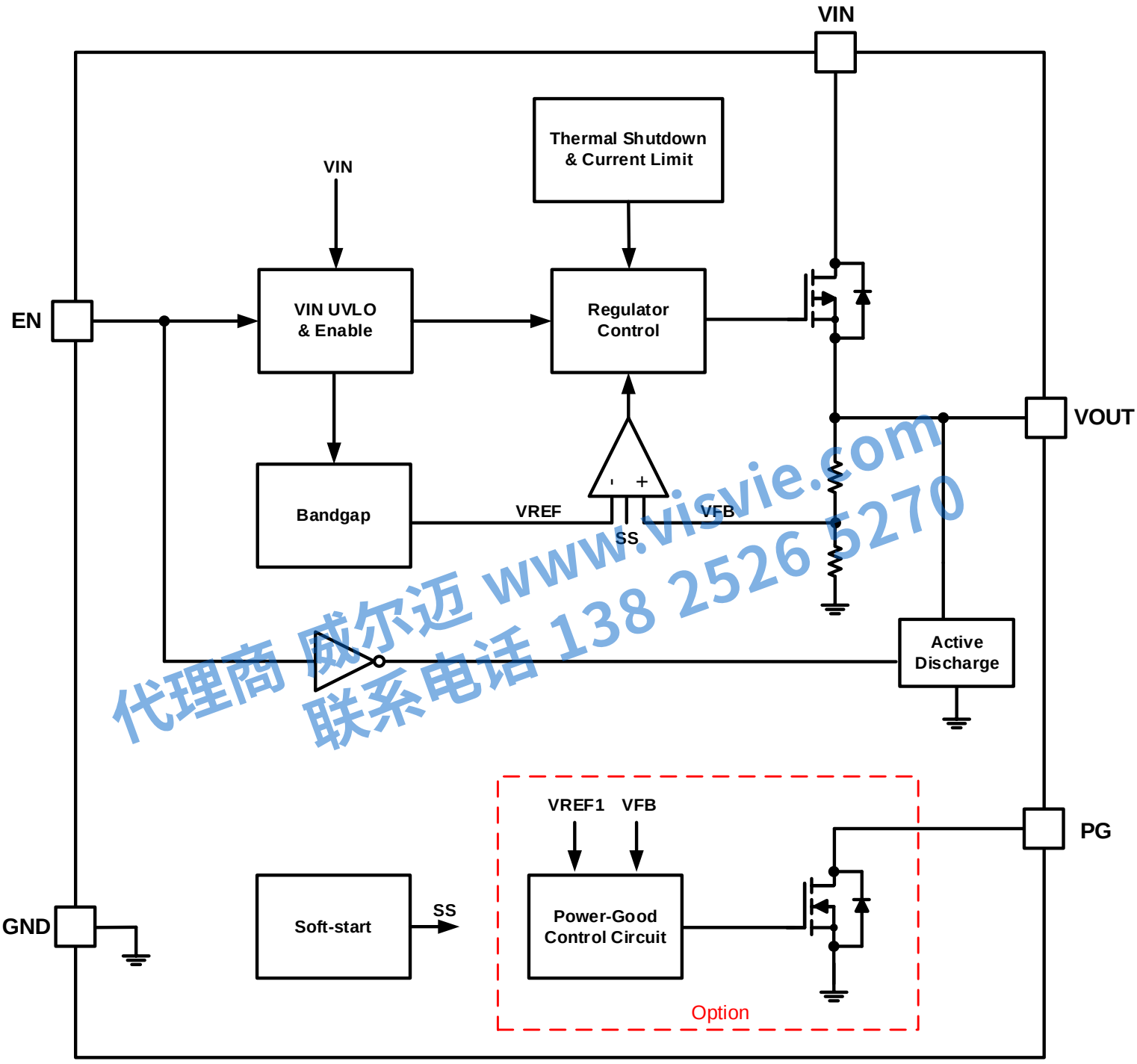


Figure 15. Functional Block Diagram of Fixed Output Version

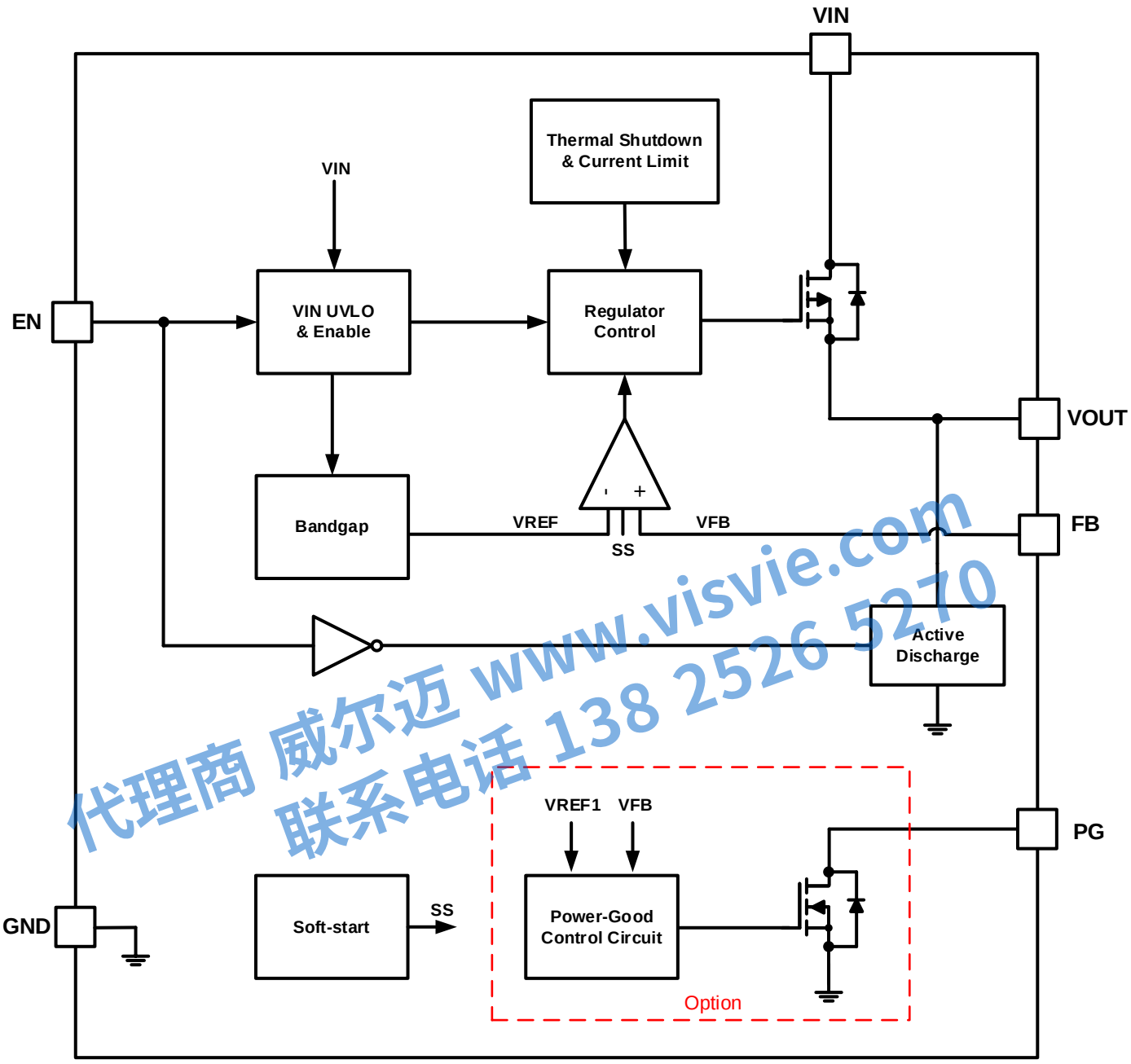


Figure 16. Functional Block Diagram of Adjust Output Version

OPERATION

Overview

The SCT71005Q product are 500mA output current linear regulators with very low quiescent current. These voltage regulators operate from 1.7V to 5.5V DC input voltage with supporting 6V transient input voltage and consume 8μA quiescent current at no load.

The SCT71005Q products are stable with 2.2uF~220uF output capacitors, and 10uF ceramic capacitor is recommended. An internal 2.3ms soft-start time avoids large inrush current and output voltage overshoot during startup.

The SCT71005Q products also provide enable control which is very suitable for the applications needing sequence configuration. Other protection features include the VIN input under-voltage lockout, over current protection, output hard short protection with OCFB and thermal shutdown protection.

The SCT71005Q series products are available in fixed voltage versions of 1.2V、1.8V and 3.3V with 1% output voltage accuracy at room temp and 2% output voltage accuracy over operating conditions.

The SCT71005Q series products also provide adjustable output version which can adjust the output voltage from 0.5V to 5V. The product is available in SOT23-5, TDFN2x2-6, DFN1x1-4 and TDFN2x3-8 packages.

If you need a new output voltage version or a new package option, please feel free to contact SCT sales.

Output Enable

The enable pin (EN) is active high. Enable the device by forcing the voltage of the enable pin to exceed the minimum EN pin high-level input voltage. Turn off the device by forcing the voltage of the enable pin to drop below the maximum EN pin low-level input voltage. If shutdown capability is not required, connect EN to IN.

This EN circuit has an pulldown resistor($R_{EN\_pulldown}$) disconnected to reduce input current when the output is enabled, and connected when EN pin low to disable the output. Floating the EN pin is not suggestion.

Regulated Output Voltage

The SCT71005Q product provide adjustable output which can adjust the output voltage from 0.5V to 5.5V. When the input voltage is higher than $V_{OUT(NOM)}+V_{DROP}$, output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT(NOM)}+V_{DROP}$, output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below UVLO threshold, the output keeps shut off.

If you need a new output voltage version or a new package option, please feel free to contact SCT sales.

Output Discharge

The SCT71005Q product has an internal pulldown MOSFET that connects an $R_{discharge}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin.

Do not rely on the active discharge circuit to discharge the output voltage after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device, especially when a large output capacitor is used. Limit reverse current to no more than 5% of the device rated current for a short period of time.

Over Current Limit and Foldback Current Limit

The SCT71005Q product has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{OC}). When the output voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current limit. When

the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{OC} and I_{SC} are listed in the Electrical Characteristics table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN}–V_{OUT})×I_{OC}]. When the output is shorted and the output voltage is less than $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN}–V_{OUT})×I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown.

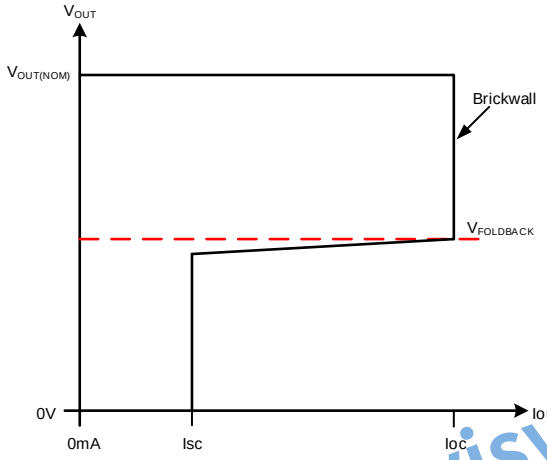


Figure 17. Current Limit with Foldback Feature

Internal Soft-Start

The SCT71005Q product integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 2.3ms. If the EN pin is pulled below 0.607V, LDO will be shut off and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Below figure shows the startup waveform at small output capacitor and large output capacitor. When output capacitor is small, for example 10uF, the slope of VOUT is limit by soft-start. When output capacitor is large, for example 100uF, the slope of VOUT is limited by foldback current limit (I_{SC}) at VOUT<$V_{FOLDBACK}$, and the slope of VOUT is limited by over current limit (I_{OC}), when VOUT> $V_{FOLDBACK}$.

In SCT71005Q product, typical Tss is 2.3ms, and typical I_{OC} is 800mA and typical Isc is 290mA, could use the following formula for initial startup time calculation.

$$\text{Tstart} = \max\left\{\frac{C_{OUT}\times 0.9\times V_{OUT}}{(I_{sc}-I_{load})} + \frac{C_{OUT}\times 0.9\times V_{OUT}}{(I_{oc}-I_{load})}, T_{SS}\right\} \quad (1)$$

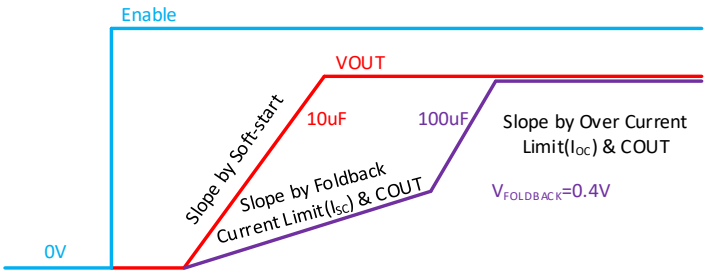


Figure 18. Soft-start Waveform vs Output Capacitor

Power-Good and Power-Good Delay

The power-good (PG) pin is an open-drain output and can be connected to any 5V or lower rail through an external pull-up resistor. The PG output is high-impedance when VOUT is greater than the PG trip threshold (V_{PG_R}=90% x $V_{OUT(NOM)}$). If VOUT drops below V_{PG_F}=80% x $V_{OUT(NOM)}$, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

The power-good delay time ($Td_{\_PGR}$) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{PG_R}) to when the PG output is high. This power-good delay time is set by an internal time, which is167us typical. The power-good deglitch time ($Td_{\_PGF}$) is defined as the time period from when V_{OUT} fall below the PG trip threshold voltage (V_{PG_F}) to when the PG output is low. This power-good deglitch time is set by an internal time, which is 66us typical. If the power-good delay time is not enough for some application, could try to connect a capacitor from PG pin to GND and using PG pull-up resistor and this capacitor generate extra delay time to meet your design.

To ensure proper operation of the power-good feature, maintain V_{IN}≥ 1.7V (V_{IN_MIN}). It allows connections of PG pin to circuit with the same or different power supply voltage to the LDO's VOUT level. Below are the connections examples.

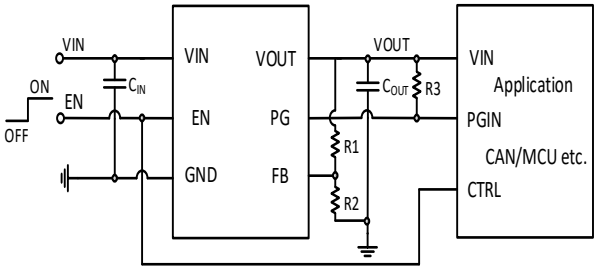


Figure 19. PG Connected to LDO's Ouput

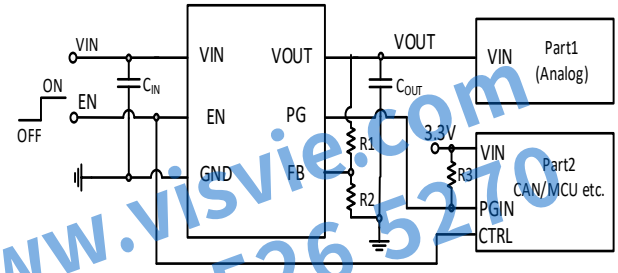


Figure 20. PG Connected to the other Power Supply

Below figure shows the startup and shutdown situation when slow power up and power down.

At the point 0, the input voltage starts to rise from 0 to 5V, LDO is in shutdown (because VIN is below its UVLO threshold) and output voltage is 0V.

At the point 1, the VIN voltage reaches UVLO threshold level and LDO starts charging of output capacitor. VOUT rising speed is defined by internal soft-start function.

At the point 2, the VOUT voltage reaches almost the VIN voltage as it rises faster and LDO gets into dropout region. The difference between VIN and VOUT is the dropout voltage.

At the point 3, the VOUT reaches PG threshold (V_{PG_R}=90% x $V_{OUT(NOM)}$) and from this point LDO counts the power good delay time ($Td_{\_PGR}$). After this delay, the PG pin rises to high level showing that VOUT is ok.

At the point 4, the VOUT reaches its nominal value (3.3V) as the VIN starts to be higher than ($V_{OUT(NOM)}$ + V_{DROP}) and LDO gets into regulation region.

At the point 5, as the VIN voltage slow power down and LDO returns to dropout region again.

At the point 6, the VOUT drops below PG threshold (V_{PG_F}=80% x $V_{OUT(NOM)}$) and LDO starts counting the power good deglitch time ($Td_{\_PGF}$), which filters fast VOUT undershoots(caused for example by line/load transient responses).After this delay, the PG output is shorted to 0 V level to highlight "power fail" state.

At the point 7, the VIN voltage is lower than input voltage UVLO threshold minus UVLO hysteresis level and LDO goes into the shutdown state.

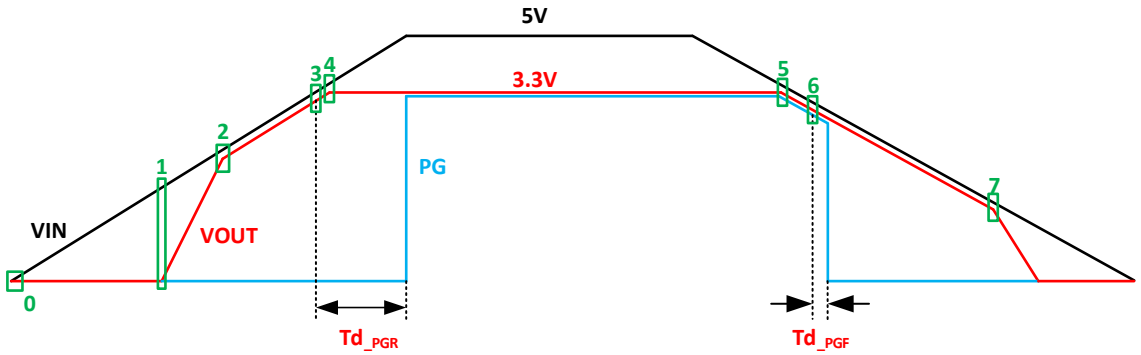


Figure 21. Startup and Shutdown Example —SCT71005Q Series

Thermal Shutdown

This device incorporates a thermal shutdown (T_{SD}) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the T_{SD} trip point. The junction temperature exceeding the T_{SD} trip point causes the output to turn off. When the junction temperature falls below the T_{SD} trip point minus thermal shutdown hysteresis, the output turns on again.

APPLICATION INFORMATION

Typical application 1:

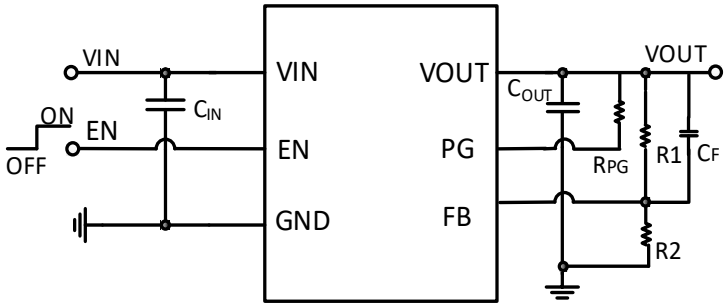


Figure 22. SCT71005Q Typical Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal, 1.7V~5.5V
Output Voltage	0.5V~5.5V
Maximum Output Current	500mA
Output Capacitor Range (C_{OUT})	2.2uF~22uF , recommends 10uF
Input Capacitor Range (C_{IN})	>2.2uF , recommends 10uF

Typical application 2:

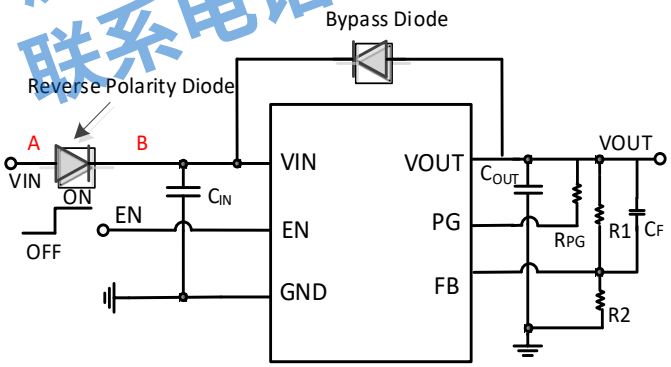


Figure 23. SCT71005Q Typical Application Schematic with Reverse Polarity Diode

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal, 1.7V~5.5V
Output Voltage	0.5V~5.5V
Maximum Output Current	500mA
Output Capacitor Range (C_{OUT})	2.2uF~22uF , recommends 10uF
Input Capacitor Range (C_{IN})	>2.2uF , recommends 10uF

In some applications, the VIN and the VOUT potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VOUT to the VIN when the VIN shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 220μF. Also by inserting a reverse polarity diode in to the VIN, it can prevent reverse current from reverse battery connection or the case, when the point A is short-circuited GND. If there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VIN and the VOUT.

Typical application 3:

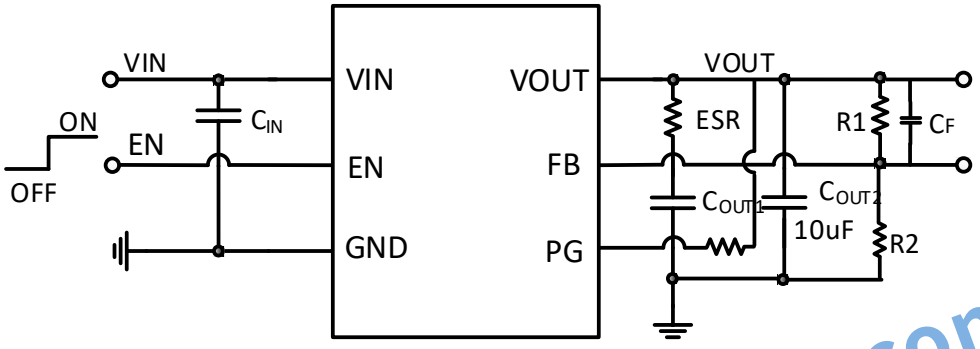


Figure 24. SCT71005Q Typical Application Schematic with Large Output Capacitor

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal, 1.7V~5.5V
Output Voltage	0.5V~5.5V
Maximum Output Current	500mA
Output Capacitor Range (C_{OUT1} and ESR)	2.2uF~220uF with ESR=0.5Ω~5Ω
Output Capacitor Range (C_{OUT2})	recommends 10uF with low ESR
Input Capacitor Range (C_{IN})	>2.2uF , recommends 10uF

Typical application 4:

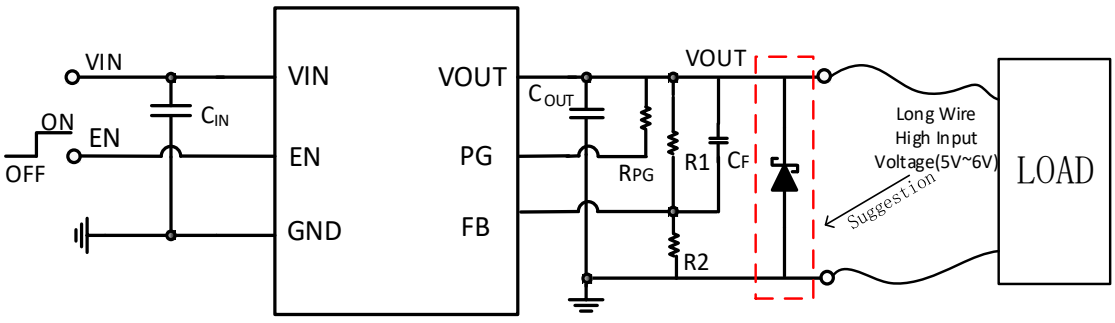


Figure 24. SCT71005Q Typical Application Schematic with Long Wire and High Input Voltage

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal, 1.7V~5.5V
Output Voltage	0.5V~5.5V
Maximum Output Current	500mA
Output Capacitor Range (C_{OUT1} and ESR)	2.2uF~220uF with ESR=0.5Ω~5Ω
Output Capacitor Range (C_{OUT2})	recommends 10uF with low ESR
Input Capacitor Range (C_{IN})	>2.2uF , recommends 10uF

A Schottlky diode is suggested between VOUT and GND under the applications of hard short event at high input voltage when big distance exists between the device and loads.

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 100kΩ. Use equation 2 to calculate R1.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_2 \quad (2)$$

where:

- V_{REF} is the feedback reference voltage, for SCT71005A01Q is 700mV and SCT71005A02Q is 500mV

Table 1: Compensation Values for Typical Output Voltage/Capacitor Combinations (SCT71005A01Q)

Vout/V	COUT/uF	Cf/pF	R1/kΩ	R2/kΩ	COUT1/uF (optional)	ESR/Ω
1.2	10	33	71.5	100	220	1
1.8	10	33	158	100	220	1
2.4	10	33	243	100	220	1
3.3	10	33	374	100	220	1
5	10	33	619	100	220	1

Table 2: Compensation Values for Typical Output Voltage/Capacitor Combinations (SCT71005A02Q)

Vout/V	COUT/uF	Cf/pF	R1/kΩ	R2/kΩ	COUT1/uF (optional)	ESR/Ω
1.2	10	33	140	100	220	1
1.8	10	33	261	100	220	1
2.4	10	33	383	100	220	1
3.3	10	33	562	100	220	1
5	10	33	909	100	220	1

Input Capacitor and Output Capacitor

SCT recommends adding a 2.2μF or greater capacitor with a 0.1μF bypass capacitor in parallel at VIN pin to keep the input voltage stable. Aluminum electrolytic capacitor or other capacitor with high capacitance is suggested for the system power with large voltage spike. The voltage rating of the capacitors must be greater than the maximum input voltage

To ensure loop stability, the SCT71005Q product requires an output capacitor with a minimum effective capacitance value of 2.2μF. And the product could support output capacitor range from 2.2uF to 220uF and with an ESR range between 0.001Ω and 5Ω. SCT recommends selecting a X5R- or X7R-type 4.7uF~10uF ceramic capacitor with low ESR over temperature range to improve the load transient response.

To further improve loop stability, we recommend using feed forward capacitors. The specific values can refer to the Figure25 and Figure26.

When using large output capacitor with higher ESR resistor, for example 100uF output electrolytic capacitor with 1Ω ESR resistor in the application, SCT recommends adding extra 10uF low ESR output capacitor parallel connection with the large electrolytic capacitor, this will eliminate the undershoot/overshoot voltage caused by the large ESR resistor and get better load transient performance.

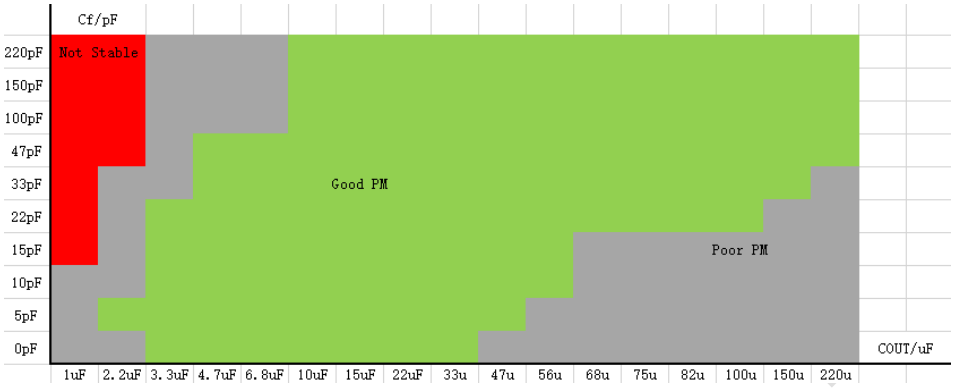


Figure 25. SCT71005Q Feed Forward Capacitors recommend(R2=100kΩ,VOUT=1.8V)

Figure 26. SCT71005Q Feed Forward Capacitors recommend(R2=10kΩ,VOUT=1.8V)

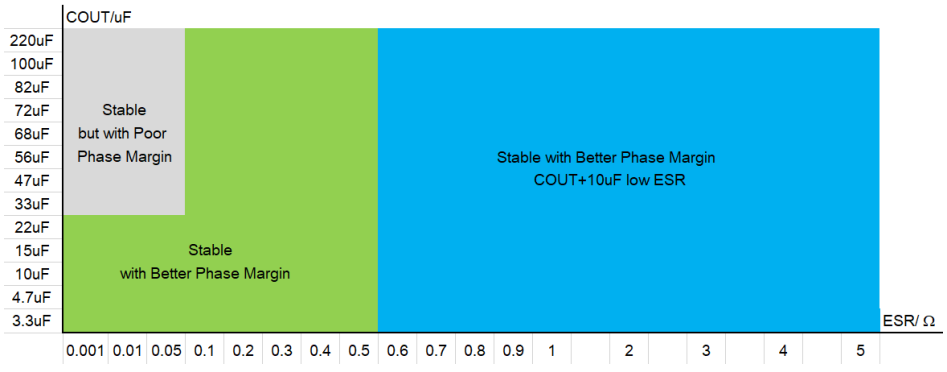


Figure 27. SCT71005 Stability vs Output Capacitor(Fixed Output)

Power Dissipation and Thermal Performance

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum junction temperature is dependent on power dissipation, package, the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

During normal operation, LDO junction temperature should not exceed 150°C, or else it may result in deterioration of the properties of the chip. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 3. Because I_{GND} « I_{OUT}, the term V_{IN} x I_{GND} in Equation 3 could be ignored.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (3)$$

The junction temperature can be estimated using Equation 4. $R_{\theta JA\_EVM}$ is the junction-to-ambient thermal resistance based on customer's PCB. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature T_J.

$$T_J = T_A + P_D \times R_{\theta JA\_EVM} \quad (4)$$

$R_{\theta JA\_EVM}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

For the SCT71005Q series products, the maximum allowable power dissipation of different packages was listed in the following table, and the test results are based on our EVM board, larger power dissipation will trigger thermal shutdown protection. As a result, we could calculate the $R_{\theta JA\_EVM}$ of different packages. The following table is just for your reference based on our EVM test, please leave enough margin when you design thermal performance.

The PCB information of our EVM: 4-layer,1oz Cu (inner 0.5oz Cu), 50mm x 30mm size.2-layer(only for DFN1X1-4), 1oz Cu, 50mm x 30mm size.

Thermal Performance of Different Packages Based on EVM Test

Package	Max Allowable PD (W) (Not Trigger TSD,VOUT=5V)	Max Allowable PD (W) (TJ≤150℃)	$R_{\theta JA\_EVM}$ (℃/W)
SOT23-5	TBD	TBD	TBD
TDFN2X2-6	TBD	TBD	TBD
TDFN2X3-8	2.46	2.12	59.04
DFN1X1-4 (2-layer)	TBD	TBD	TBD

THERMAL CHARACTERISTICS

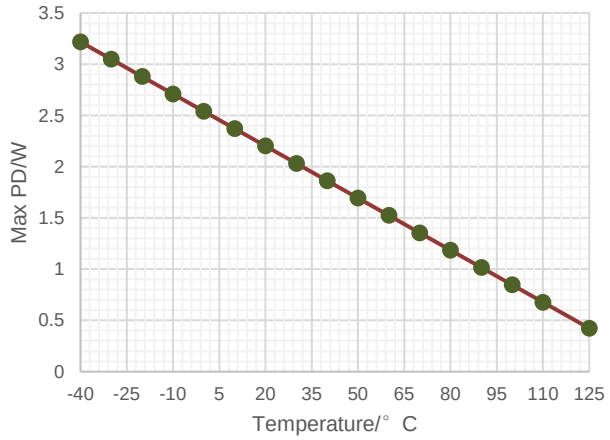


Figure 28. Maximum Allowed Power Dissipation vs Ambient Temperature, TDFN2X3,TJ ≤ 150℃

Application Waveforms

Vin=Vout +1V, unless otherwise noted

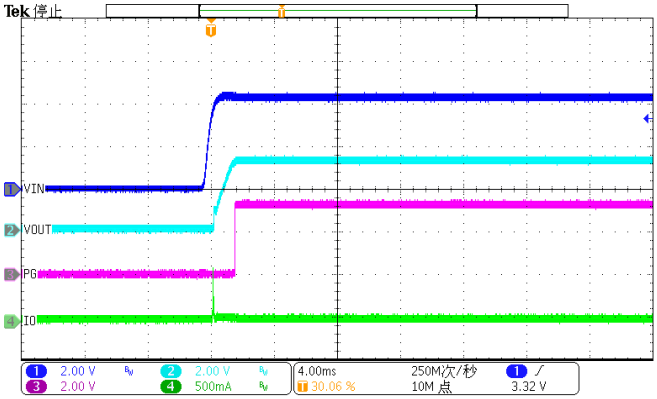


Figure 29. Power up (Iload=10mA)

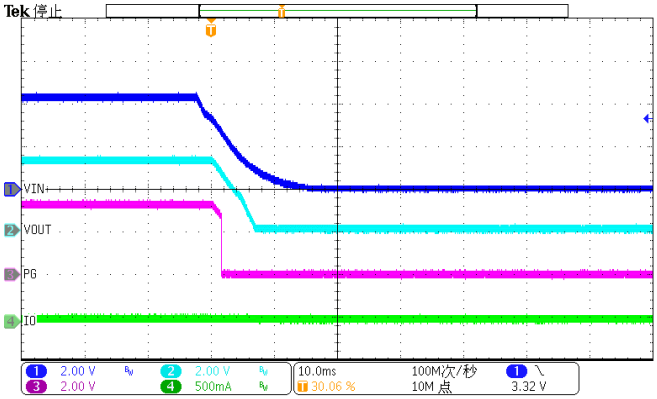


Figure 30. Power down (Iload=10mA)

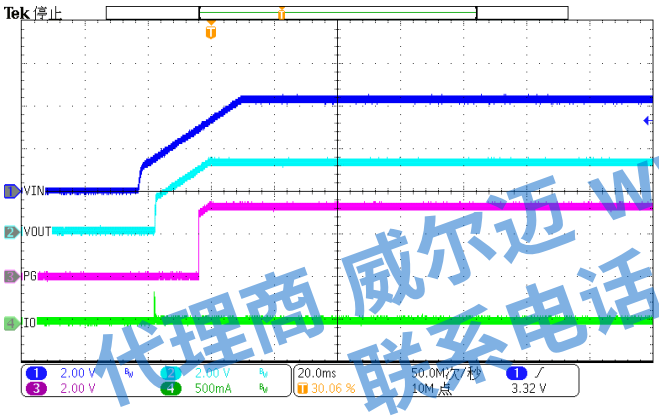


Figure 31. Slow Power up (Iload=10mA)

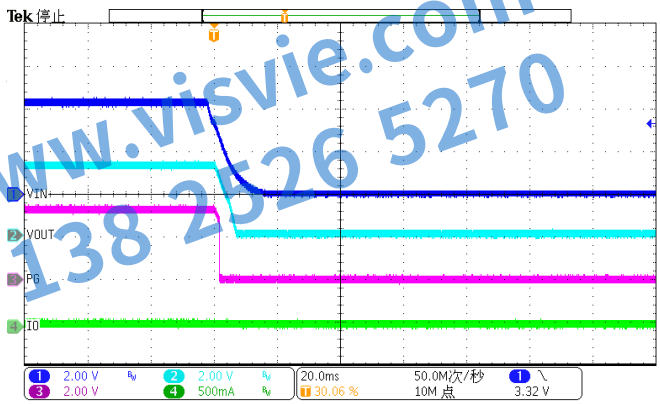


Figure 32. Slow Power down (Iload=10mA)

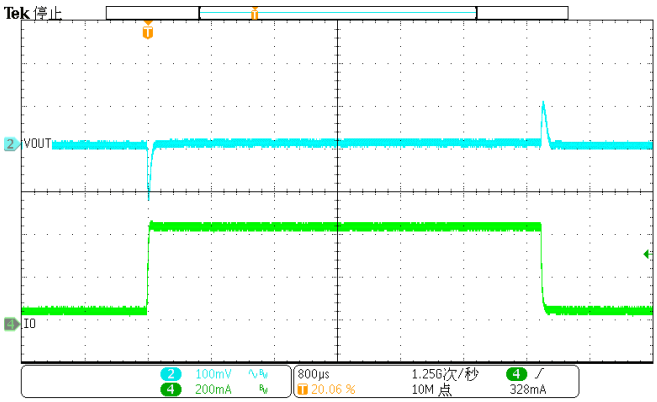


Figure 33. DC-DC Load Transient (50mA-450mA),VOUT=3.3V

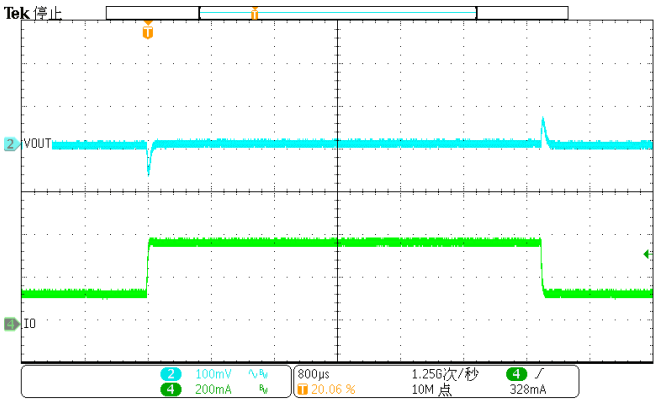


Figure 34. DC-DC Load Transient (130mA-370mA),V_{OUT}=3.3V

Application Waveforms(Continued)

Vin=Vout +1V, unless otherwise noted

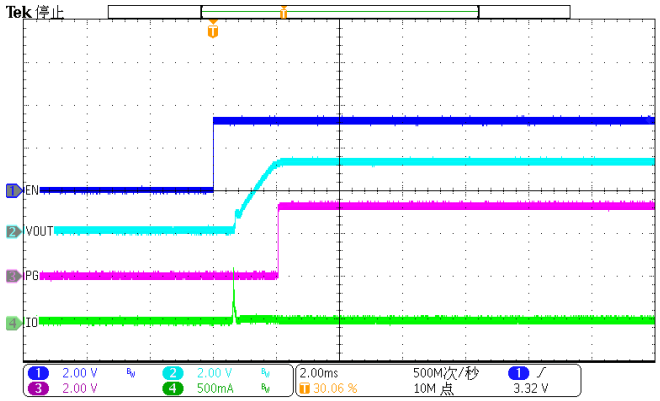


Figure 35. Enable (Iload=10mA)

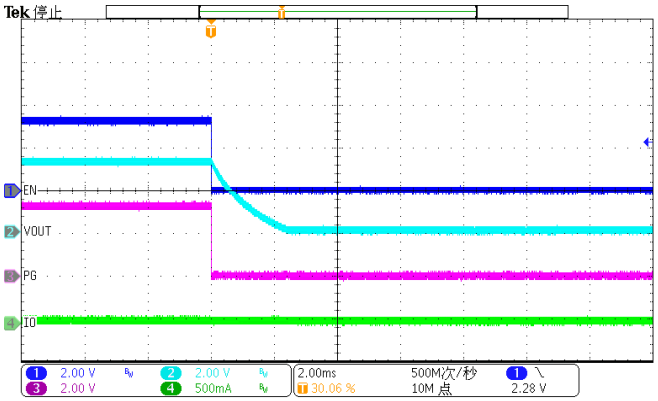


Figure 36. Disable (Iload=10mA)

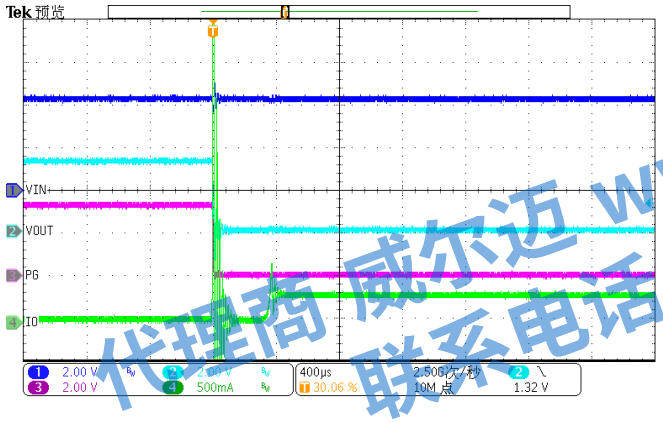


Figure 37. Enter Short Circuit Protection

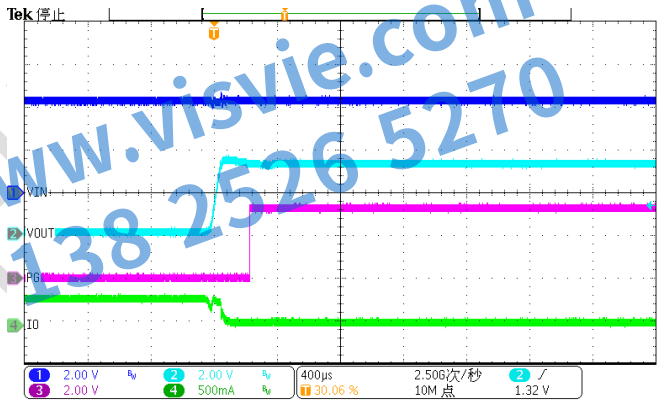


Figure 38. Exit Short Circuit Protection

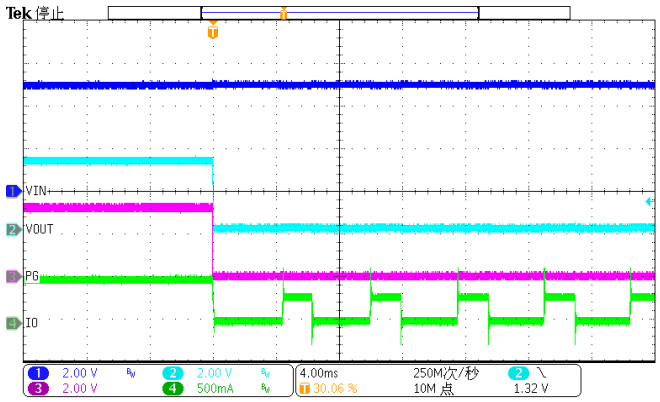


Figure 39. Enter Over Temperature Protection(Vin=5.5V)

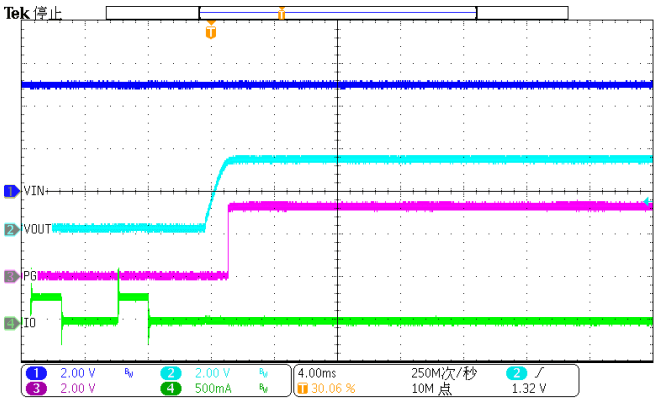


Figure 40. Exit Over Temperature Protection(Vin=5.5V)

Layout Guideline

Proper PCB layout is a critical for SCT71005Q's stability, transient performance and good regulation characteristics. For better results, follow these guidelines as below:

1. Both input capacitors and output capacitors must be placed as close to the device pins as possible.
2. It is recommended to bypass the input pin to ground with a 0.1μF bypass capacitor. The loop area formed by the bypass capacitor connection, V_{IN} pin and the GND pin of the system must be as small as possible.
3. It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.
4. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, SCT recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad.
5. If using large electrolytic capacitor with high ESR resistor, SCT recommends adding a 10uF low ESR capacitor parallel connection with the large electrolytic capacitor.

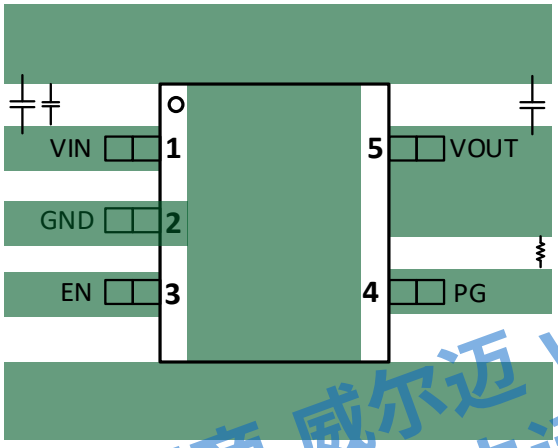


Figure 41. PCB Layout Example

SCT71005FxxQTWDR

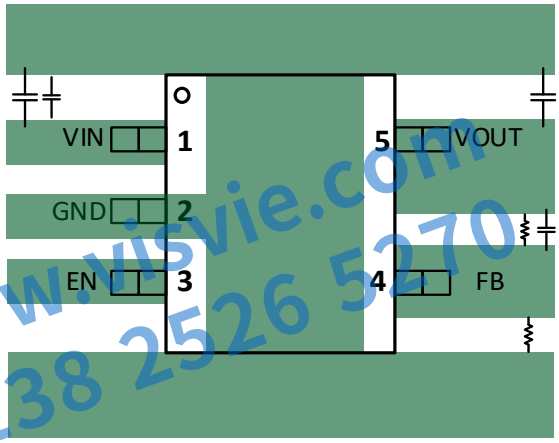


Figure 42. PCB Layout Example

SCT71005A01QTWDR

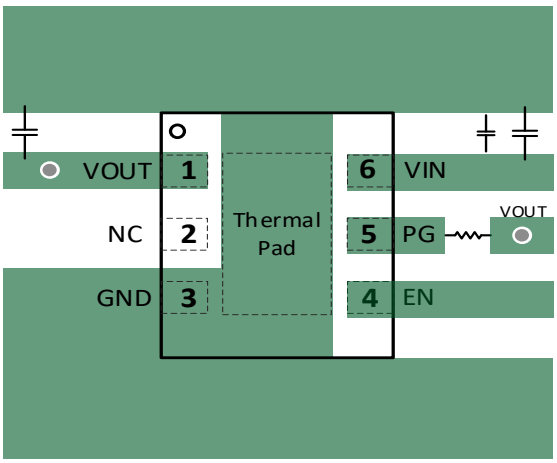


Figure 4. PCB Layout Example

SCT71005FxxQDVAR

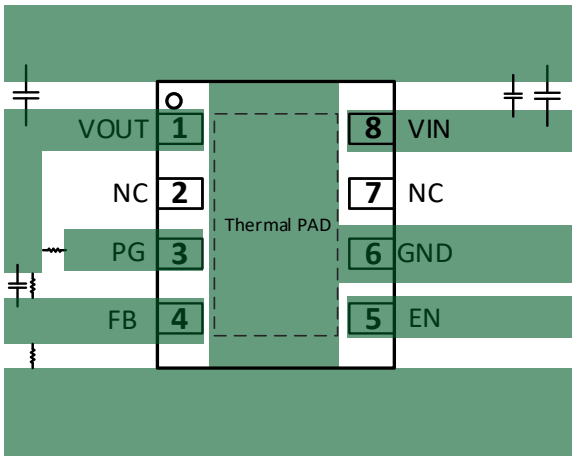
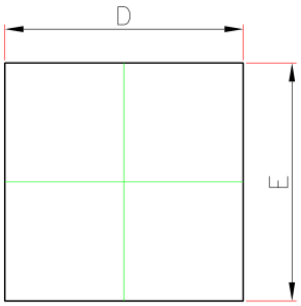


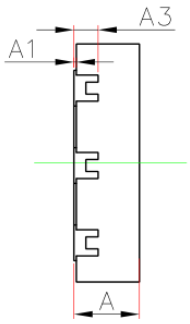
Figure 5. PCB Layout Example

SCT71005A02QDTDR

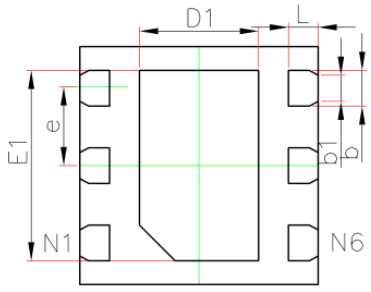
PACKAGE INFORMATION



TOP VIEW



SIDE VIEW



BOTTOM VIEW

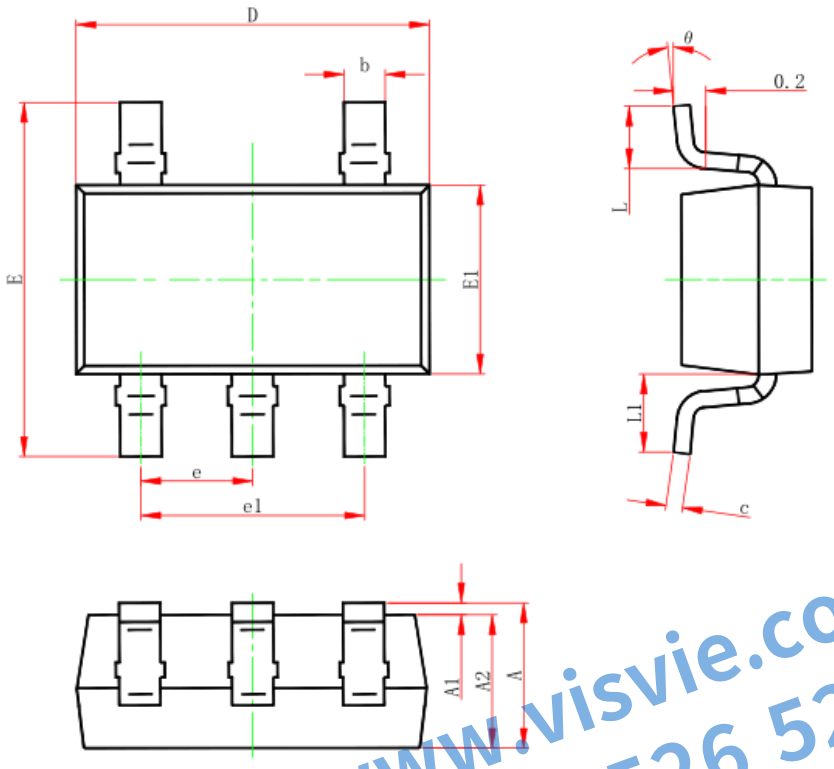
TDFN2x2-6 Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF		0.008 REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.900	1.100	0.035	0.043
E1	1.500	1.700	0.059	0.067
b	0.250	0.350	0.010	0.014
b1	0.220 REF.		0.009 REF.	
e	0.650 BSC.		0.026 BSC.	
L	0.174	0.326	0.007	0.013

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

PACKAGE INFORMATION



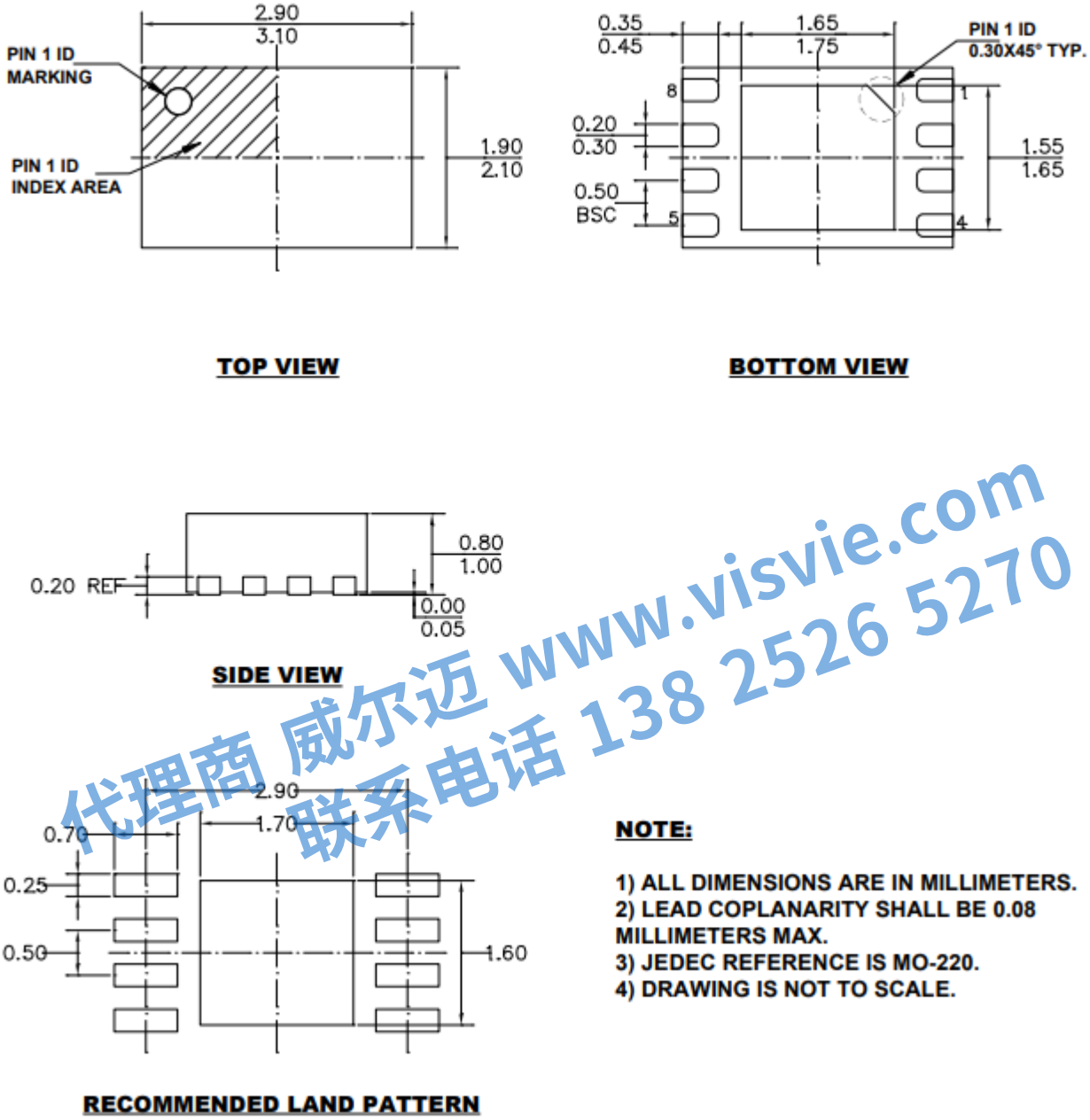
SOT23-5 Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600 REF		0.024 REF	
θ	0°	8°	0°	8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

PACKAGE INFORMATION



NOTE:

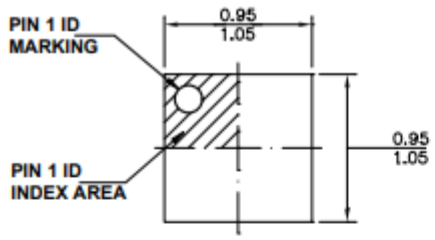
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

TDFN2x3-8 Package Outline Dimensions

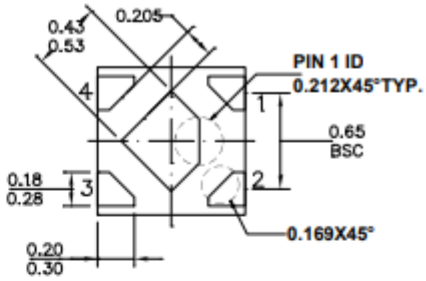
NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

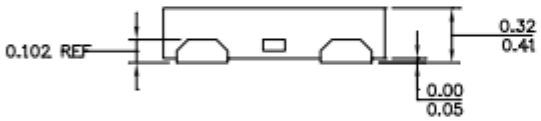
PACKAGE INFORMATION



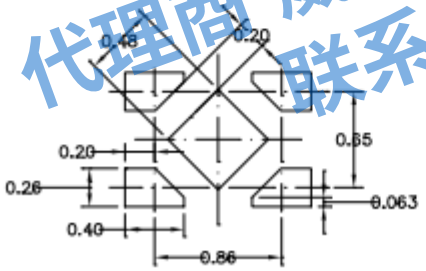
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

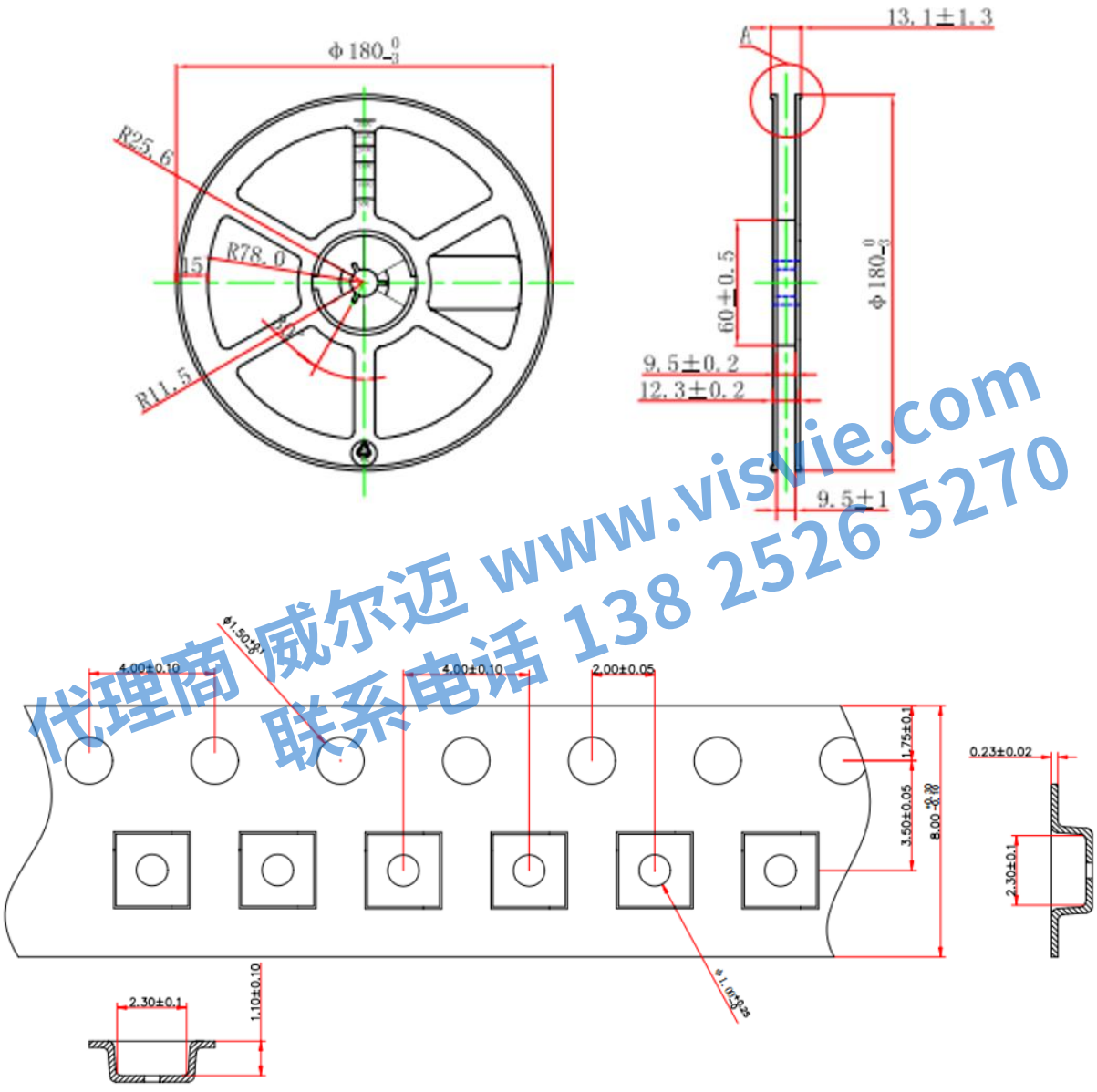
DFN1x1-4 Package Outline Dimensions

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT71005Q Series	TDFN2x2-6	6	3000



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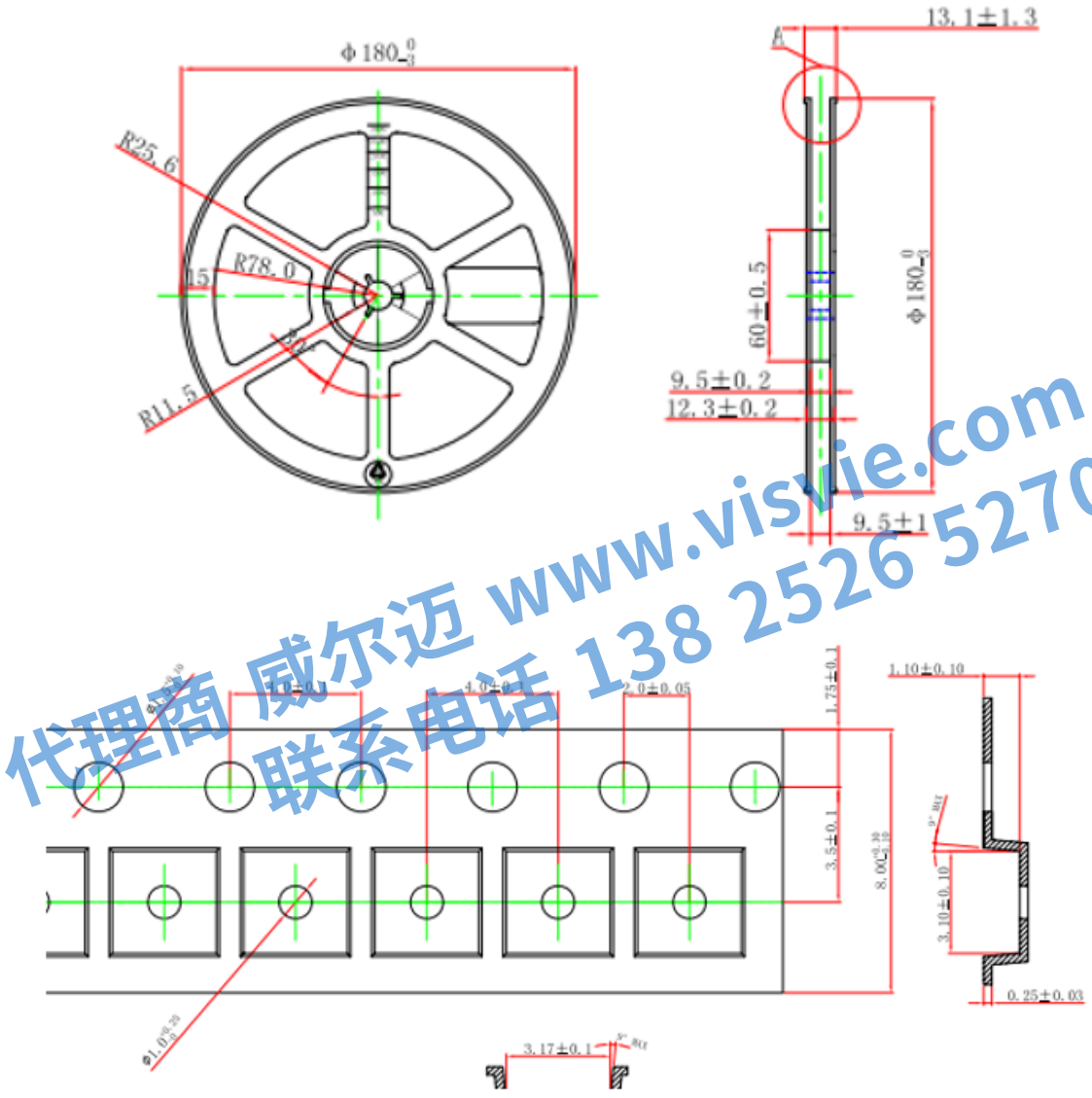
TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT71005Q Series	SOT23-5	5	3000



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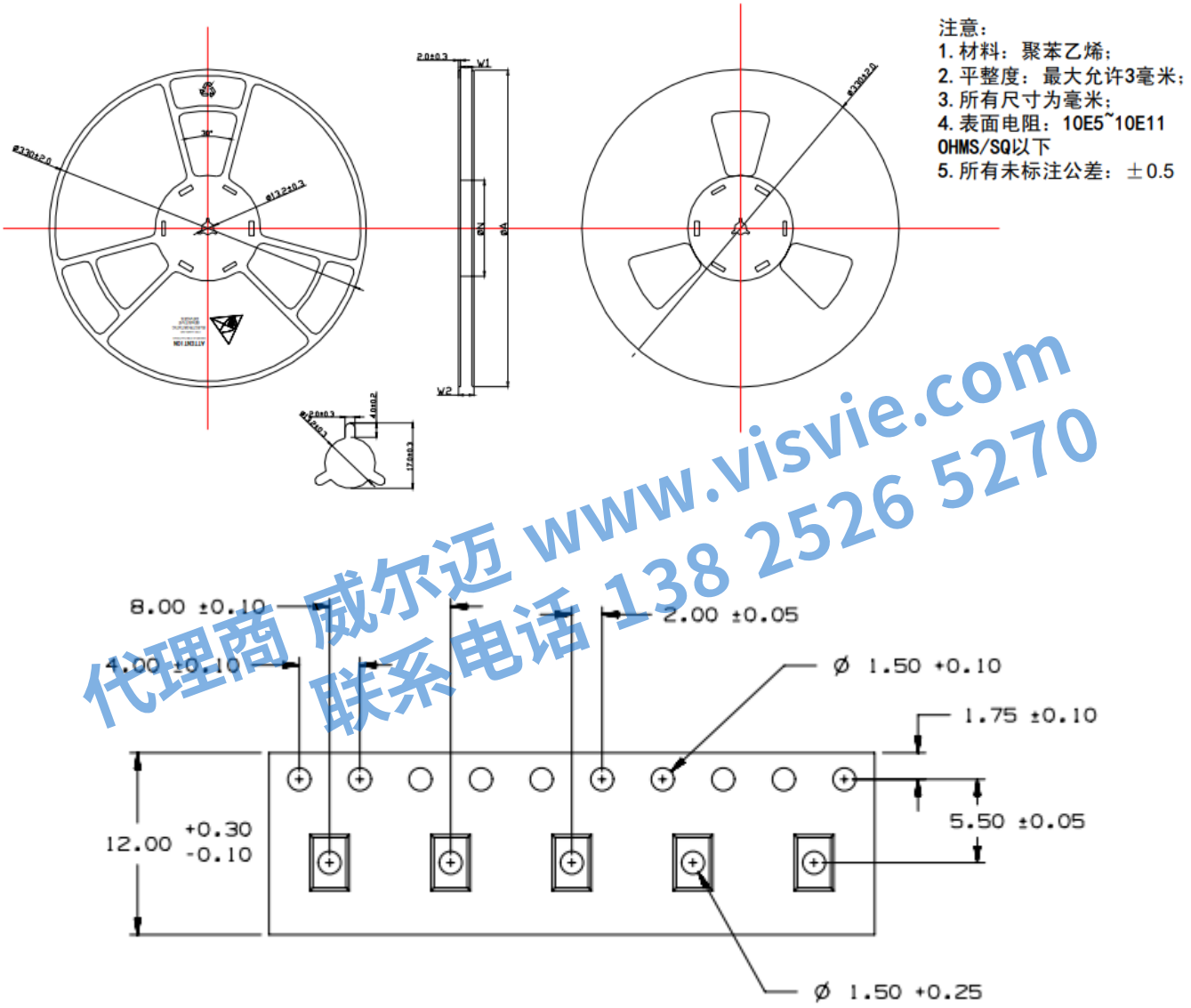
TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT71005Q Series	TDFN2x3-8	8	5000



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