# 3V-40V Vin, 200mA, Ultra-Low Quiescent Current LDO with Adjustable Output Voltage

## FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C5
- Wide Input Range: 3V-40V
- With up to 45V Transient Input Voltage
- Maximum Output Current: 200mA
- Output Voltage: 1.215V~25V
- Output Voltage Accuracy:
  - $T_J$= 25℃：±1%
  - $T_J$= -40℃~ 150℃：±2%
- Ultra-Low Quiescent Current: 2.6μA
- Low Dropout Voltage：
  - 270mV at 200mA load current
- Support Output Capacitors Range:
  - 3.3uF~220uF
  - Low-ESR: 0.001Ω~ 5 Ω
- 1.5ms Internal Soft-start Time
- Current Limit Protection with VIN_HIGH Control
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Over-Temperature Protection
- Available Package：TDFN3X3-8

## APPLICATIONS

- Automotive Head Units
- Headlights
- Body Control Modules
- Inverter and Motor Controls

## DESCRIPTION

The SCT71402Q series products is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3V to 40V and 200mA output current with enable control. The SCT71402Q series products is stable with 3.3uF~220uF output capacitors, and 10uF ceramic capacitor is recommended.

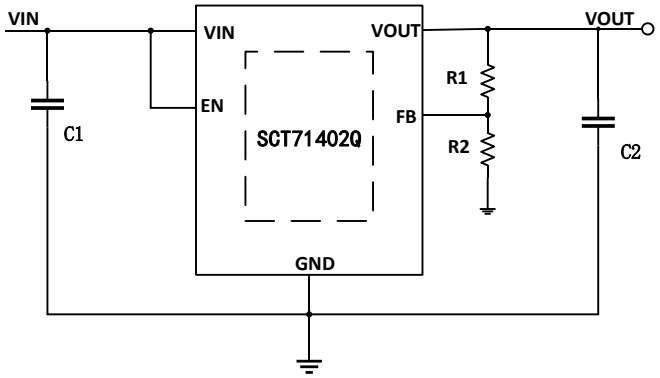
Only 2.6-μA typical quiescent current at light load makes the SCT71402Q series products ideal choices for portable devices with battery power supply and an optimal solution for powering microcontrollers (MCUs) and CAN/LIN transceivers in always-on systems.

The SCT71402Q series products integrated short-circuit and overcurrent protection with VIN_HIGH Control feature, which makes the device more reliable during transient high-load current faults or shorting events.

The SCT71402Q series products provide adjustable output voltage which can adjust the output voltage from 1.215V to 25V.

The SCT71402Q series products is available in TDFN3X3-8 package, for other package options, please contact SCT sales.

## TYPICAL APPLICATION



## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Sampling.

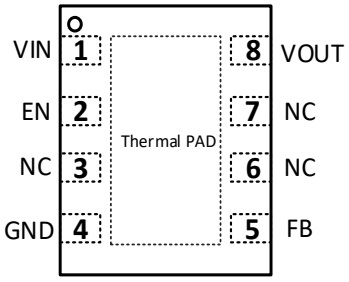
Revision 0.81: Update the curve of the temperature data and Part Number.

## DEVICE ORDER INFORMATION

| Part Number | Output Voltage | Package | Package Marking | Transport Media, Quantity |
|---|---|---|---|---|
| SCT71402A00QDTBR | Adjustable | TDFN3x3-8 | 2A00Q | Tape & Reel, 5000 |

## PIN CONFIGURATION




**SCT71402A00QDTBR**

TDFN3x3-8 Package

## PIN FUNCTIONS

| NAME | PIN NUMBER | PIN FUNCTION |
|---|---|---|
| | TDFN3x3-8 | |
| VIN | 1 | Input voltage pin |
| EN | 2 | Enable input pin |
| NC | 3,6,7 | No connection |
| GND | 4 | Ground reference pin |
| FB | 5 | Feedback Input for Output Adjustable Version |
| VOUT | 8 | Regulated output voltage pin |

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 3 | 40 | V |
| $V_{OUT}$ | Adjustable Output Version | 1.215 | 25 | V |
| $V_{EN}$ | Enable input voltage | 0 | $V_{IN}$ | V |
| $C_{IN}$ | Input capacitor | 2.2 | -- | uF |
| $C_{OUT}$ | Output capacitor | 3.3 | 220 | uF |
| ESR | Output capacitor ESR requirements | 0.001 | 5 | Ω |
| $T_A$ | Operating ambient temperature | -40 | 125 | °C |
| $T_J$ | Operating junction temperature | -40 | 150 | °C |
| $V_{IN}$ | Input voltage range | 3 | 40 | V |

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted (1)

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Maximum input voltage range | -0.3 | 45 | V |
| $V_{OUT}$ | Maximum output voltage range | -0.3 | 25 | V |
| $V_{EN}$ | Maximum enable input voltage | -0.3 | $V_{IN}$ | V |
| $V_{FB}$ | Maximum feedback pin voltage | -0.3 | 5.5 | V |
| $T_J$ (2) | Junction temperature range | -40 | 150 | °C |
| $T_{stg}$ | Storage temperature range | -65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

## ESD RATINGS

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1) | -4.5 | +4.5 | kV |
| | Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2) | -2 | +2 | kV |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## THERMAL INFORMATION

| PARAMETER | THERMAL METRIC | ESOP-8 | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction to ambient thermal resistance(1) | 62.58 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 9.25 | |
| $\Psi_{JB}$ | Junction-to-board characterization parameter(1) | 34.7 | |
| $R_{\theta JCtop}$ | Junction to case thermal resistance(1) | 78.32 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance(1) | 35.65 | |

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT71402Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT71402Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

## ELECTRICAL CHARACTERISTICS

(1) $V_{IN}$=$V_{OUT}$+1V, $C_{OUT}$=10uF, $T_J$= -40°C~125°C, typical value is tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_{IN}$ | Operating input voltage | | 3 | | 40 | V |
| $V_{UVLO}$ | $V_{IN}$ UVLO Threshold | $V_{IN}$ rising | 2.38 | 2.5 | 2.81 | V |
| | Hysteresis | | | 10 | | mV |
| $I_{SHDN}$ | Shutdown current from VIN pin | EN=0, $V_{OUT}$=3.3V, $V_{IN}$=4.3V | | 0.29 | | μA |
| | | EN=0, $V_{OUT}$=5V, $V_{IN}$=6V | | 0.43 | | μA |
| | | EN=0, $V_{OUT}$=3.3V/5V, $V_{IN}$=12V | | 0.7 | | μA |
| $I_Q$ | Quiescent current from GND pin | EN float, no load, $V_{IN}$=$V_{OUT}$+1V | | 2.6 | | μA |
| | | EN float, no load, $V_{IN}$=12V | | 2.9 | | μA |
| **Regulated Output Voltage and Current** | | | | | | |
| $V_{OUT}$ | Output voltage accuracy | $T_J$= 25°C | -1% | | 1% | |
| | | $T_J$= -40°C~125°C | -2% | | 2% | |
| $\Delta V_{OUT}$ | Line regulation | $V_{IN}$=3V to 40V, Iout=1mA，OUT=FB | | 1 | | mV |
| | Load regulation | Iout=1mA to 200mA，OUT=3.3V | | 10 | | mV |
| $V_{DROP}$ | Dropout voltage(1) | $V_{IN}$=$V_{OUT}$-0.1V ,Iout =100mA | | 117 | | mV |
| | | $V_{IN}$=$V_{OUT}$-0.1V ,Iout =150mA | | 190 | | mV |
| | | $V_{IN}$=$V_{OUT}$-0.1V ,Iout =200mA | | 270 | | mV |
| $I_{OUT}$ | Output current | $V_{OUT}$ in regulation | 0 | | 200 | mA |
| $I_{SC\_VINLOW}$ | Short current limit | $V_{OUT}$=0V, VIN<30V | | 400 | | mA |
| $I_{SC\_VINHIGH}$ | Short current limit | $V_{OUT}$=0V, VIN>30V | | 310 | | mA |
| PSRR | Power supply rejection ratio(2) | $I_{OUT}$=10mA, f=1kHz, $C_{OUT}$=10μF | | 53 | | dB |
| | | $I_{OUT}$=10mA, f=10kHz, $C_{OUT}$=10μF | | 35 | | dB |
| | | $I_{OUT}$=10mA, f=100kHz, $C_{OUT}$=10μF | | 43 | | dB |
| **Enable and Soft-startup** | | | | | | |
| $V_{EN\_H}$ | Enable high threshold | | | 1.5 | | V |
| $V_{EN\_L}$ | Enable low threshold | | | 1.22 | | V |
| $V_{EN\_Hys}$ | Enable threshold hysteresis | | | 300 | | mV |
| $I_{EN\_0V}$ | Enable pin pull-up current | EN=0V | | 0.27 | | μA |
| $T_{SS}$ | Soft-start time | | | 1.5 | | mS |
| **Thermal Protection** | | | | | | |
| $T_{SD}$ | Thermal shutdown threshold(3) | $T_J$ rising | | 175 | | °C |
| | | Hysteresis | | 12 | | °C |

(2) The dropout voltage is defined as $V_{IN}$-$V_{OUT}$, when force $V_{IN}$ is 100mV below the value of $V_{OUT}$ for $V_{IN}$=$V_{OUT(NOM)}$+1V.

(3) PSRR is derived from bench characterization, not production test.

(4) Thermal shutdown threshold is derived from bench characterization, not production test.

## TYPICAL CHARACTERISTICS

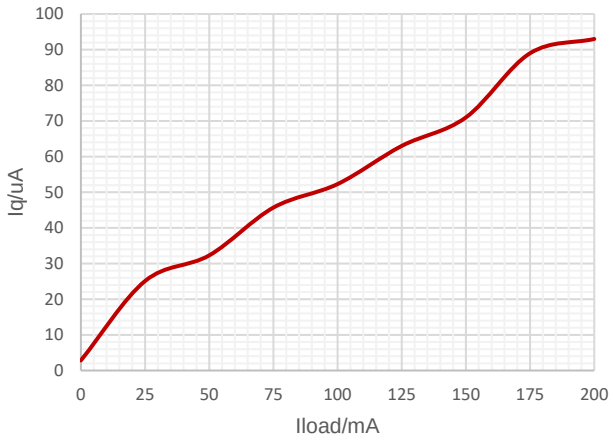



Figure 1. Quiescent Current vs Output Current

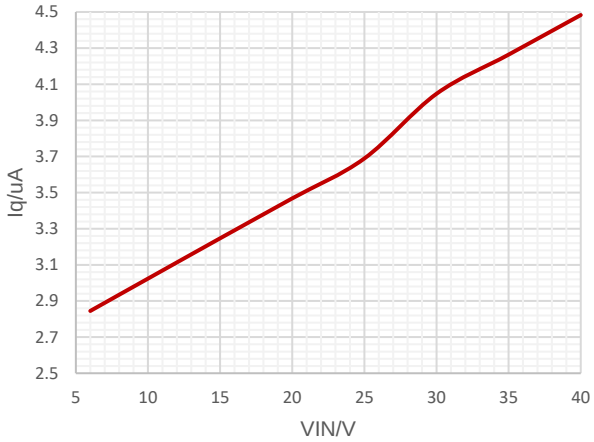



Figure 2. Quiescent Current vs Input Voltage, No load

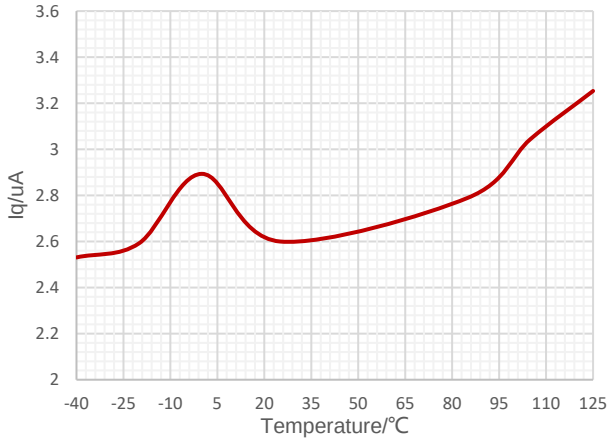



Figure 3. Quiescent Current vs Ambient Temperature

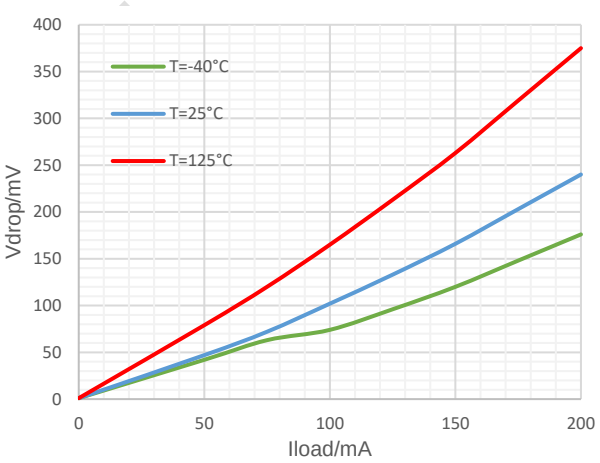



Figure 4. Dropout Voltage vs Output Current

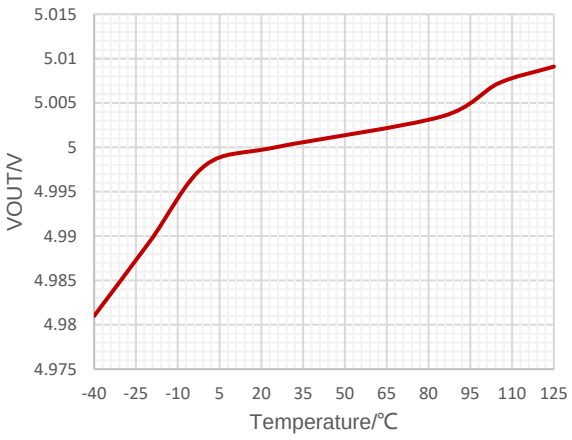



Figure 5. Output Voltage vs Ambient Temperature at VOUT=5V

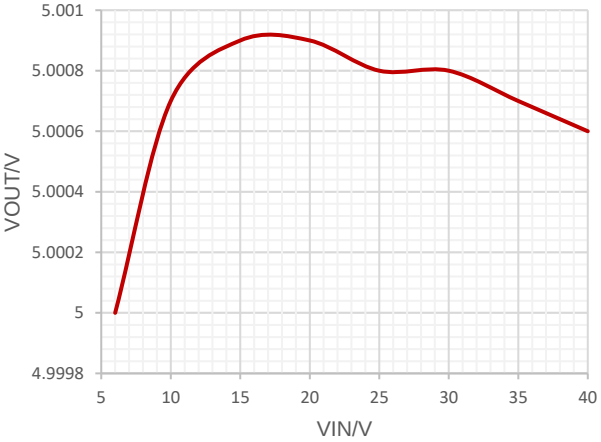



Figure 6. Output Voltage vs Input Voltage

## TYPICAL CHARACTERISTICS (continued)

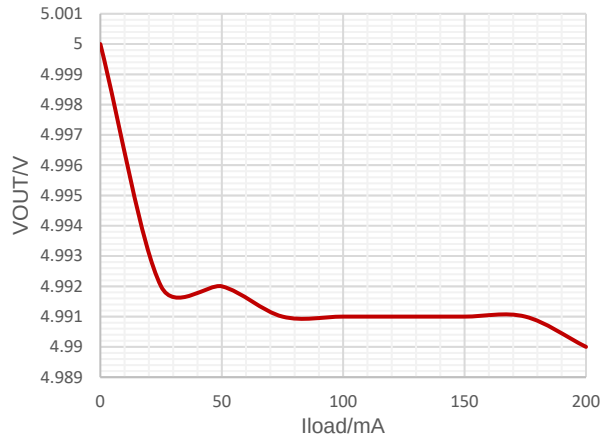



Figure 7. Output Voltage vs Output Current

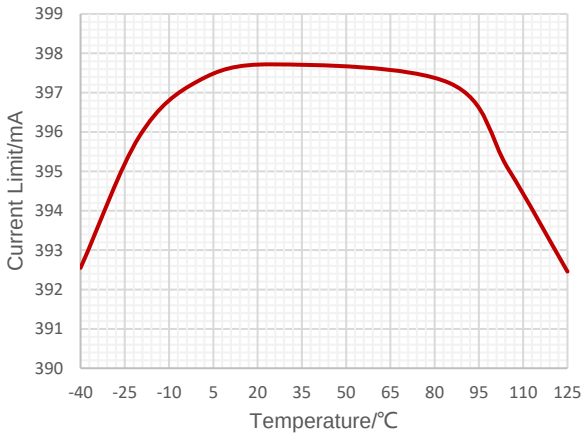



Figure 8. Output Current Limit vs Ambient Temperature at VIN<30V

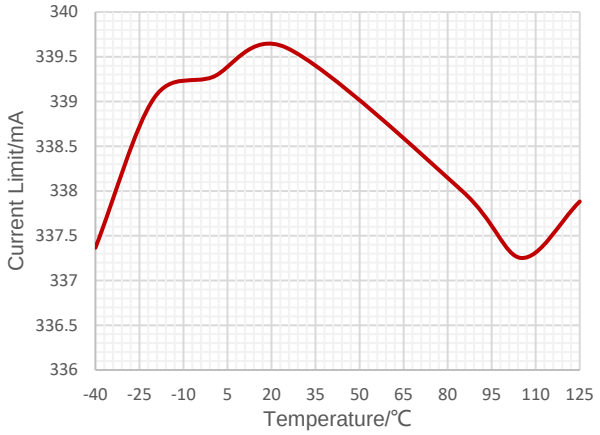



Figure 9. Output Current Limit vs Ambient Temperature at VIN≥30V

## TYPICAL CHARACTERISTICS (continued)

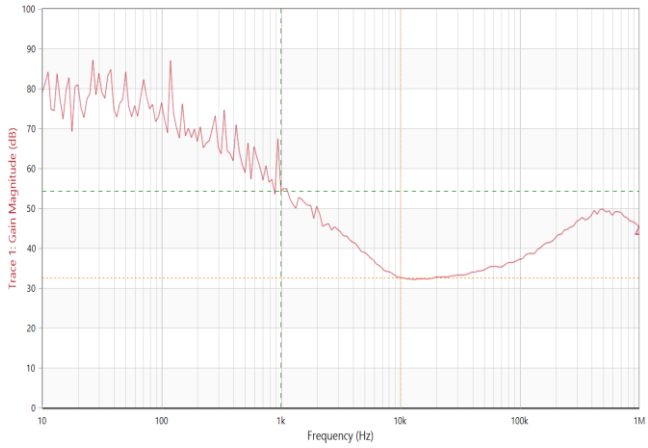



Figure 10. PSRR vs Frequency at Iout=10mA, $C_{OUT}$=4.7uF

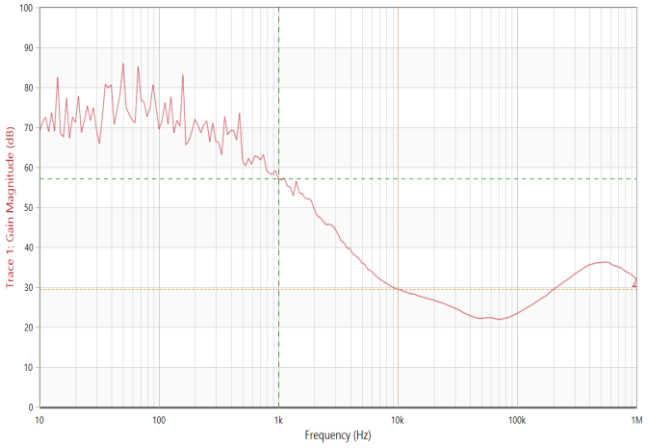



Figure 11. PSRR vs Frequency at Iout=100mA, $C_{OUT}$=4.7uF

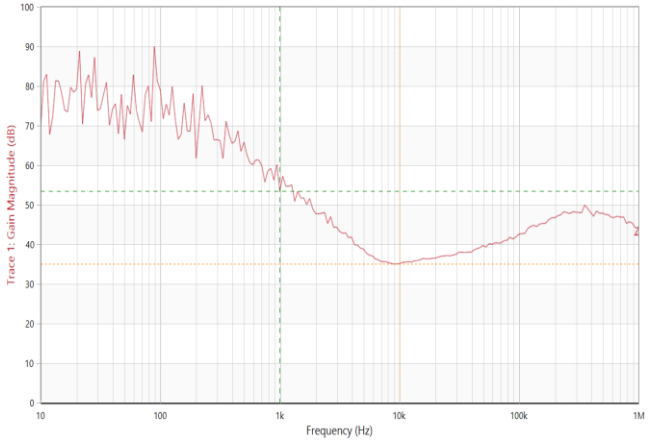



Figure 12. PSRR vs Frequency at Iout=10mA, $C_{OUT}$=10uF

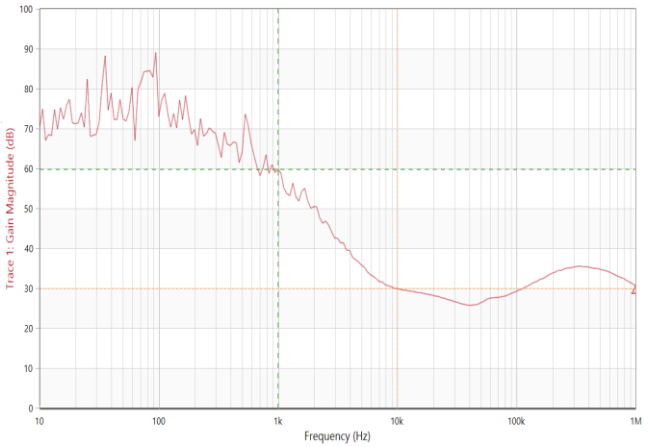



Figure 13. PSRR vs Frequency at Iout=100mA, $C_{OUT}$=10uF

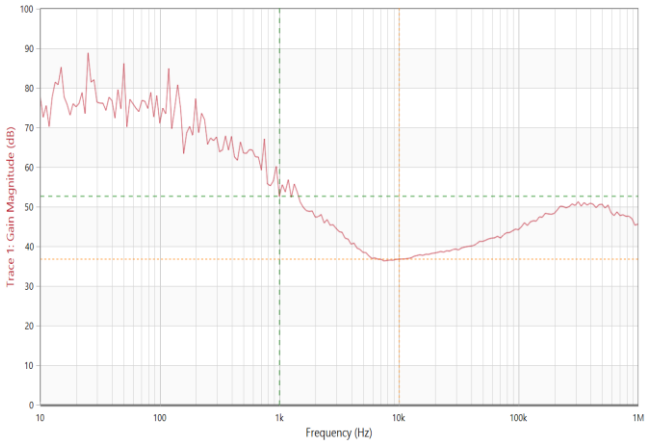



Figure 14. PSRR vs Frequency at Iout=10mA, $C_{OUT}$=22uF

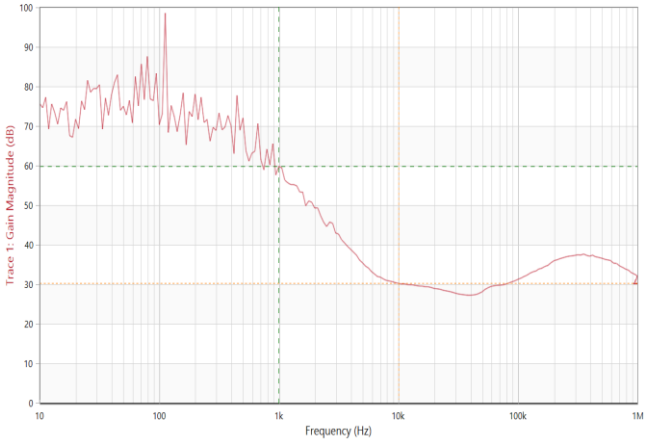



Figure 15. PSRR vs Frequency at Iout=100mA, $C_{OUT}$=22uF

## FUNCTIONAL BLOCK DIAGRAM

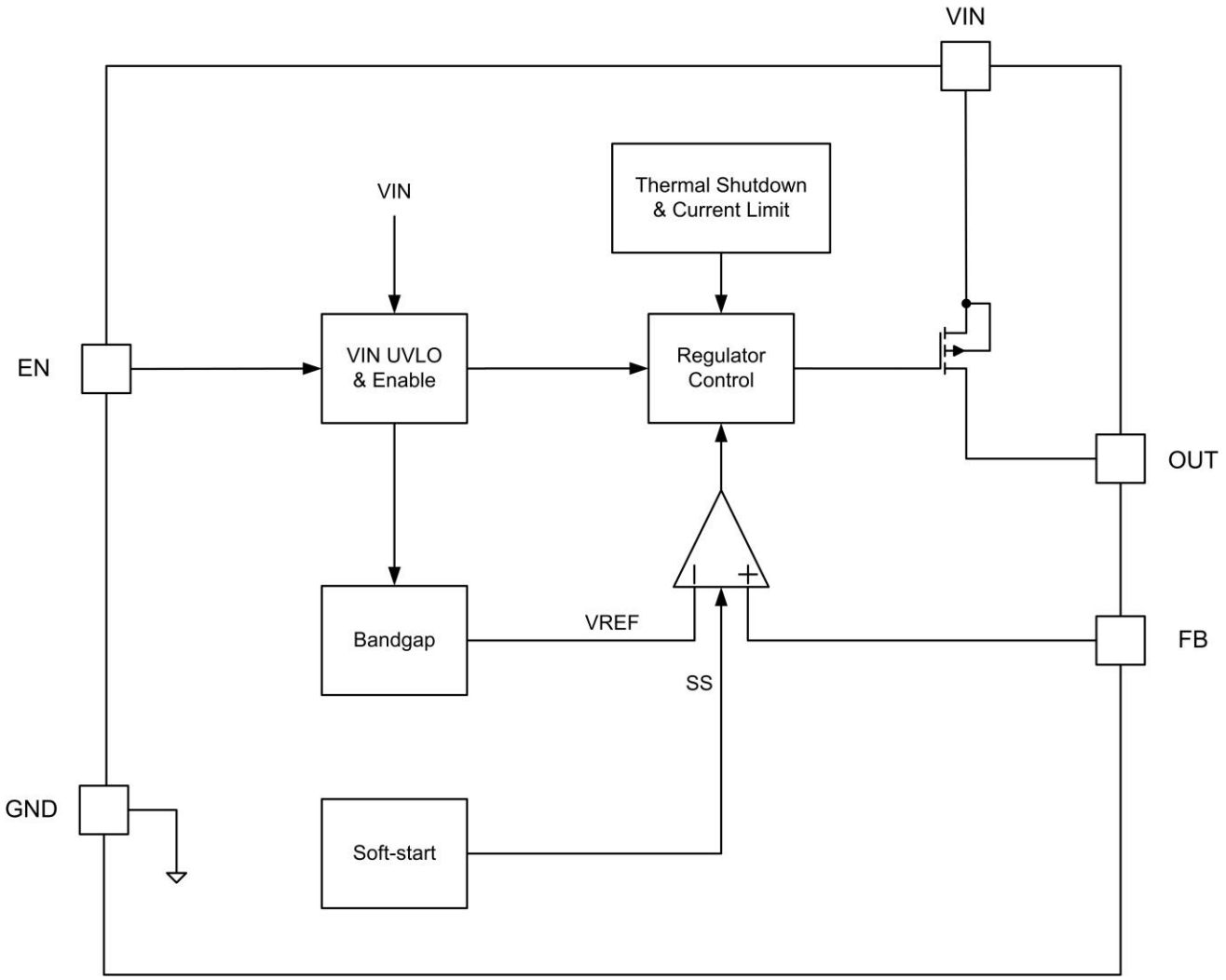



Figure 16. Functional Block Diagram

# OPERATION

### Overview

The SCT71402Q series products are 200mA wide input voltage range linear regulators with very low quiescent current. These voltage regulators operate from 3V to 40V DC input voltage with supporting 45V transient input voltage and consume 2.6μA quiescent current at no load.

The SCT71402Q series products is stable with 3.3uF~220uF output capacitors, and 10uF ceramic capacitor is recommended. An internal 1.5ms soft-start time avoids large inrush current and output voltage overshoot during startup.

The SCT71402Q series products also provide enable control. Other protection features include the VIN input under-voltage lockout, over current protection and output hard short protection with VIN_HIGH Control feature, which makes the device more reliable during transient high-load current faults or shorting events. And thermal shutdown protection.

The SCT71402Q series products provide adjustable output version which can adjust the output voltage from 1.215V to 25V with 1% output voltage accuracy at room temp and 2% output voltage accuracy over operating conditions. The series products are available in TDFN3X3-8 packages.

If you need a new output voltage version or a new package option, please feel free to contact SCT sales.

### Enable and Under Voltage Lockout Threshold

The SCT71402Q series products is enabled when the VIN pin voltage rises above 2.5V and the EN pin voltage exceeds the enable threshold $V_{EN\_H}$. The device is disabled when the VIN pin voltage falls below 2.5V or when the EN pin voltage is below $V_{EN\_L}$. Internal pull up current source to EN pin allows the device enable when EN pin floats.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) from VIN to GND shown in Figure 17. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$VIN_{rise} = V_{EN\_H} * \frac{R1 + R2}{R2} \quad (1)$$

$$VIN_{hys} = (V_{EN\_H} - V_{EN_L}) * \frac{R1 + R2}{R2} \quad (2)$$

Where

$VIN_{rise}$: Vin rise threshold to enable the device

$VIN_{hys}$: Vin hysteresis threshold

$I_1$=0.27uA and could be neglected in the calculation

$V_{EN\_H}$=1.5V

$V_{EN\_L}$=1.22V

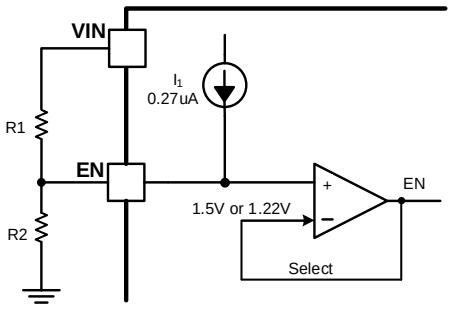



Figure 17. System UVLO by enable divide

### Regulated Output Voltage

The SCT71402Q series products provide adjustable output version which can adjust the output voltage from 1.215V to 25V. When the input voltage is higher than $V_{OUT(NOM)}$+$V_{DROP}$, output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT(NOM)}$+$V_{DROP}$, output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below UVLO threshold, the output keeps shut off.

Please feel free to contact SCT sales, if you need a new output voltage version or a new package option.

### Over Current Limit and Foldback Current Limit

The SCT71402Q series products has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is 400mA when VIN<30V, but SCT71402Q supplies a fold-back current limit 310mA when VIN>30V.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown.

With the over current foldback limit feature, the SCT71402Q series products would be more robust and safer when over current faults and shorting events occur. But it also requires the maximum loading current should be smaller than Isc during startup. The characteristic is shown in the following figure.

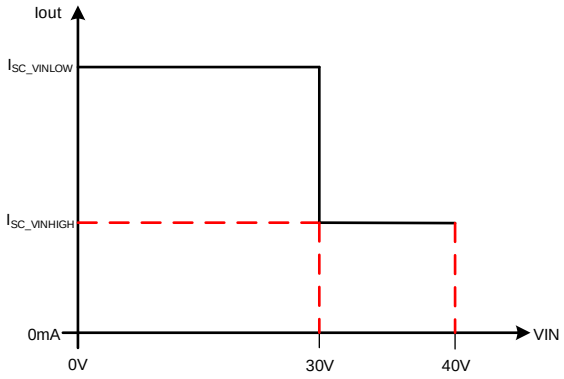



Figure 18. Current Limit with Foldback Feature

### Internal Soft-Start

The SCT71402Q series products integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.6V reference voltage in 1.5ms. If the EN pin is pulled below 1.22V, LDO will be shut off and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Below figure shows the startup waveform at small output capacitor and large output capacitor. When output capacitor is small, for example 10uF, the slope of VOUT is limit by soft-start. When output capacitor is large, for example 100uF, the slope of VOUT is limited by current limit ($I_{SC\_VINLOW}$) at VIN<30V, and the slope of VOUT is limited by current limit ($I_{SC\_VINHIGH}$), when VIN> 30V.

In SCT71405 series products, typical Tss is 1.5ms, and typical $I_{SC\_VINLOW}$ is 400mA and typical $I_{SC\_VINHIGH}$ is 310mA, could use the following formula for initial startup time calculation.

$$\text{Tstart} = \max\left\{\frac{C_{OUT}\times V_{OUT}}{(I_{sc}-I_{load})}, T_{SS}\right\} \quad (3)$$

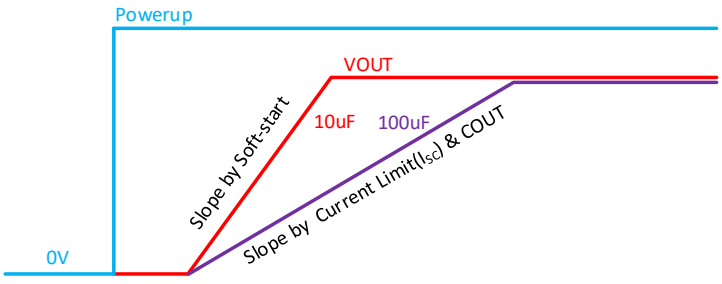



Figure 19. Soft-start Waveform vs Output Capacitor

### Thermal Shutdown

This device incorporates a thermal shutdown ($T_{SD}$) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the $T_{SD}$ trip point. The junction temperature exceeding the $T_{SD}$ trip point causes the output to turn off. When the junction temperature falls below the $T_{SD}$ trip point minus thermal shutdown hysteresis, the output turns on again.

## APPLICATION INFORMATION

**Typical application 1:**

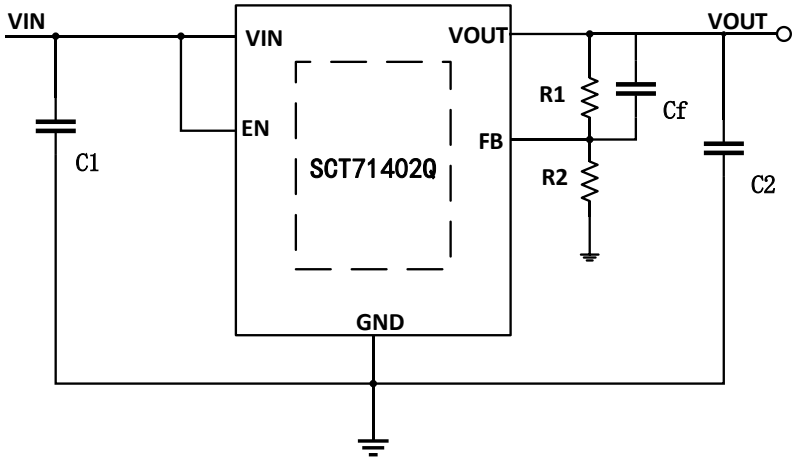



Figure 20. SCT71402Q Typical Application Schematic

**Design Parameters**

| Design Parameters | Example Value |
|---|---|
| Input Voltage | 12V Normal, 3V~40V |
| Output Voltage | 5V Normal, 1.215V~25V |
| Maximum Output Current | 200mA |
| Output Capacitor Range ($C_2$) | 3.3uF~220uF , recommends 10uF |
| Input Capacitor Range ($C_1$) | >2.2uF , recommends 10uF |

**Typical application 2:**

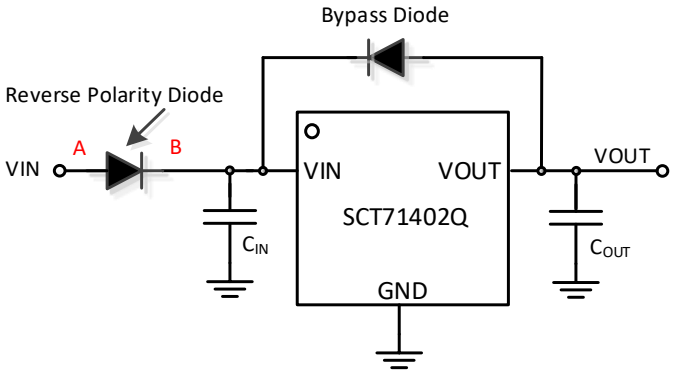



Figure 21. SCT71402Q Typical Application Schematic with Reverse Polarity Diode

**Design Parameters**

| Design Parameters | Example Value |
|---|---|
| Input Voltage | 12V Normal, 3V~40V |
| Output Voltage | 5V Normal, 1.215V~25V |
| Maximum Output Current | 200mA |
| Output Capacitor Range ($C_{OUT}$) | 3.3uF~220uF , recommends 10uF |
| Input Capacitor Range ($C_{IN}$) | >2.2uF , recommends 10uF |

In some applications, the VIN and the VOUT potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VOUT to the VIN when the VIN shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 220μF. Also by inserting a reverse polarity diode in series to the VIN, it can prevent reverse current from reverse battery connection or the case, when the point A is short-circuited GND. If there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VIN and the VOUT.

**Typical application 3:**

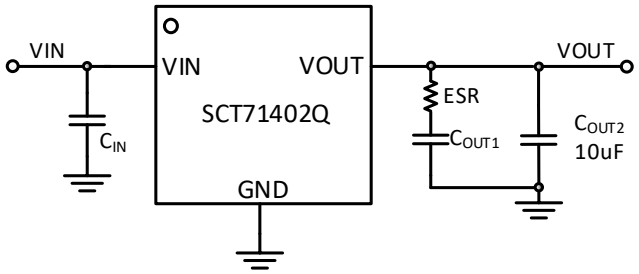



Figure 22. SCT71402Q Typical Application Schematic with Large Output Capacitor

**Design Parameters**

| Design Parameters | Example Value |
|---|---|
| Input Voltage | 12V Normal, 3V~40V |
| Output Voltage | 5V Normal, 1.215V~25V |
| Maximum Output Current | 200mA |
| Output Capacitor Range ($C_{OUT1}$ and ESR) | 3.3uF~220uF with ESR=0.5Ω~5Ω |
| Output Capacitor Range ($C_{OUT2}$) | recommends 10uF with low ESR |
| Input Capacitor Range ($C_{IN}$) | >2.2uF , recommends 10uF |

### Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 100KΩ. Use equation 4 to calculate R1.

$$R_1 = \left(\frac{V_{OUT}}{1.215\text{V}} - 1\right) * R_2 \quad (4)$$

**Table 1: Compensation Values for Typical Output Voltage/Capacitor Combinations**

| Vout/V | COUT/uF | Cf/pF | R1/KΩ | R2/KΩ | COUT1/uF (optional) | ESR/Ω |
|---|---|---|---|---|---|---|
| 1.8 | 33 | 68 | 48.7 | 100 | 220 | 1 |
| 2.5 | 33 | 33 | 105 | 100 | 220 | 1 |
| 3.3 | 15 | 22 | 174 | 100 | 220 | 1 |
| 5 | 15 | 10 | 309 | 100 | 220 | 1 |
| 12 | 15 | 3.3 | 887 | 100 | 220 | 1 |

### Input Capacitor and Output Capacitor

SCT recommends adding a 2.2μF or greater capacitor with a 0.1μF bypass capacitor in parallel at VIN pin to keep the input voltage stable. Aluminum electrolytic capacitor or other capacitor with high capacitance is suggested for the system power with large voltage spike. The voltage rating of the capacitors must be greater than the maximum input voltage

To ensure loop stability, the SCT71402Q series products requires an output capacitor with a minimum effective capacitance value of 3.3μF. And the series products could support output capacitor range from 3.3uF to 220uF and with an ESR range between 0.001Ω and 5Ω. SCT recommends selecting a X5R- or X7R-type 4.7uF~10uF ceramic capacitor with low ESR over temperature range to improve the load transient response.

When using large output capacitor with higher ESR resistor, for example 100uF output electrolytic capacitor with 1Ω ESR resistor in the application, SCT recommends adding extra 10uF low ESR output capacitor parallel connection with the large electrolytic capacitor, this will eliminate the undershoot/overshoot voltage caused by the large ESR resistor and get better load transient performance.

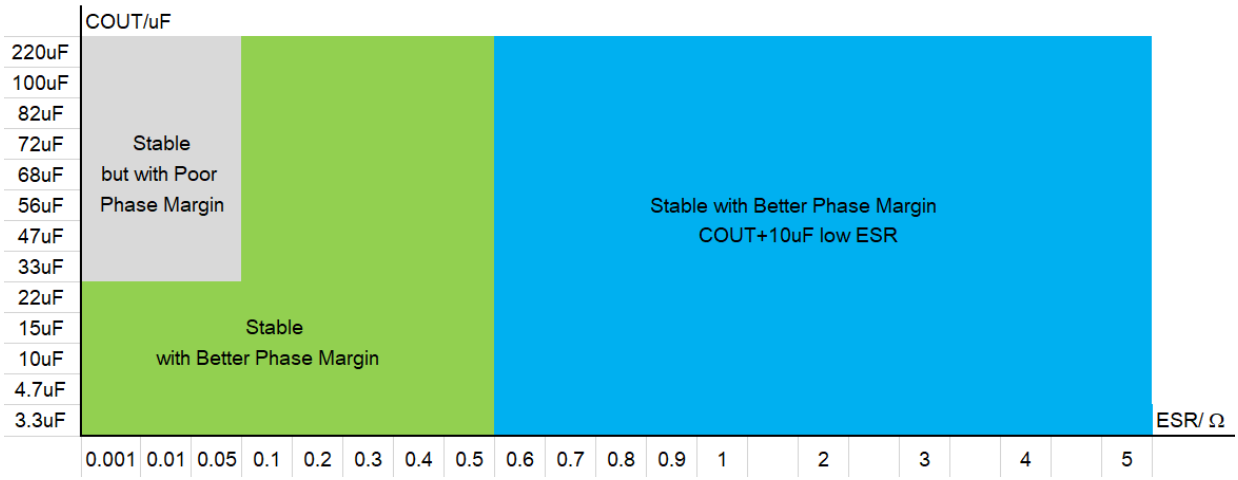



Figure 23. SCT71402Q Stability vs Output Capacitor

**Power Dissipation and Thermal Performance**

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum junction temperature is dependent on power dissipation, package, the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

During normal operation, LDO junction temperature should not exceed 150°C, or else it may result in deterioration of the properties of the chip. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 5. Because $I_{GND}$ « $I_{OUT}$, the term $V_{IN}$ x $I_{GND}$ in Equation 5 could be ignored.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (5)$$

The junction temperature can be estimated using Equation 6. $R_{\theta JA\_EVM}$ is the junction-to-ambient thermal resistance based on customer's PCB. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature $T_J$.

$$T_J = T_A + P_D \times R_{\theta JA\_EVM} \quad (6)$$

$R_{\theta JA\_EVM}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

For the SCT71402Q series products, the maximum allowable power dissipation of different packages was listed in the following table, and the test results are based on our EVM board, larger power dissipation will trigger thermal shutdown protection. As a result, we could calculate the $R_{\theta JA\_EVM}$ of different packages. The following table is just for your reference based on our EVM test, please leave enough margin when you design thermal performance.

The PCB information of our EVM : 2-layer, 1 oz Cu, 50mm x 30mm size.

**Thermal Performance of Different Packages Based on EVM Test**

| Package | Max Allowable PD (W) (Not Trigger TSD,VOUT=5V) | Max Allowable PD (W) (TJ≤150℃) | $R_{\theta JA\_EVM}$ (℃/W) |
|---|---|---|---|
| TDFN3x3 | 3.786 | 3.264 | 38.3 |

## THERMAL CHARACTERISTICS

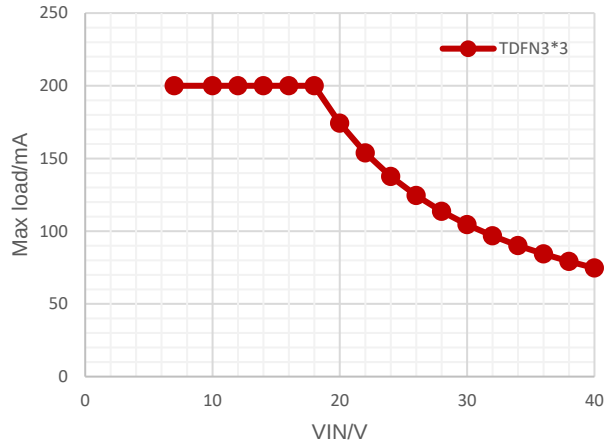



Figure 24. Maximum Output Current vs Input Voltage, VOUT=5V of TDFN3X3 ,$T_J$ ≤ TSD_R

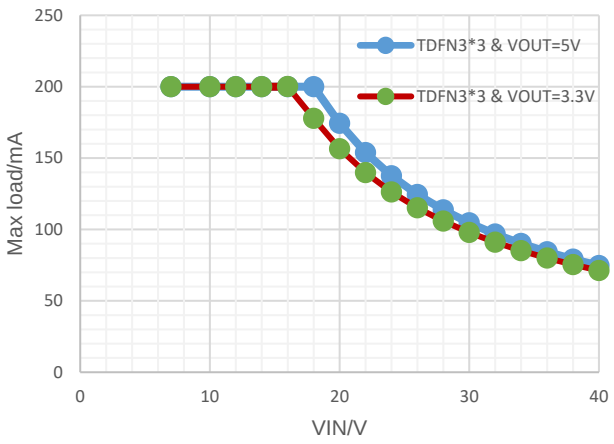



Figure 25. Maximum Output Current vs Input Voltage, TDFN3X3,TJ ≤ 150℃

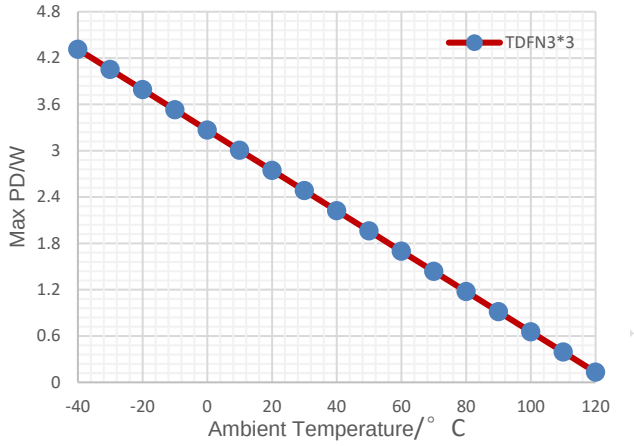



Figure 26. Maximum Allowed Power Dissipation vs Ambient Temperature, TDFN3X3,TJ ≤ 150℃

### Application Waveforms

Vin=Vout +1V, unless otherwise noted

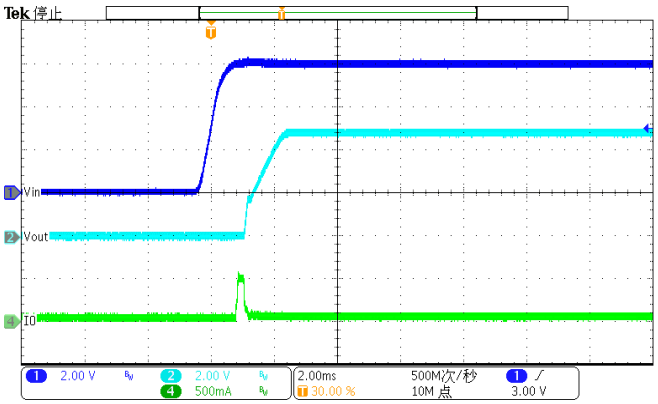



Figure 27. Power up (Iload=10mA)

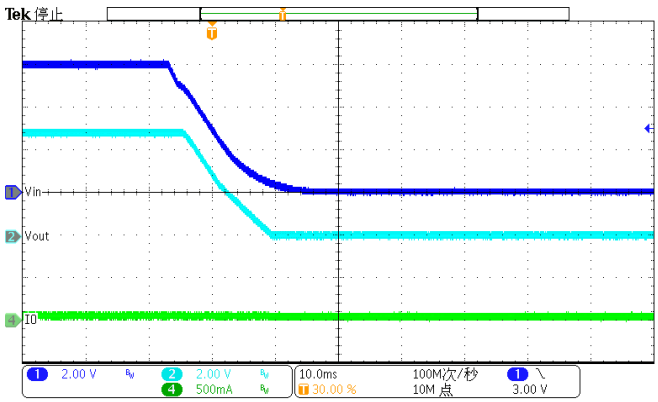



Figure 28. Power down (Iload=10mA)

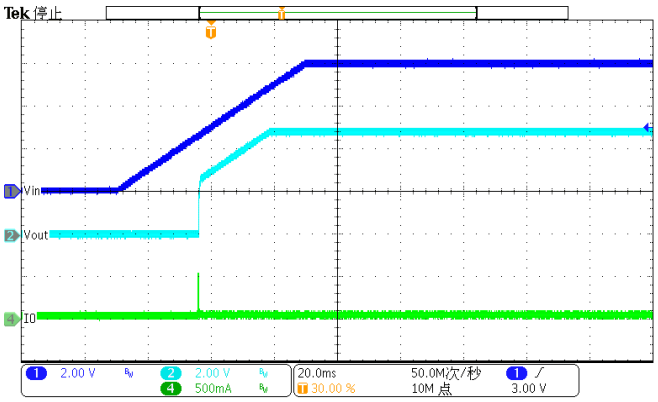



Figure 29. Slow Power up (Iload=10mA)

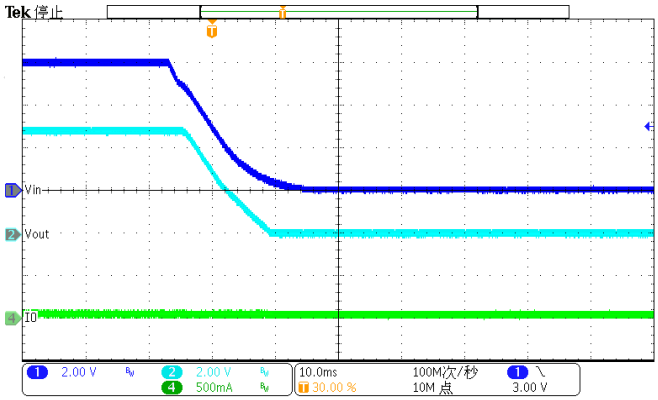



Figure 30. Slow Power down (Iload=10mA)

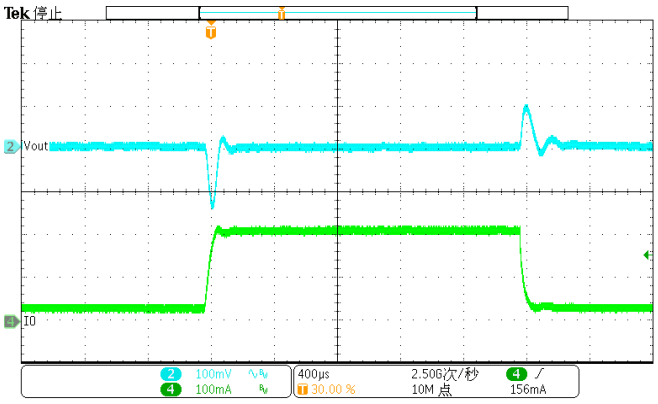



Figure 31. DC-DC Load Transient (20mA-180mA),VOUT=5V

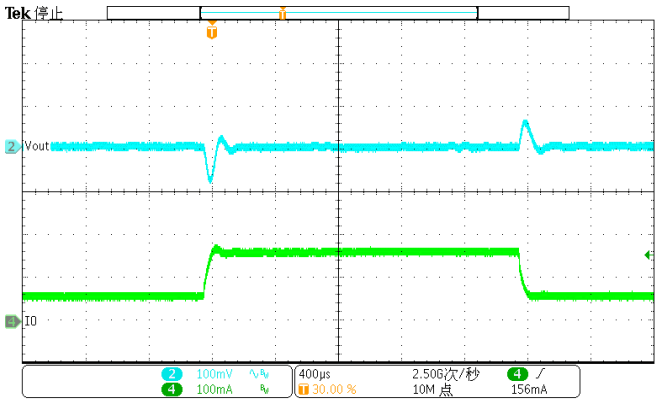



Figure 32. DC-DC Load Transient (50mA-150mA),$V_{OUT}$=5V

**Application Waveforms(Continued)**

Vin=Vout +1V, unless otherwise noted

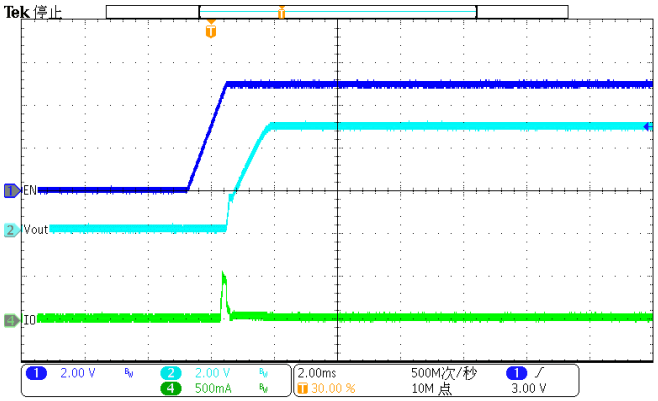



Figure 33. Enable (Iload=10mA)

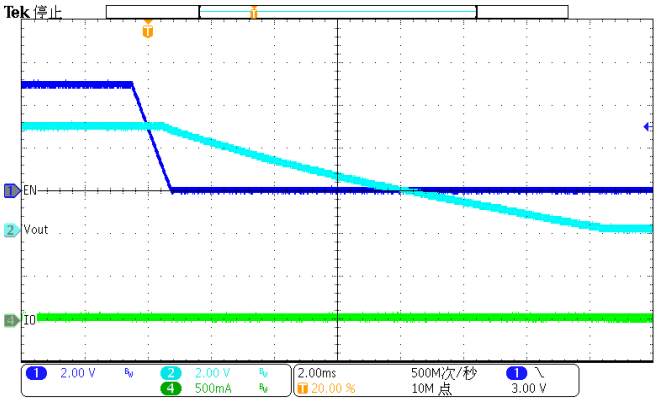



Figure 34. Disable (Iload=10mA)

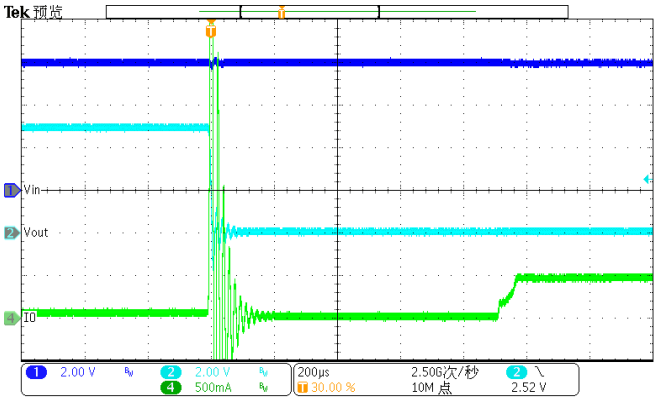



Figure 35. Enter Short Circuit Protection

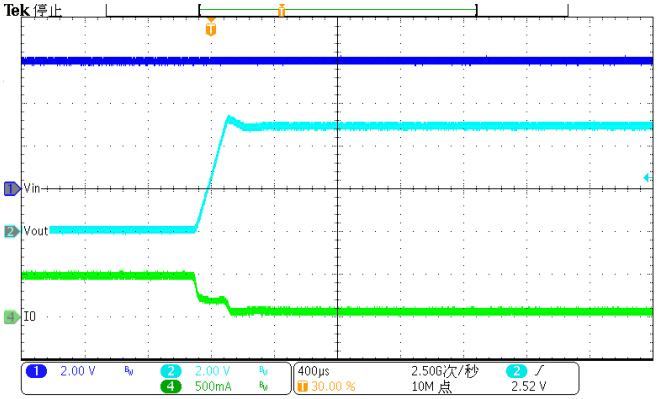



Figure 36. Exit Short Circuit Protection

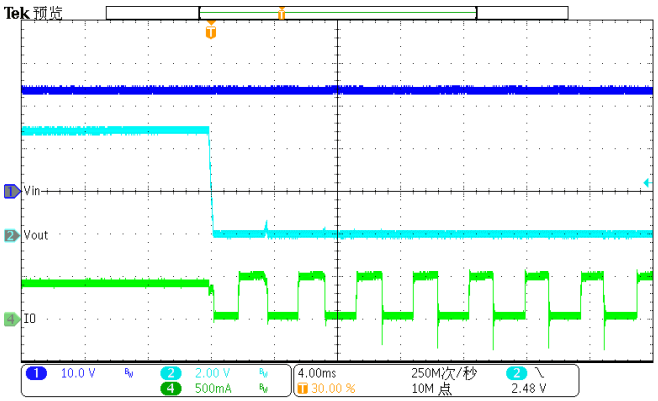



Figure 37. Enter Over Temperature Protection(Vin=24V)

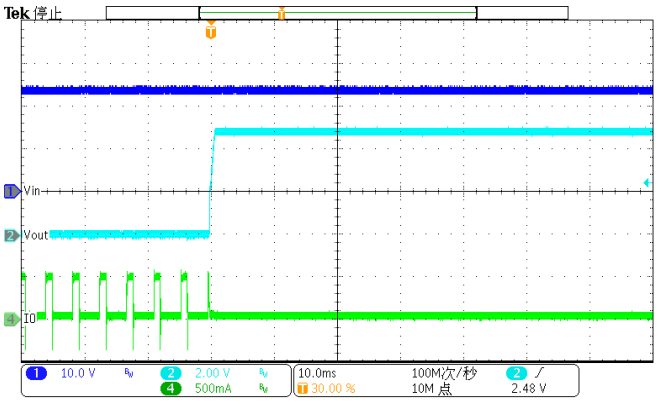



Figure 38. Exit Over Temperature Protection(Vin=24V)

### Layout Guideline

Proper PCB layout is a critical for SCT71402Q's stability, transient performance and good regulation characteristics. For better results, follow these guidelines as below:

1. Both input capacitors and output capacitors must be placed as close to the device pins as possible.
2. It is recommended to bypass the input pin to ground with a 0.1μF bypass capacitor. The loop area formed by the bypass capacitor connection, $V_{IN}$ pin and the GND pin of the system must be as small as possible.
3. It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.
4. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, SCT recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad.
5. If using large electrolytic capacitor with high ESR resistor, SCT recommends adding a 10uF low ESR capacitor parallel connection with the large electrolytic capacitor.

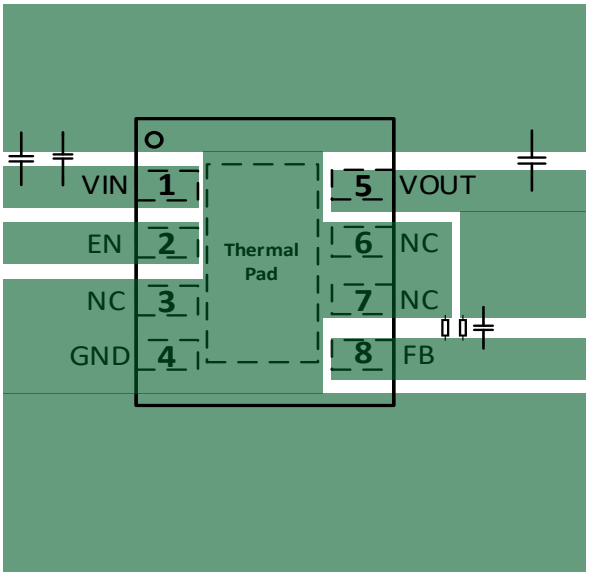
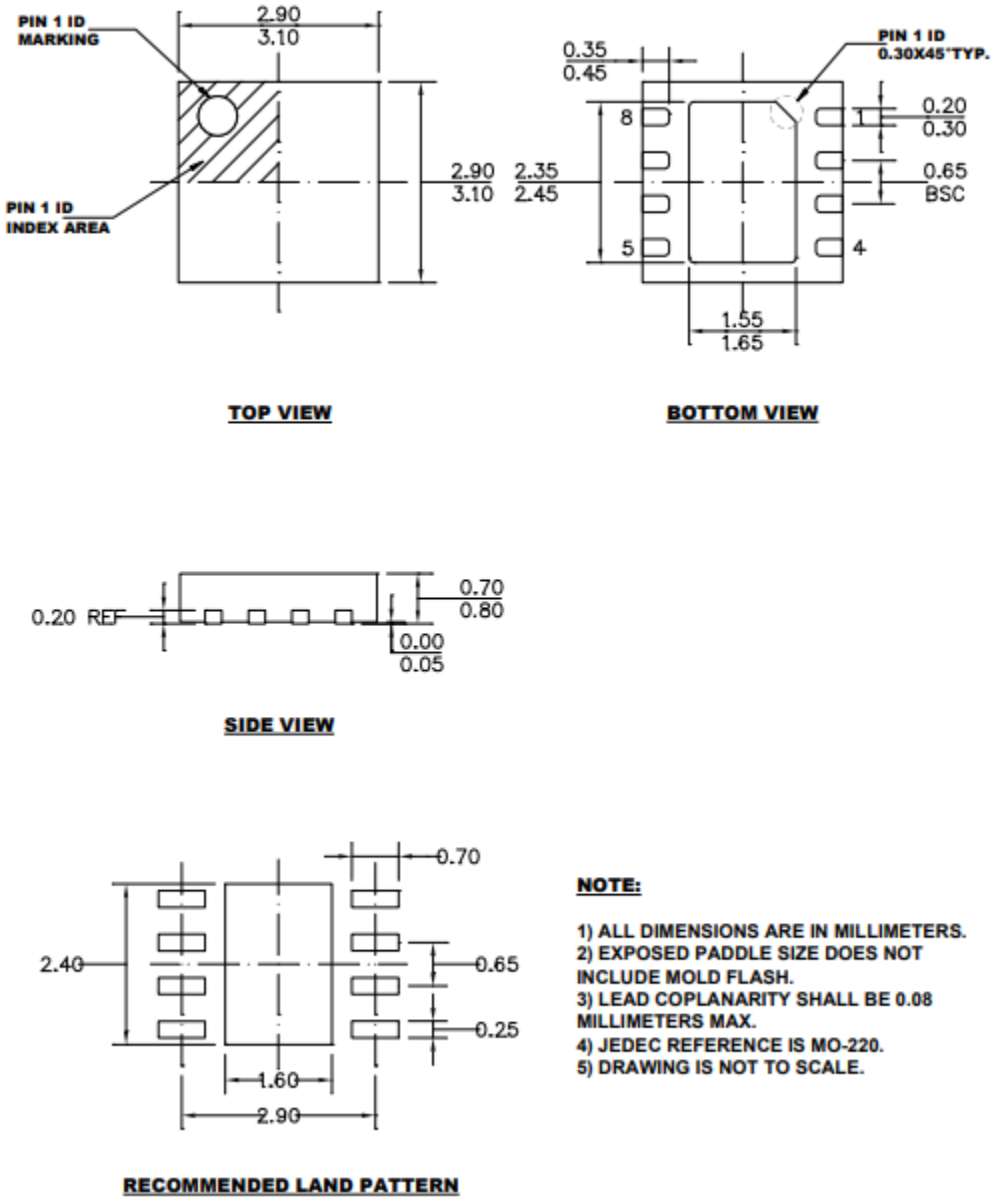



Figure 39. PCB Layout Example

**SCT71402A00QDTBR**

## PACKAGE INFORMATION




TDFN3x3-8 Package Outline Dimensions

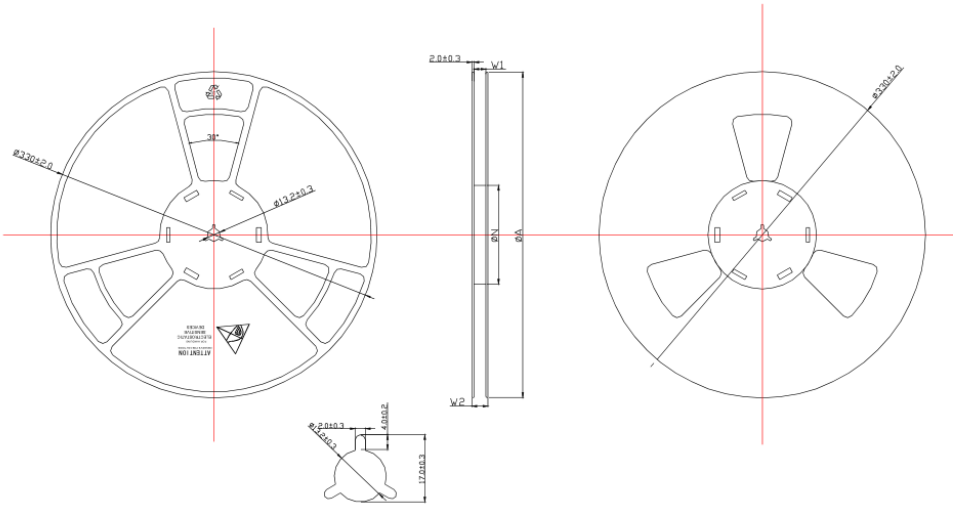
**NOTE:**

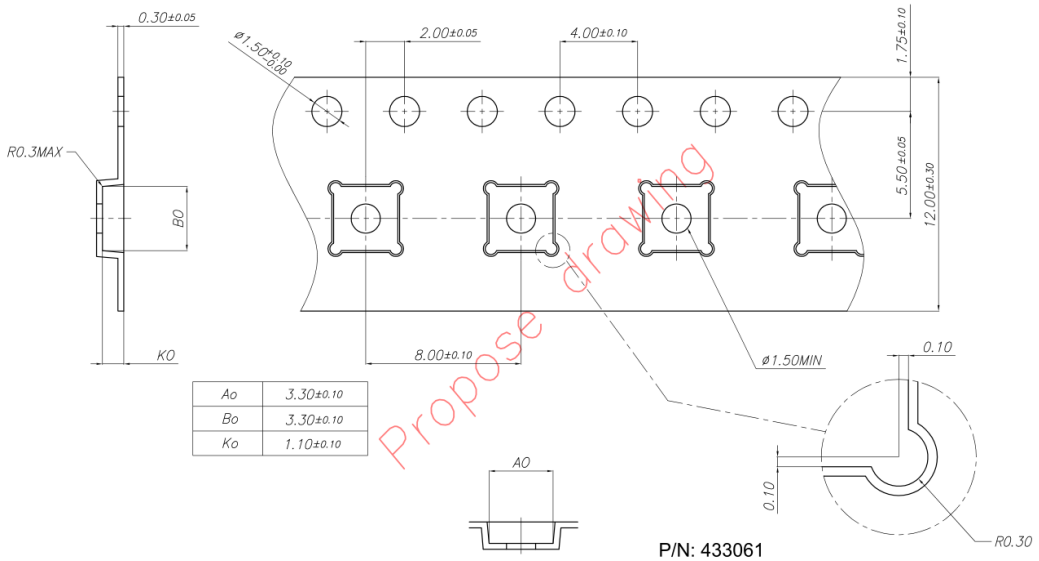
1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

## TAPE AND REEL INFORMATION

| Orderable Device | Package Type | Pins | SPQ |
|---|---|---|---|
| SCT71402Q Series | TDFN3x3-8 | 8 | 5000 |



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